Deeper Sampling CMOS Transient Waveform Recording ASICs

The IRS and BLAB3 Deep Storage ASICs for UHE Radio Neutrino and Next Generation Collider Particle Identification

Matt Andrew, Kurtis Nishimura, Gary S. Varner
University of Hawai’i, and the Large Area Picosecond PhotoDetector Collaboration

TIPP 2011, June 10, 2011
Why Waveform Sampling?

• Traditional “crate based” electronics
  – Gated Analog-to-Digital Converters
  – Referenced “triggered” Time-to-Digital Converters

• High-rate applications
  – “pipelined operation”
  – Low-speed, low-resolution sampling

• High channel counts
  – Motivation to reduce cabling
  – Integrate electronics onto detector elements

Issues: cost, power, resolution, data volume
Switched Capacitor Array Sampling

• Write pointer is ~few switches closed @ once

Tiny charge: 1mV ~ 100e⁻
“Oscilloscope on a chip”

PMT pulse comparison

- 2 GSa/s, 1GHz ABW Tektronics Scope
- 2.56 GSa/s LAB
Easy access to Waveform sampling

<table>
<thead>
<tr>
<th></th>
<th>WFS ASIC</th>
<th>Commercial</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sampling speed</td>
<td>0.1-6 GSa/s</td>
<td>3 GSa/s</td>
</tr>
<tr>
<td>Bits/ENOBs</td>
<td>16/9-13+</td>
<td>8/7.4</td>
</tr>
<tr>
<td>Power/Chan.</td>
<td>&lt;= 0.05W</td>
<td>Few W</td>
</tr>
<tr>
<td>Cost/Ch.</td>
<td>&lt; $10 (vol)</td>
<td>&gt; 100$</td>
</tr>
</tbody>
</table>
An Intrinsic Limitation

No power (performance savings) for continuous digitization

We aren’t going to put Analog Devices out of business

“analog down conversion”

→ For most “triggered” ‘event’ applications, not a serious drawback
Gigasamples/s, but Nyquist?

Difficult to couple in Large BW (input C is deadly)

More than 3pF input (ESD protection alone often more) limits ABW < 1GHz

As a result, first generation WFS ASICs a few hundred to 1k samples (ATWD, SAM, DRS, LABRADOR...)

Is this an fundamental limitation?
Why Deeper sampling?

Legend:
- Green line: Power/comms cable
- Orange dot: Power/comms/calib. station
- Blue dot: Testbed station
- Yellow dot: Production Station

Askaryan Radio Array

CLEAN AIR SECTOR

South Pole Operation zone

QUIET CIRCLE

QUIET SECTOR

DARK SECTOR

1.33 km

Runway

Belle II

10^{18} \text{ eV } \nu_\mu

\sim \text{ km}

Secondary showers

Primary vertex

\sim 2850 \text{ mm}
Deeper storage: Buffered LABRADOR (BLAB1) ASIC

- Single channel
- 64k samples deep, same SCA technique as LAB, no ripple pointer
- Multi-MSa/s to Multi-GSa/s
- 12-64us to form Global trigger

3mm x 2.8mm, TSMC 0.25um
BLAB1 High speed Waveform sampling

• Comparable performance to best CFD + HPTDC
• MUCH lower power, no need for huge cable plant!
• Using full samples reduces the impact of noise
• Photodetector limited

NIM A602 (2009) 438
Ice Radio Sampler (IRS) / Buffered LABRADOR 3 (BLAB3) Specifications

<table>
<thead>
<tr>
<th>32768 samples/chan (8-32us trig latency)</th>
<th>8 channels/IRS ASIC</th>
</tr>
</thead>
<tbody>
<tr>
<td>8 Trigger channels</td>
<td>~9 bits resolution (12-bits logging)</td>
</tr>
<tr>
<td>64 samples convert window (~16-64ns)</td>
<td>1-4 GSa/s</td>
</tr>
<tr>
<td>1 word (RAM) chan, sample readout</td>
<td>16 us to read all samples</td>
</tr>
<tr>
<td>100's Hz sustained readout (multibuffer)</td>
<td></td>
</tr>
</tbody>
</table>

- **Difference between IRS/BLAB**
  - BLAB has input amplifier
  - IRS doesn’t really use internal trigger capability
IRS/BLAB3
Single Channel

- **Sampling:** 128 (2x 64) separate transfer lanes

  Recording in one set 64, transferring other ("ping-pong" → "2 stage sampling")

- **Storage:** 64 x 512 (512 = 8 * 64)

- **Wilkinson (32x2):**
  64 conv/channel
IRS/BLAB Die photo

5.82mm

7.62mm

8x RF inputs (die upside down)

32k storage cells per channel (512 groups of 64)
Analog bandwidth

ADC Frequency response

Analog BW
~1GHz
Input coupling simulation (35fF sample)

~1 GHz stored

Onto chip (flip chip)
Wilkinson ADC – easy to integrate on-chip

- No missing codes
- Linearity as good as can make ramp
- Can bracket range of interest

- Excellent linearity
- Basically as good as can make current source/comparator

12-bit ADC

Labrador ADC Performance

\[ y = 1606.8x + 105.26 \]
\[ R^2 = 0.9999 \]

Modified! (on-chip clock/counter) 
[~0.7 GHz]
• **Diff. Pair as comparator**
  - Density ~ 25k storage cells/mm\(^2\) (0.25um)
On chip Wilkinson Clock

\[ \text{Wilk. CLK (MHz)} \]

\[ \text{delta V} \]

~1us to 9-10 bits
~4us to 12 bits
512 ADC in parallel
Linearity Calibration

CAM and/or LUT in FPGA
Example: 100 MHz sine wave input

- Need dT calibrations – but only 128 per channel
- Any way to automate? (see K. Nishimura talk)
Not a small effect

More like 10% effect at 3.2GSa/s
Now a variety of options...

<table>
<thead>
<tr>
<th>ASIC</th>
<th>Amplification?</th>
<th># chan</th>
<th>Depth/chan</th>
<th>Sampling [GSa/s]</th>
<th>Vendor</th>
<th>Size [nm]</th>
<th>Ext ADC?</th>
</tr>
</thead>
<tbody>
<tr>
<td>DRS4</td>
<td>no.</td>
<td>8</td>
<td>1024</td>
<td>1-5</td>
<td>IBM</td>
<td>250</td>
<td>yes.</td>
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<tr>
<td>SAM</td>
<td>no.</td>
<td>2</td>
<td>1024</td>
<td>1-3</td>
<td>AMS</td>
<td>350</td>
<td>yes.</td>
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<tr>
<td>IRS2</td>
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<td>32536</td>
<td>1-4</td>
<td>TSMC</td>
<td>250</td>
<td>no.</td>
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<tr>
<td>BLAB3A</td>
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<td>8</td>
<td>32536</td>
<td>1-4</td>
<td>TSMC</td>
<td>250</td>
<td>no.</td>
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<tr>
<td>TARGET</td>
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<td>4192</td>
<td>1-2.5</td>
<td>TSMC</td>
<td>250</td>
<td>no.</td>
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<tr>
<td>TARGET2</td>
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<td>16384</td>
<td>1-2.5</td>
<td>TSMC</td>
<td>250</td>
<td>no.</td>
</tr>
<tr>
<td>TARGET3</td>
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<td>16</td>
<td>16384</td>
<td>1-2.5</td>
<td>TSMC</td>
<td>250</td>
<td>no.</td>
</tr>
<tr>
<td>PSEC3</td>
<td>no.</td>
<td>4</td>
<td>256</td>
<td>1-16</td>
<td>IBM</td>
<td>130</td>
<td>no.</td>
</tr>
<tr>
<td>PSEC4</td>
<td>no.</td>
<td>6</td>
<td>256</td>
<td>1-16</td>
<td>IBM</td>
<td>130</td>
<td>no.</td>
</tr>
</tbody>
</table>

成功的PSEC3: 现实概念的证明，朝着更小的特征尺寸迈进。

- 下一个DRS计划使用110nm；下一个SAM计划使用180nm。
Future Prospects

• Expect many other designs in future
  – Barriers to entry are low
  – Many different reference designs out there

• Challenges (R&D continues):
  – Fine timing (~ 1ps)
  – Larger dynamic range
  – Deeper (continuous) sampling
  – Faster, sparsified readout
  – Calibration

• Key enabling technology
  – Large telescope arrays (CTA)
  – > 100km$^3$ neutrino detectors
  – PID, Fast x-ray detectors
Back-up slides
Underlying Technology

- **Track and Hold (T/H)**

- **Pipelined storage = array of T/H elements, with output buffering**

\[
\text{Bus } V_{\text{out}} = \frac{A}{1+A} \times \frac{Q}{C_s}
\]

\[
v_1 = V, \quad Q = C_s \cdot v_1
\]

\[
\text{Return Bus}
\]

\[
\text{Top Read Bus}
\]

\[
\text{Bottom Read BUS}
\]

\[
\text{N caps}
\]
Real MCP-PMT Signals (with BLAB2)

Residual Time Walk

Rather robust for amplitude invariant signals,
TOF still hard, but can shape extract
Simulated Performance vs. SNR

Time Difference Dependence on Signal-Noise Ratio (SNR)

\[ \sqrt{kTZ\Delta \nu} \]

- Signal Noise Ratio
- Time Difference Resolution [ps]
- Voltage (mV)
- Time (ns)

300MHz ABW, 5.9GSa/s
- Input bandwidth depends on 2x terms
  - \( f_{3dB[\text{input}]} = \left[2\pi Z C_{tot}\right]^{-1} \)
  - \( f_{3dB[\text{storage}]} = \left[2\pi R_{on} C_{store}\right]^{-1} \)
Wilkinson Clock Generation

IRS Wilk PRO Strb (IRS_WilkPRO)
Wilkinson Recording

Start = start 0.5-1.5GHz Clock

Ripple counter (run as fast as can)
Triggering

IRS Trigger 1 (IRS_trig1)

4.38um x 3.84um = 16um^2
~100fF

- Need 9th channel for monitoring

\[ \text{dQ} = \text{CdV} = (100fF)(1.5V) \]
\[ \text{dt} \approx 5\mu s \]
\[ I = \frac{\text{dQ}}{\text{dt}} = \frac{(150fC)}{(50\mu s)} \approx 30\mu A \]
Triggering – same as previous results

- Monitor 9th channel (uses Ch.1 threshold) to compensate for temperature dependence
Hit Processing numbers

Assume:
100kHz charged track hits on each bar

~32 p.e./track (1% of 100ns windows)
30kHz trigger rate
Each PMT pair sees <8> hits
240k hits/s
Each BLAB3 has an average occupancy
<1 hit (assume 1)
400ns to convert 256 samples
16ns/sample to transfer
At least 16 deep buffering
(Markov overflow probability est. < 10^{-38})

Each hit = 64samples * 8bits = 512bits
⇒~125Mbits/s
(link is 3.0 Gb/s ~ x30 margin)

Plan to model in standard queuing simulator, but looks like no problem
(CF have done same exercise with Jerry Va’vra for 150kHz L1 of SuperB and can handle rate)
Front-end Electronics studies

1GHz analog bandwidth, 5GSa/s

Simulation includes detector response

G. Varner and L. Ruckman

J-F Genat, G. Varner, F. Tang, H. Frisch
Ice Radio Sampler (IRS)

RF input coupling (S11)
Ice Radio Sampler (IRS)

P. Gorham -- measurement
WFS Evolution and Philosophy

- **SAM**
  1. Maximize dynamic range and minimize signal distortion.
  3. Minimize costs (both for development & production)

- **DRS family**
  - Get a solid, general design working
  - Something that can work, in volume, for many apps

- **LAB and siblings (6→8 generations)**
  - Continue to explore parameter space
  - Concentrate on applications where more general solutions above many not be best choice

Approaches very complementary
References

• PSI activities (DRS)
  – IEEE/NSS 2008, TIPP09
  – http://midas.psi.ch/drs

• DAPNIA activities

• Hawaii activities
  – STURM: EPAC08-TUOCM02, June, 2008.