TOP DAQ integration status
timeout / deadbeef

- created a set of testbenches to narrow down causes
- timeout occurs in 3 situations:
  - 1) writing to / reading from particular fee32 registers in a particular sequence, even if from just a single thread
  - 2) using reghs(x) to write to a carrier that is not yet programmed (or not present)
  - 3) using reghs(x) to write to an hslb that does not have a link up to a boardstack
- *none* of these are what we had suspected all along: that it occurred when we were streaming fifo data out via readhs while talking to the copper local bus via reghs(x)
- situations 2 and 3 are not likely to occur during normal Belle II operations
- have a workaround (for situation 1) in our svn (bitfiles b1000029 / e0000029) that simply generates a timeout and if the state machine gets stuck (as it does in situation 1)
  - it will recover and not require a reprogramming cycle
- so we should be able to use the regular b2daq machinery
Zynq programming

• for PS/ARM, we only need 3 functions in xmd (after connecting):
  - "dow" (download elf)
  - "con" (continue program)
  - ps7_init/ps7_post_config, which are a series of "mask_write" commands
    • each "mask_write" is a combination of mrd (memory read), modify, mwr (memory write)
    • may be possible to avoid this step entirely in exchange for a second set of "dow"/"con" commands by writing a custom "first-stage bootloader" that just does what we need