production front-end electronics

bPIDs/TOP front-end boardstack schematic diagram

2-stage amp \( (x8) \)

ASIC 0

ASIC 1

ASIC 2

ASIC 3

Zynq '030 SoC

Zynq '045 SoC

LVDS fanout

timing trigger

SFP+ data

JTAG

SFP+ trigger

mechanical mockup for production boardstack
SCROD revB

bPID/TOP front-end boardstack schematic diagram

Zynq '030 SoC

ASIC 0 (x8) ASIC 1 (x8) ASIC 2 (x8) ASIC 3 (x8)

carrier revE (x4)

LVDS fanout
timing trigger
SFP+ data
JTAG
SFP+ trigger

Zynq '045 SoC

in addition, on the board, there are:
- 14 voltage regulators
- voltage and current monitoring for all regulators
- power supply sequencing logic
- calibration signal input, amplification and fanout
- breadboard area
- automatic fallover wiring to close JTAG chain
- humidity sensor (I2C)
- temperature sensor (I2C)
- EEPROM (I2C)

LPC FMC
100 pin connector
2GiB LPDDR2 RAM
128MiB QSPI flash
USB ULPI
LVDS fanout
100 pin connector
SFP+ data
JTAG
OSC
14 pin JTAG
timing trigger

2014-06-19
TOP electronics session @ B2GM18

M. Andrew
• 95% of connections routed

• goal is to submit for fab by the end of this week
carrier revE

bP1D/TOP front-end boardstack schematic diagram

2-stage amp (x8) 2-stage amp (x8) 2-stage amp (x8) 2-stage amp (x8)

ASIC 0  ASIC 1  ASIC 2  ASIC 3

Zynq '030 SoC

2-stage amp 2-stage amp 2-stage amp 2-stage amp

ASIC 0  ASIC 1  ASIC 2  ASIC 3

100 pin connector

2GIB LPDDR2 RAM

in addition, on the board, there are:
11 voltage regulators
voltage and current monitoring for all regulators
power supply sequencing logic
calibration signal amplification and fanout
automatic fallover wiring to close JTAG chain
temperature sensor (i2c)
EEPROM (i2c)

Zynq '045 SoC

timing

LVDS fanout

SFP+ data

JTAG

SFP+ trigger

carrier revE detail

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carrier revE

- will draw elements from two existing designs:
  - SCROD revB (but with a smaller FPGA package)
  - carrier revD (but with a different ASIC, and a two-stage amplifier)
- should take approximately one month to complete the PCB design
### IRS-based iTOP Readout

#### Pre-Production Prototype Board Stack

<table>
<thead>
<tr>
<th>Component</th>
<th>6/16</th>
<th>6/23</th>
<th>6/30</th>
<th>7/7</th>
<th>7/14</th>
<th>7/21</th>
<th>7/28</th>
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<td>Evaluation</td>
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<td>Fab/Assy</td>
<td>Ready</td>
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<td>Design</td>
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<tr>
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#### Production Board Stack: Schedule to Completion

- **Travel & Other Schedules**
  - Ready for integration with electronics
  - Fabrication
  - Assembly

- **Electronics Modules**
  - Stand-alone verification
    - Integration with QBB
    - Verification on CRT slot 0
    - Verification on CRT slot 1
    - Verification on CRT slot 2
    - Verification on CRT slot 3

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