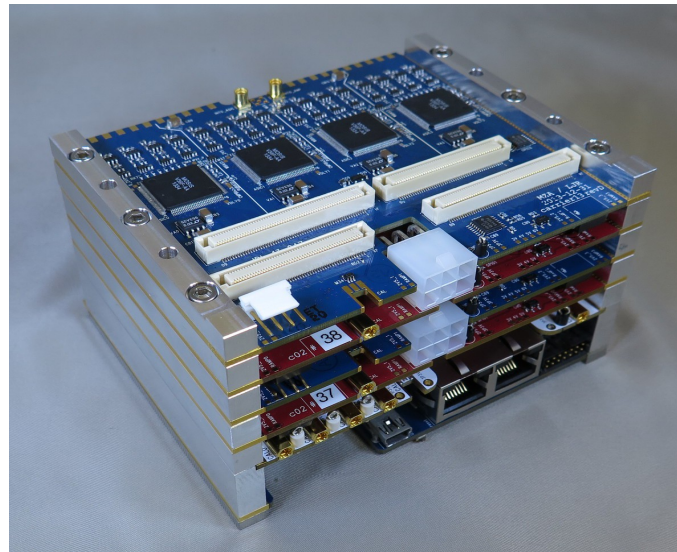


128 channel waveform sampling digitizer/readout in the TOP counter for the Belle II upgrade

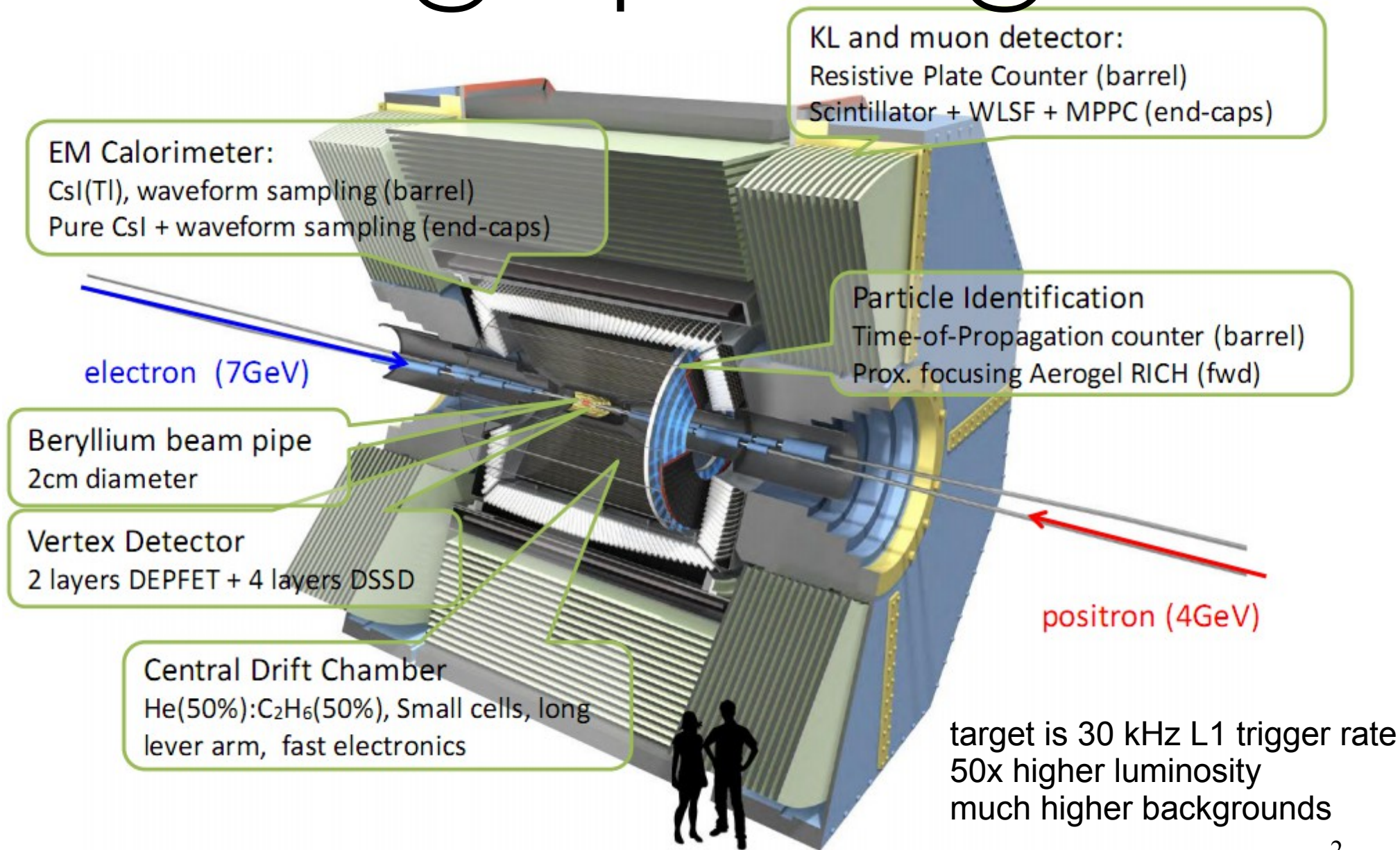
University of Hawai`i
SLAC
Indiana University
Nagoya University
PNNL
University of South Carolina
University of Pittsburgh
KEK



on behalf of:
the Belle II bPID/TOP group

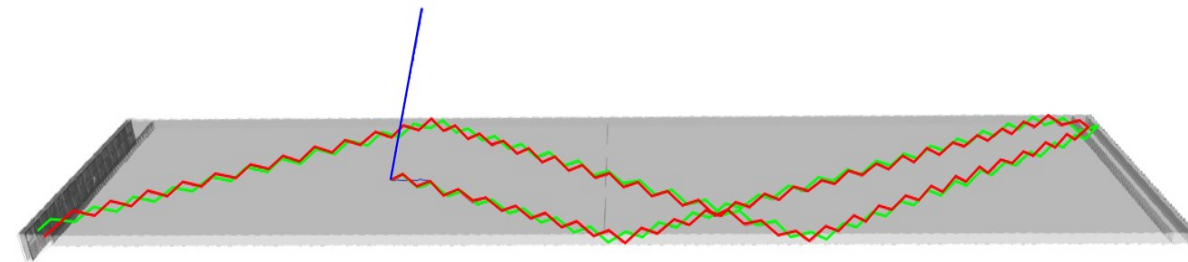


Belle II @ SuperKEKb @ KEK

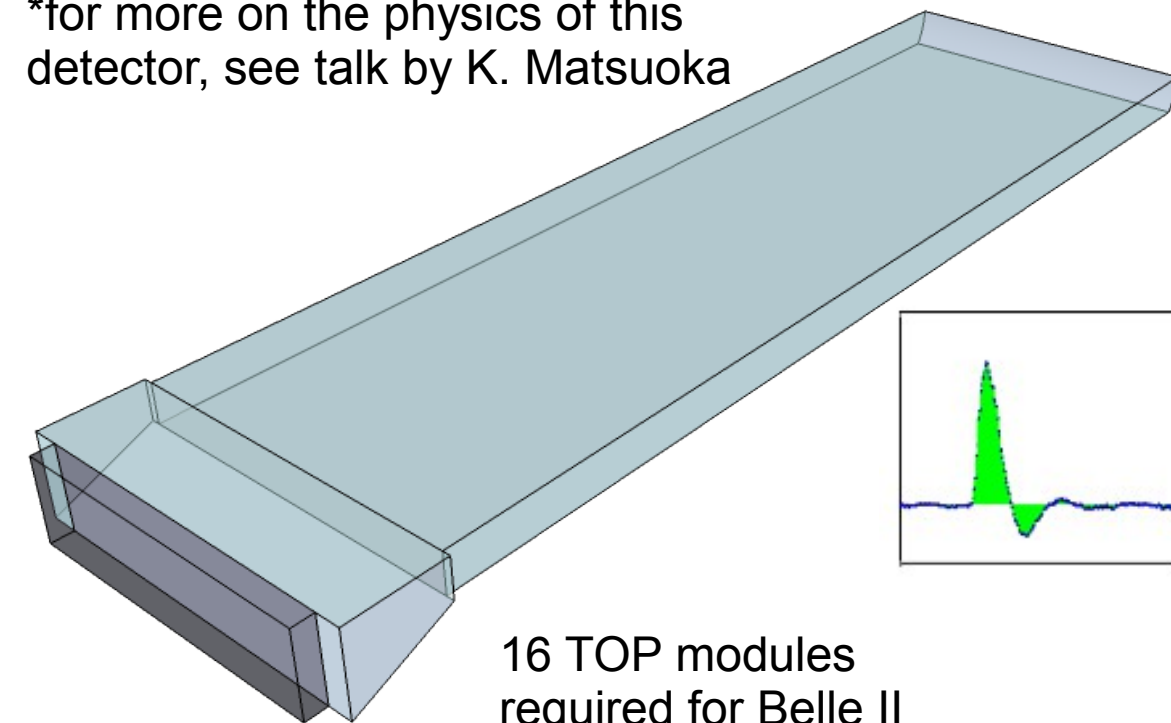


Time-Of-Propagation (TOP) counter: Cherenkov PID based on PDFs

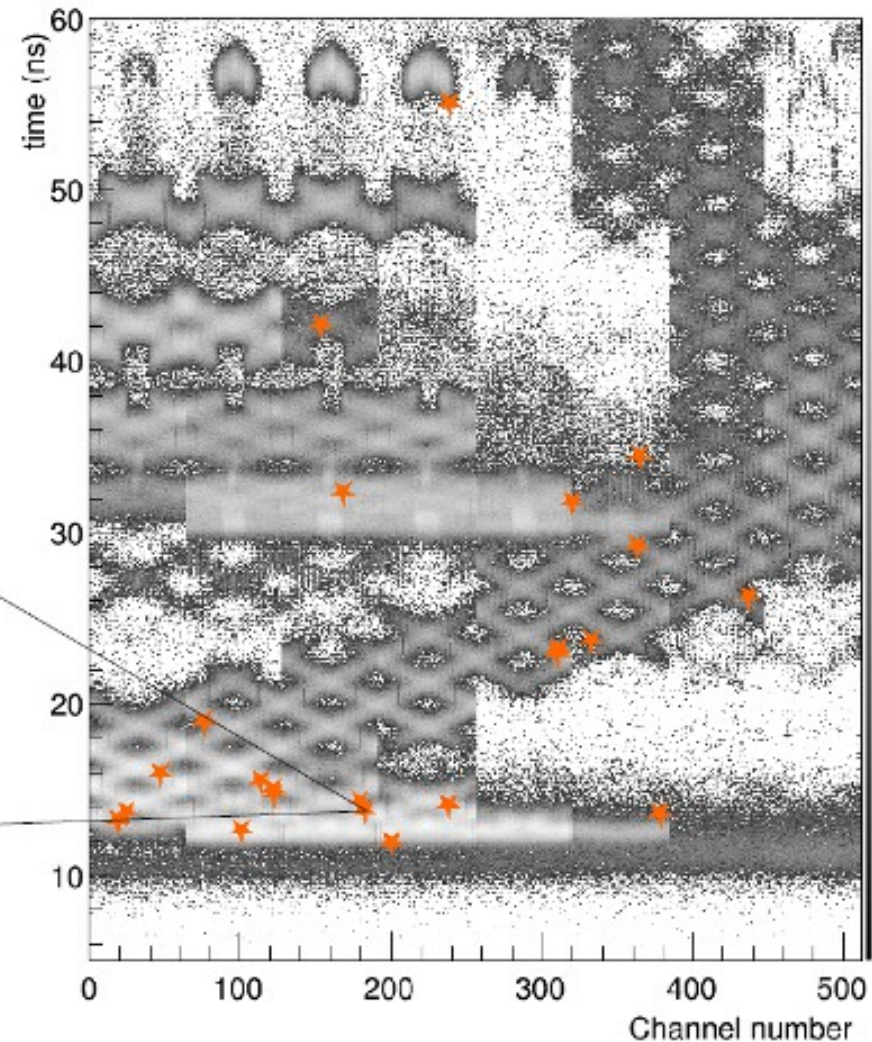
Beamtest Experiment 2 Run 568 Event 1



*for more on the physics of this detector, see talk by K. Matsuoka



16 TOP modules
required for Belle II



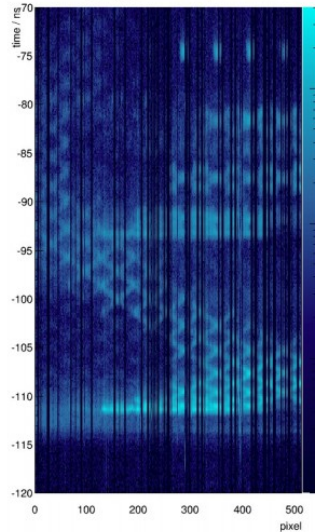
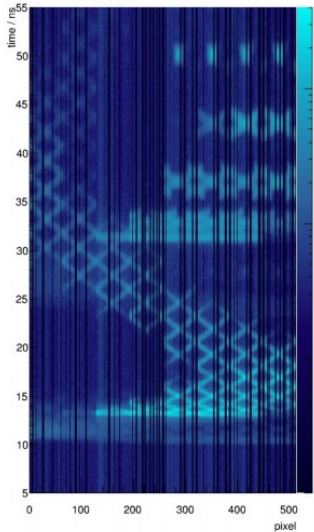
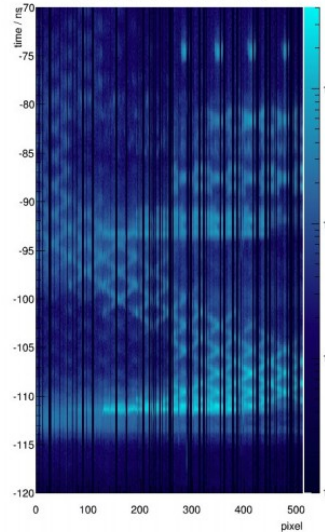
folded ring images from SPring-8 / LEPS

Data ring image for $\cos\theta = 0.00$

Simulated ring image for $\cos\theta = 0.00$

Data ring image (with LEPS TOF cut) for $\cos\theta = 0.00$

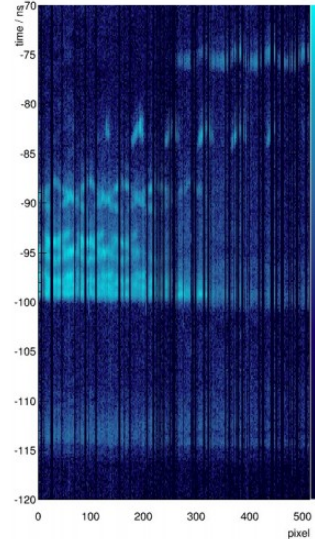
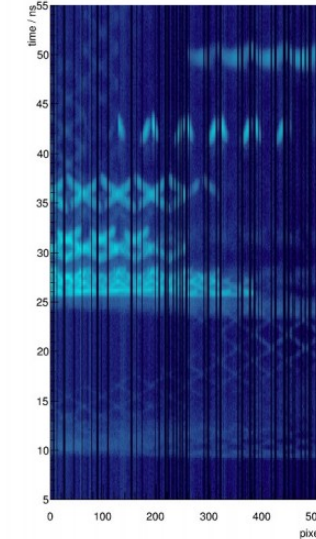
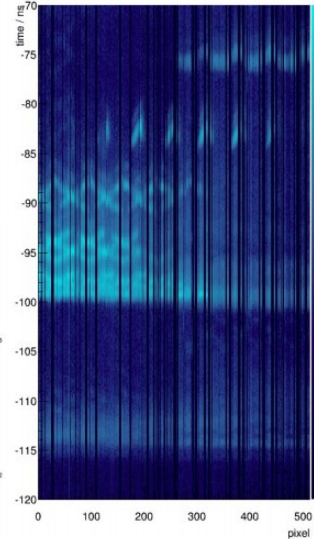
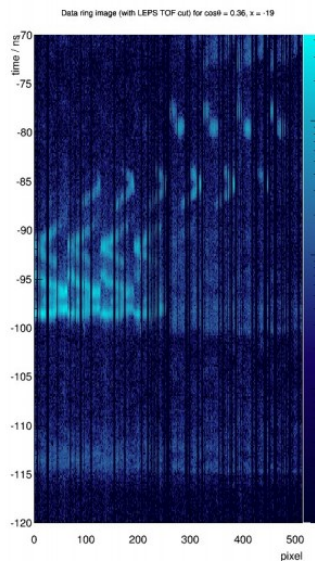
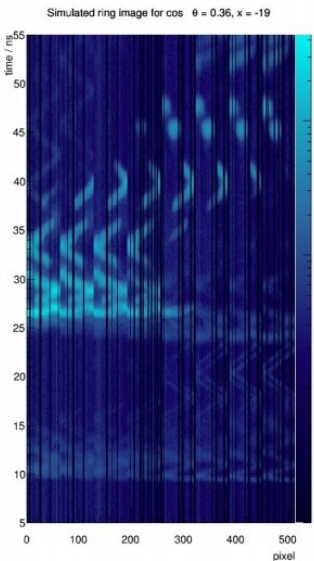
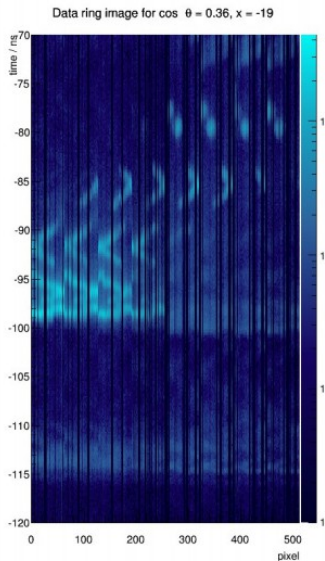
data from previous prototype:
IRS3B ASIC
low gain from single-stage discrete amplifier
timing resolution ~ 95 ps
80% efficient



Data ring image for $\cos\theta = 0.43$

Simulated ring image for $\cos\theta = 0.43$

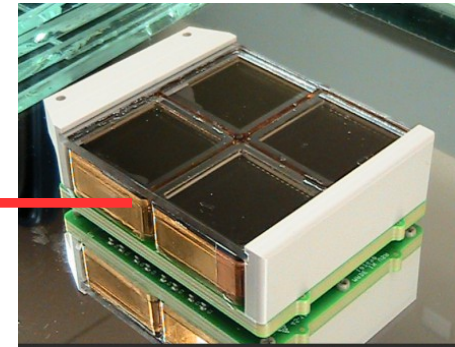
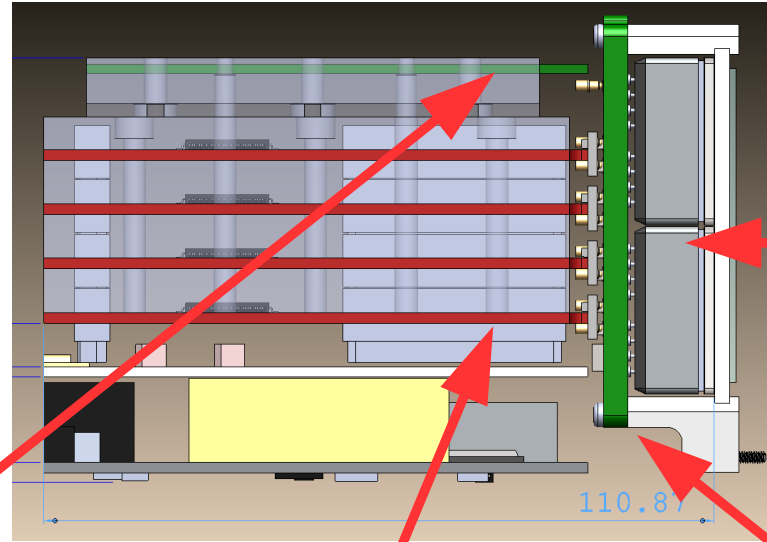
Data ring image (with LEPS TOF cut) for $\cos\theta = 0.43$



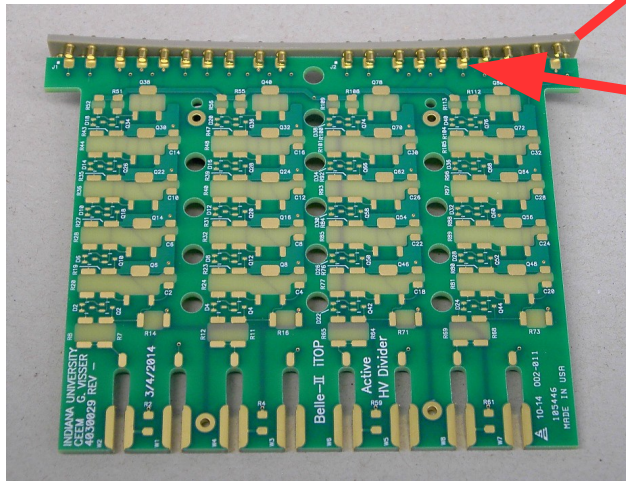
vertical bands are due to
dead channels (90/512)

current prototype front-end electronics

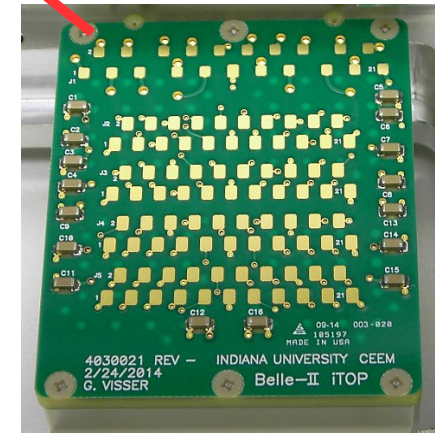
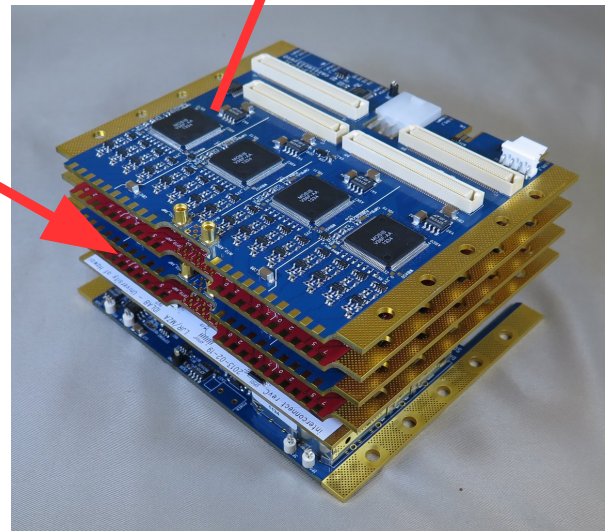
- IRS3C ASIC
- higher gain from single-stage discrete amplifiers
- nearly same form-factor as production boardstack
 - includes pogo pin PMT interface



*for more on MCP-PMTs, see talk by T. Yonekura

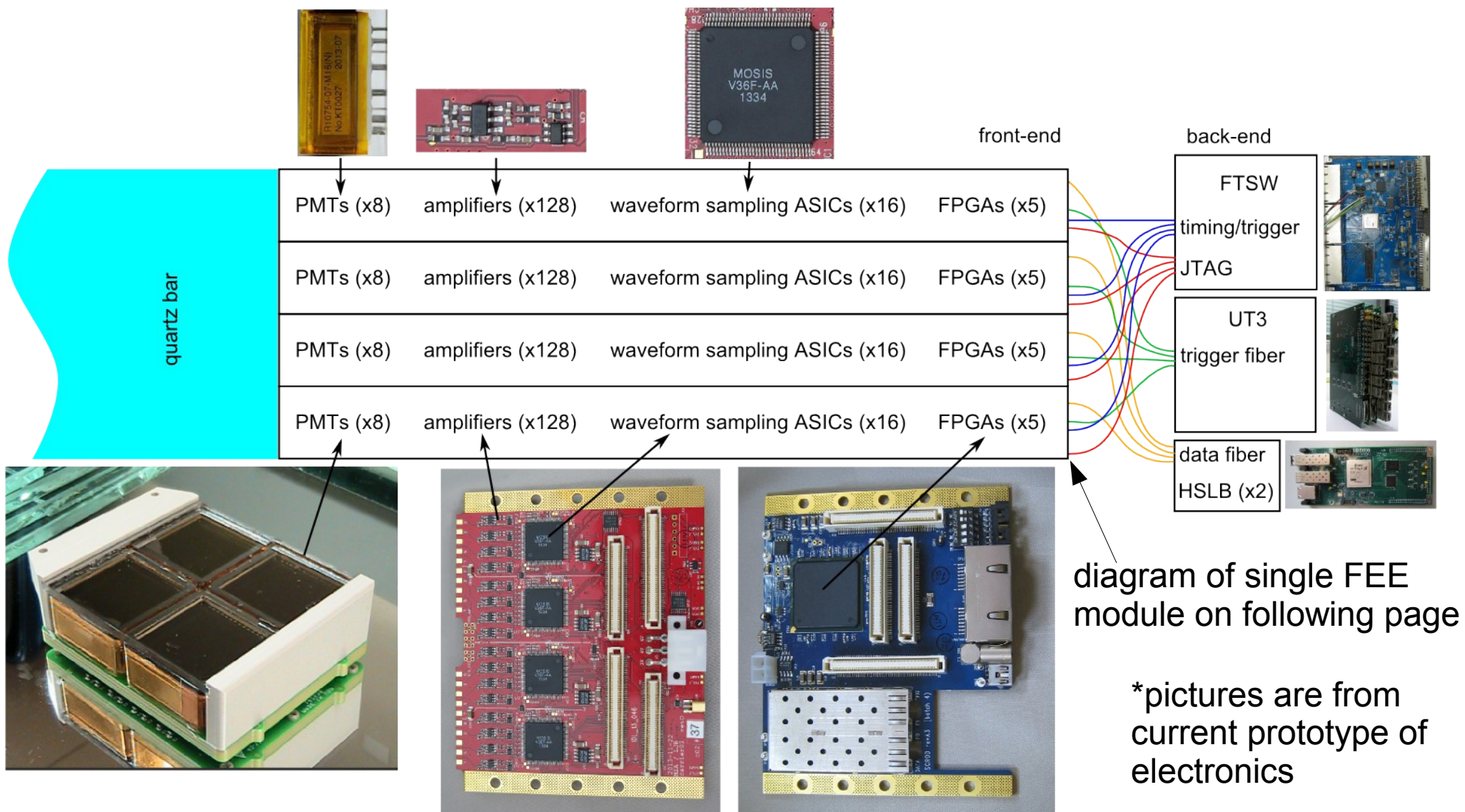


spring-loaded "pogo" pins



pogo pin landing pads

FEE+DAQ for production TOP module



calibration steps

(to aid online feature extraction and zero-suppression)

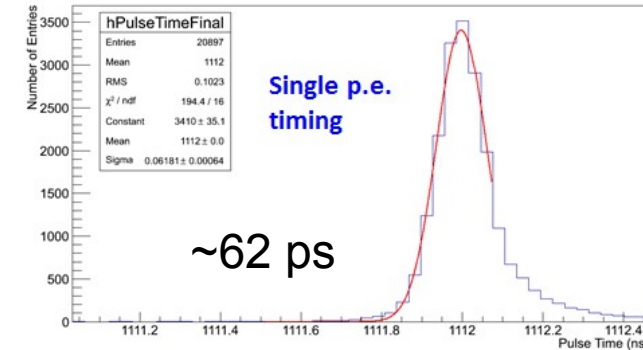
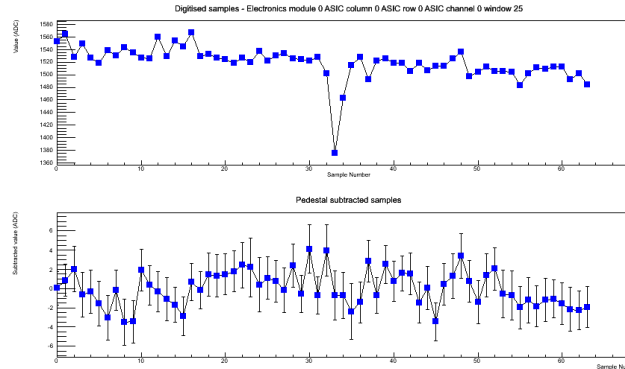
1. Subtract storage cell pedestal
2. Linearity correction
3. Individual sample time offset correction

*these data are from IRS3B with higher gain from single-stage discrete amplifier with 96% efficiency

Three sets of calibration constants required:

- **Sample pedestal values**
 - (262144 samples/ASIC)
- **Sample time widths**
 - (128 values per ASIC)
- **Timewalk correction**
 - (~20 values per ASIC)

after calibration:



Pulse Time Vs Sample Array Bin #
(used to measure Sample-DTs)

Pulse Time Vs Height
(timewalk correction)

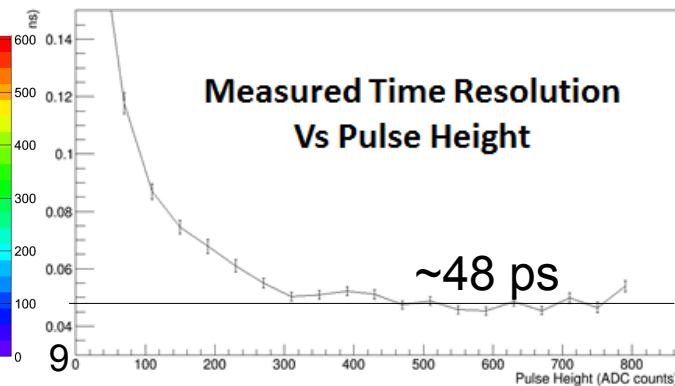
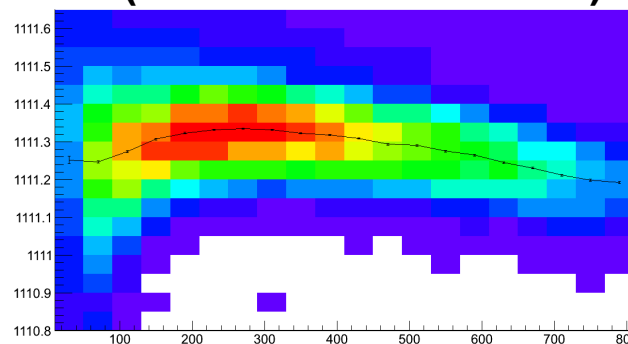
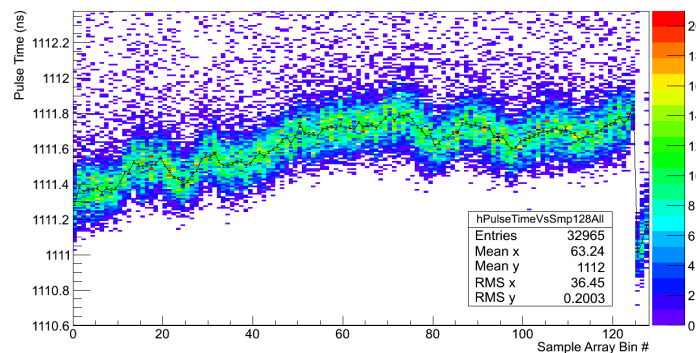
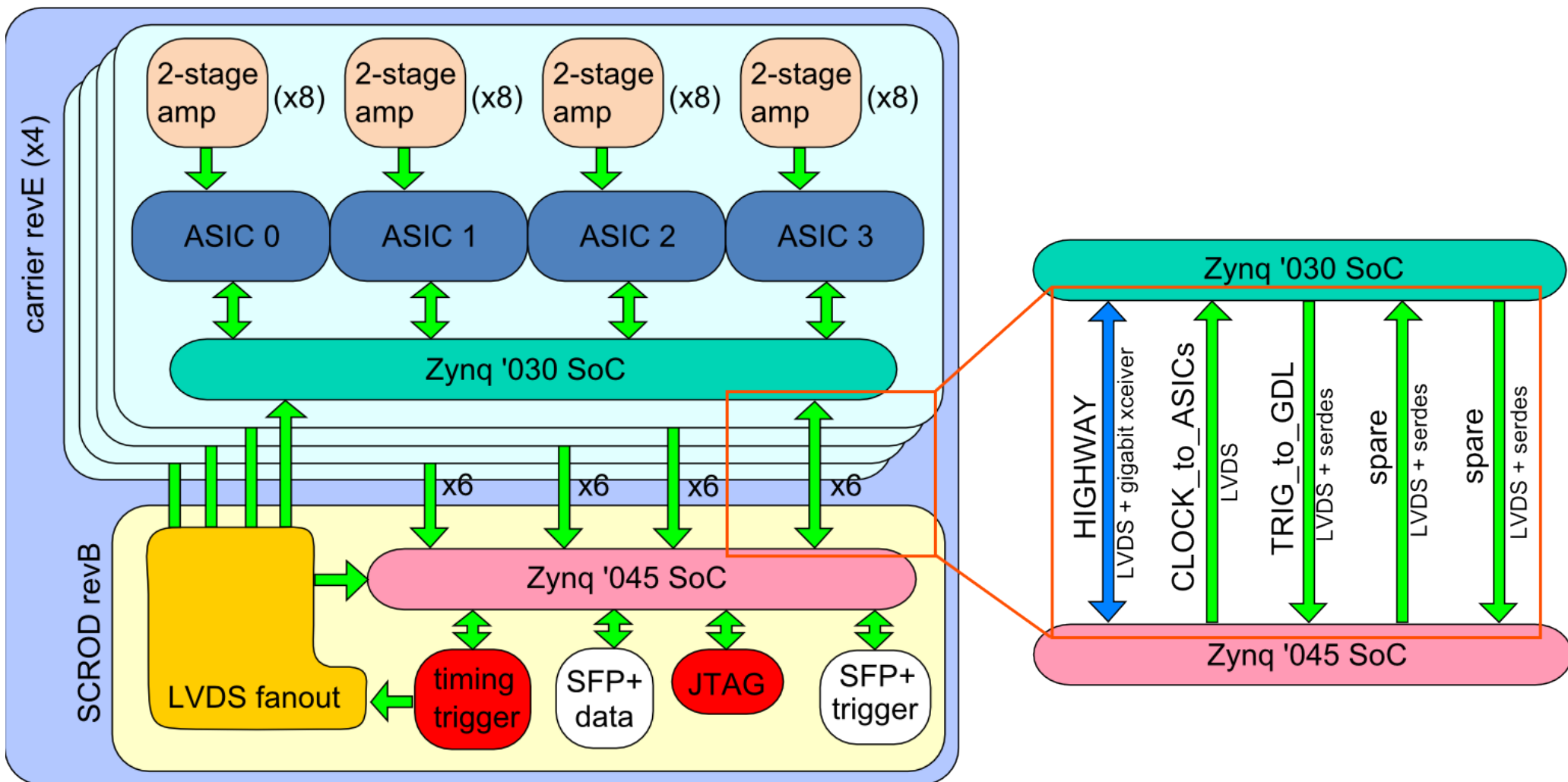


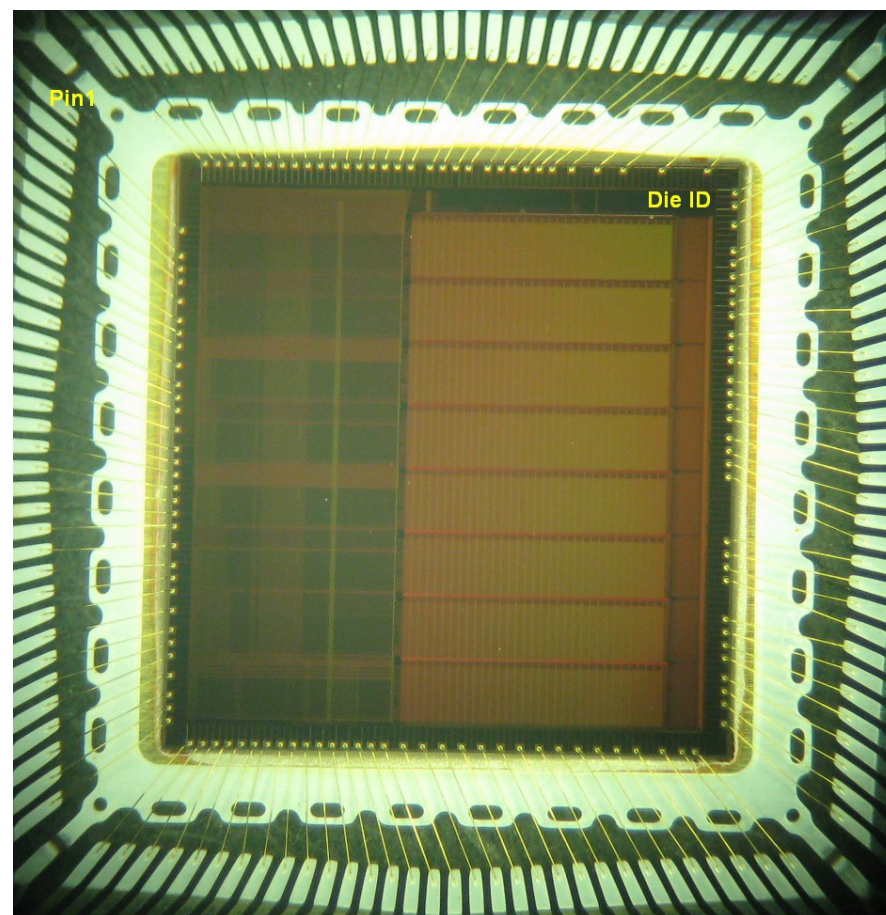
diagram of production front-end

bPID/TOP front-end boardstack schematic diagram

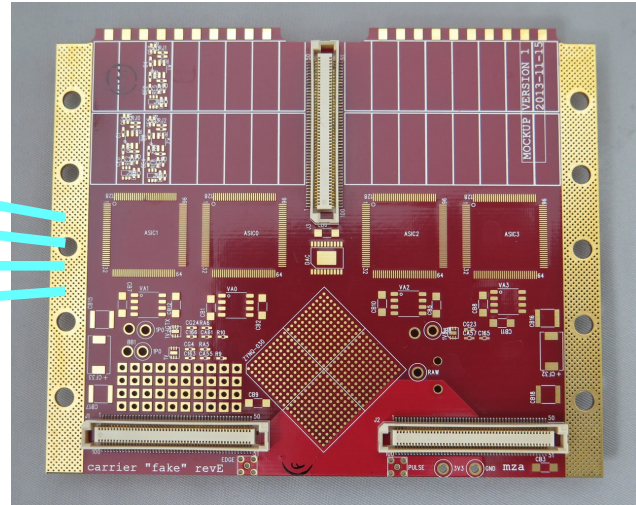
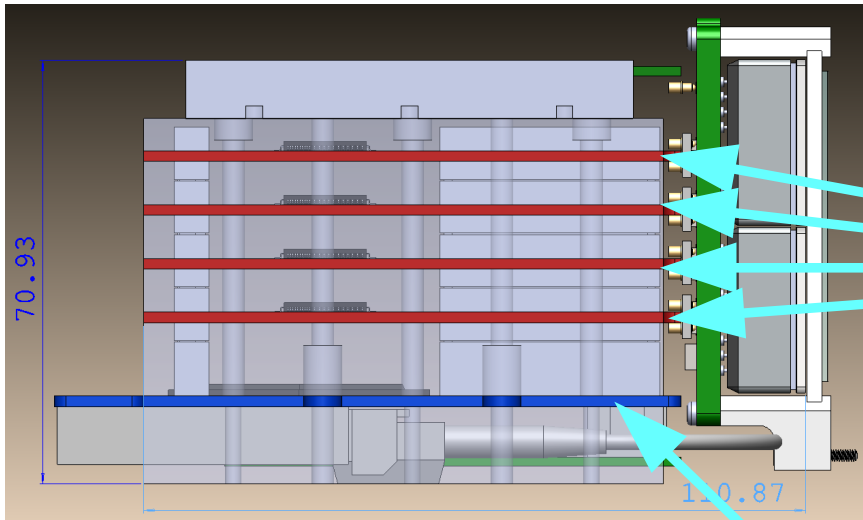


production ASIC (IRSX)

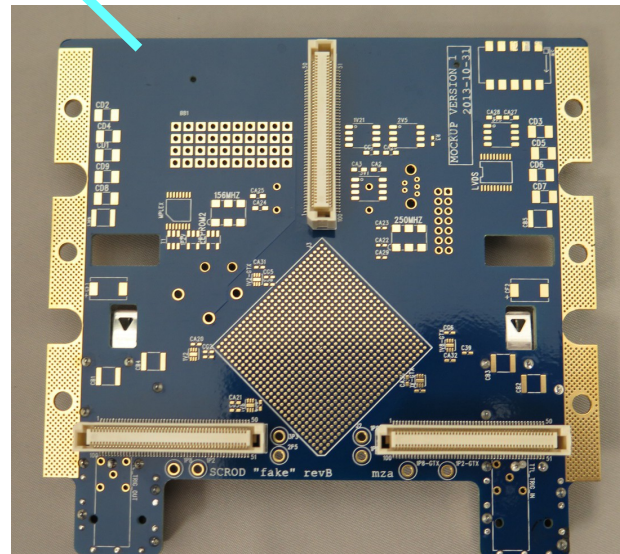
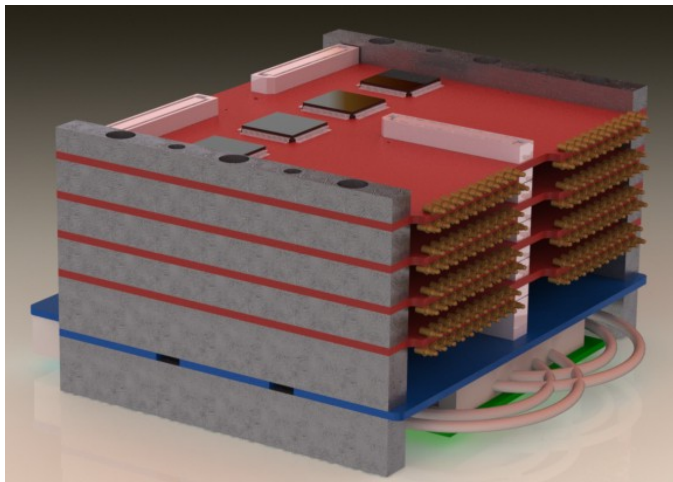
- 8 channels
- 128-sample Switched-Capacitor Array (SCA)
 - up to 4 GSa/s
- trimDAC for each sample in timing generator
 - to remove nonlinearities from time base
- 2-stage (analog) transfer to deep storage array (32,768 samples deep)
 - in principle allows deadtimeless readout
- trigger bit output
 - sent to global decision logic for Belle II
- 12-bit Wilkinson conversion of 8*64 samples
- serial readout over LVDS pair
- TSMC 0.25 um via MOSIS engineering run
- packaged in TQFP-128A



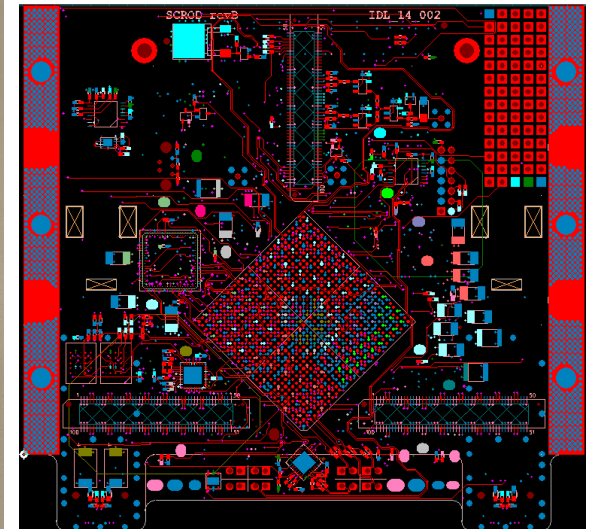
production “boardstack” design



carrier (mockup)



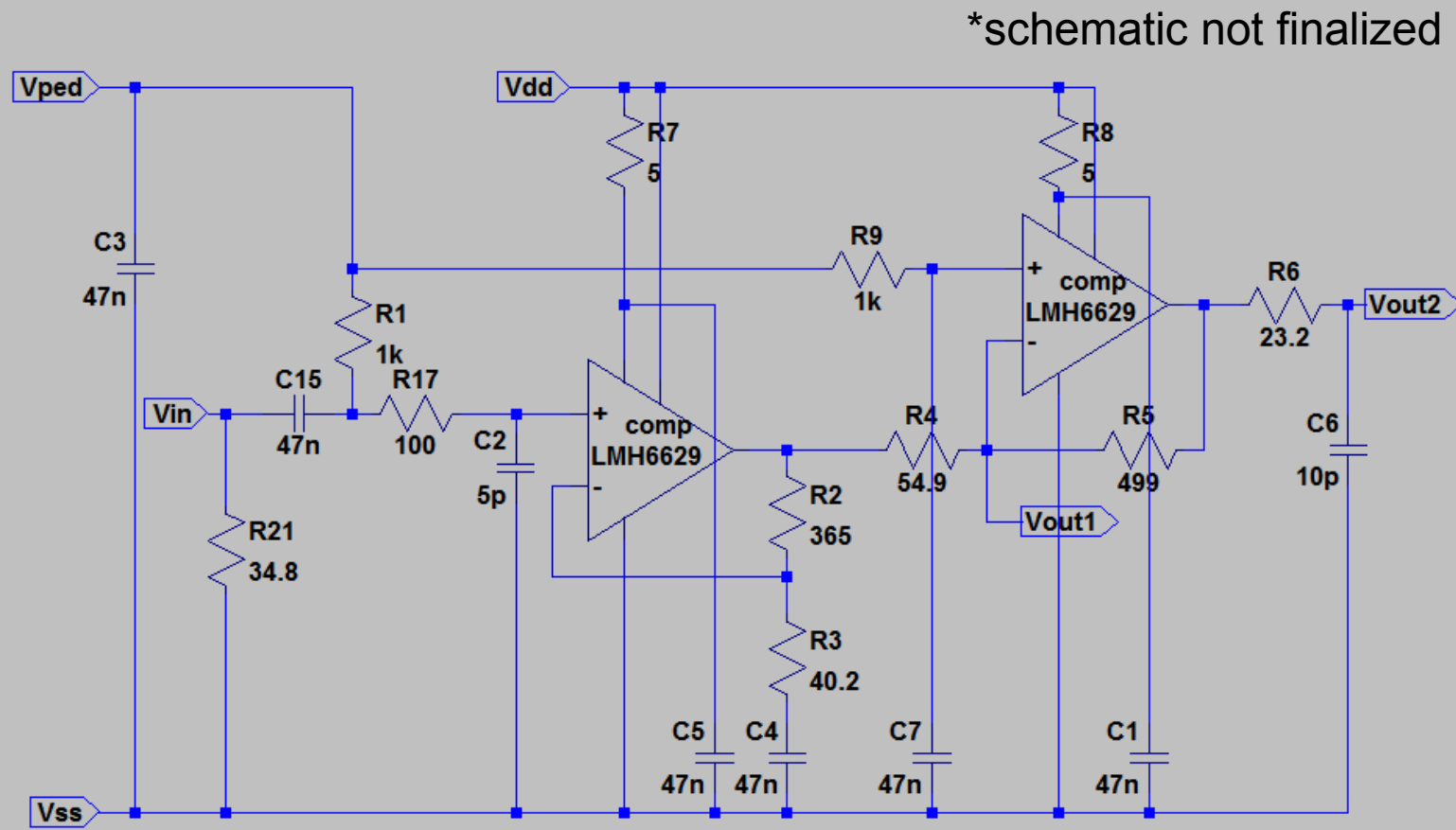
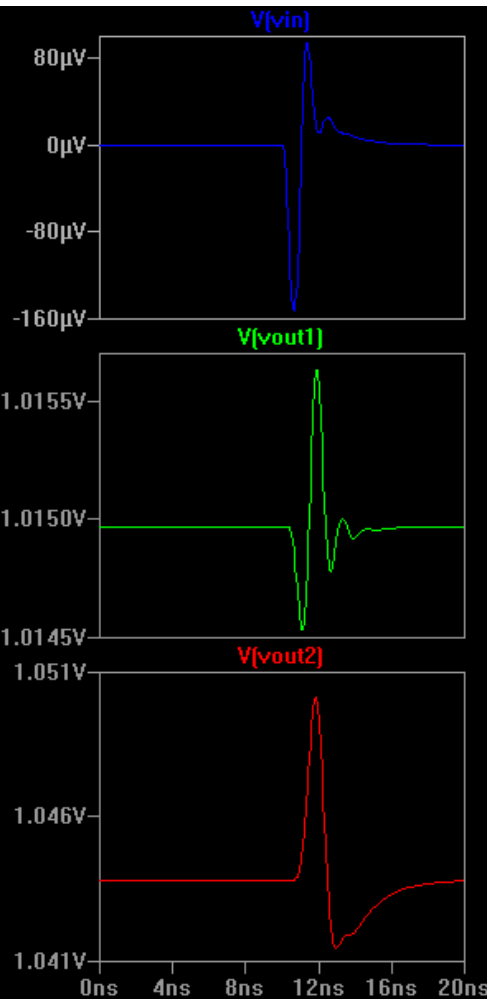
SCROD (mockup)



SCROD revB

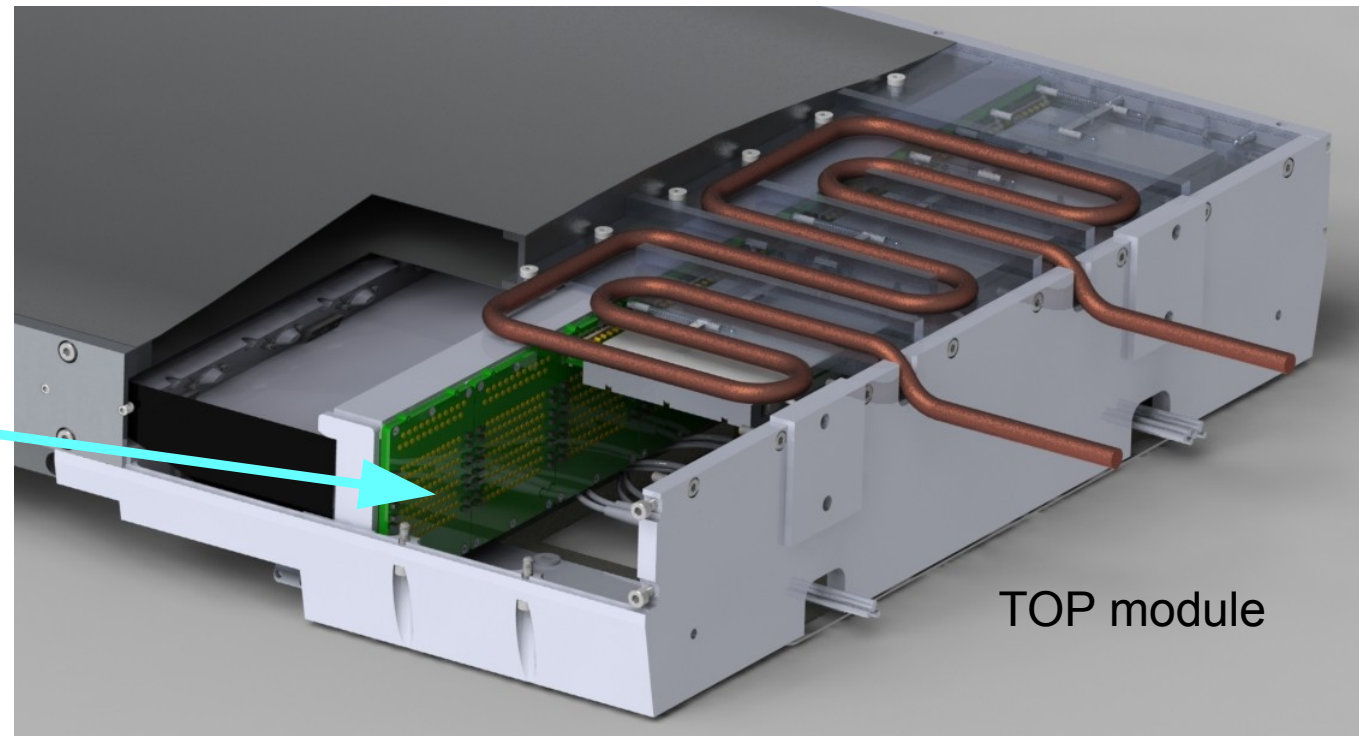
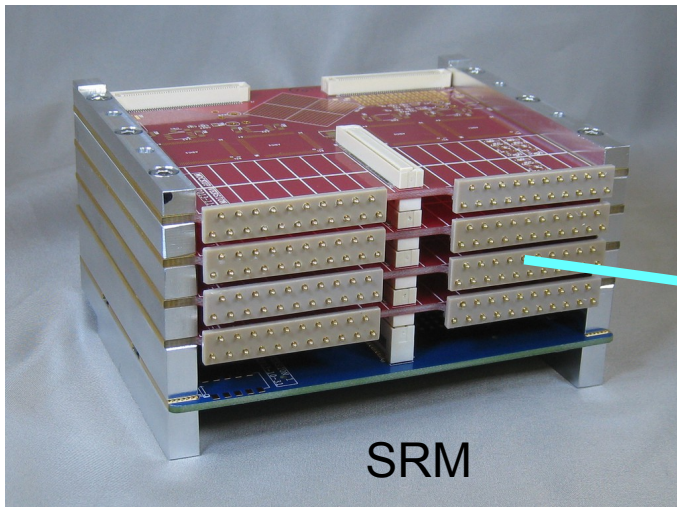
two-stage amplifier

- needed to run MCP-PMTs at 5×10^5 gain



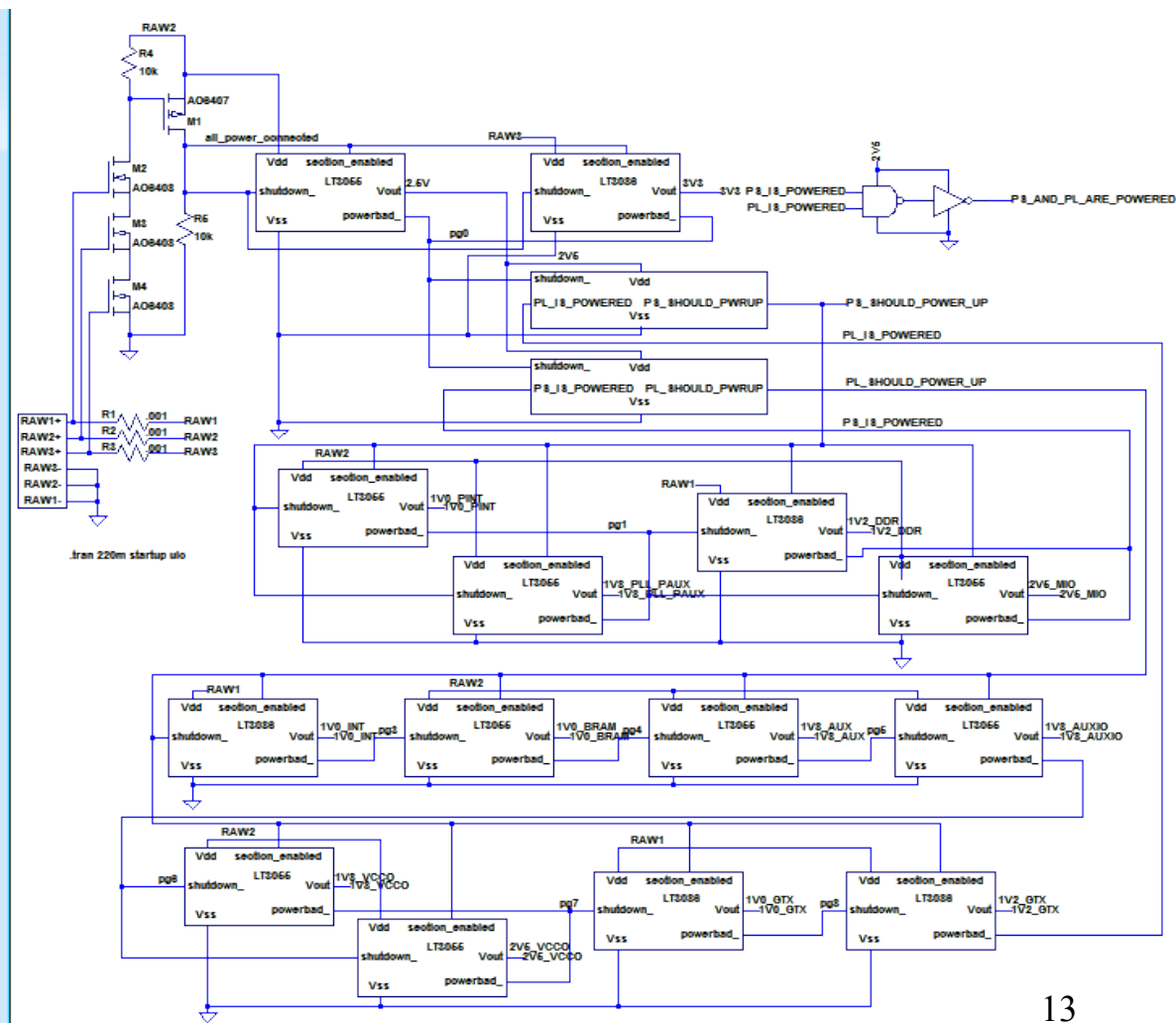
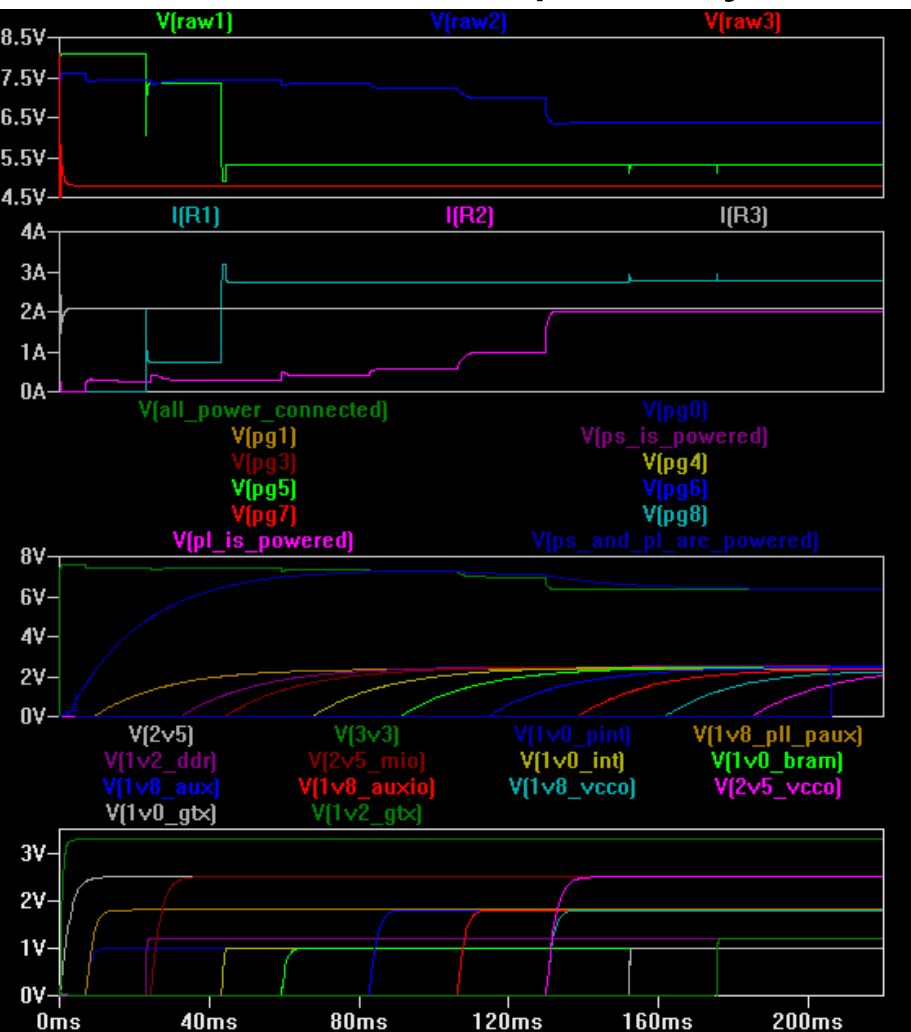
power draw / cooling

- expected power draw for each production SRM: 50-78 W
- 200-312 W per TOP module



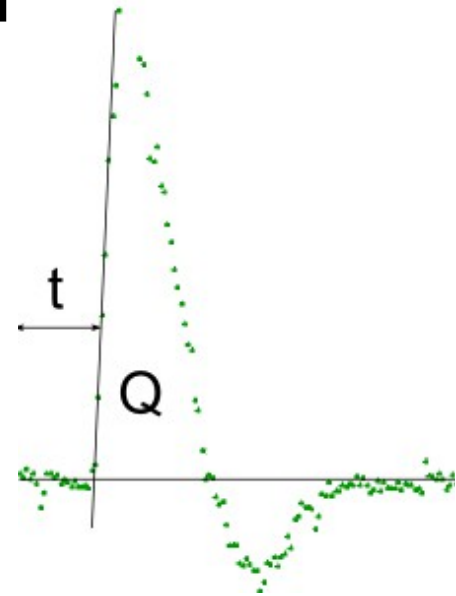
power-supply sequencing

- 10 stages (per board; daisy-chained up boardstack)
 - reduces peak system inrush current



outstanding issues

- service space is extremely constrained
 - LV, HV, fiber optics, timing/trigger, JTAG links
 - cooling pipes
- must extract Q , t from waveforms in FPGA in real time to be sent to downstream DAQ system
 - processing done by dual ARM cores on each FPGA (with help from programmable logic)
 - need to get data down from ~ 100 bytes per hit to ~ 10 bytes per hit



status / plans

- took previous prototype electronics to beam test at SPring-8/LEPS (~95 ps; 80% efficient)
- continue to evaluate electronics in bench tests (~62 ps; 96% efficient)
- working on production board designs now:
 - will evaluate next few months thereafter
 - will go into production near end of this Summer
- cosmic-ray test for each TOP module this Fall
- installation into detector to commence next year