bPID / TOP front-end electronics

University of Hawaii:
• Brian Kirby
• Gary Varner
• Matt Andrew
• James Bynes
• Boštjan Maček
• Matt Barrett

PNNL:
• Lynn Wood
• Eric Choi
• Hardeep Mehta
• Ryan Conrad

SLAC:
• Kurtis Nishimura

Indiana University:
• Gerard Visser

University of Pittsburgh:
• Vladimir Savinov
• Istvan Danko
bPID / TOP front-end electronics: Outline

- the past
- the present
- the future
bPID / TOP front-end electronics: SPring-8 / LEPS beam test

**Table:**

<table>
<thead>
<tr>
<th>iTOP configuration</th>
<th># events (IRS)</th>
<th># events (CFD)</th>
<th>LEPS fill pattern</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal incidence</td>
<td>540k</td>
<td>250k</td>
<td>A-mode/H-mode</td>
</tr>
<tr>
<td>Normal incidence (highest rate poss.)</td>
<td>70k</td>
<td></td>
<td>A-mode</td>
</tr>
<tr>
<td>Forward (cosθ~0.4)</td>
<td>400k</td>
<td>950k</td>
<td>D-mode/H-mode</td>
</tr>
<tr>
<td>Forward (cosθ~0.4) + x shift (20cm)</td>
<td>235k</td>
<td>700k</td>
<td>D-mode/A-mode</td>
</tr>
</tbody>
</table>

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bPID / TOP front-end electronics: DAQ at SPring-8 / LEPS
bPID / TOP front-end electronics: PID based on PDFs
bPID / TOP front-end electronics: Ring images from SPring-8 / LEPS

vertical bands are due to dead channels (90/512)
bPID / TOP front-end electronics: FTSW-trigger/JTAG PCB

- provides a path for trigger and JTAG
- plugs directly into existing headers on FTSW (with minor soldering required to replace S4 with headers)
- which front-end module(s) is/are connected to JTAG selectable with front-panel rotary switch
- trigger maintains 50 Ohm path from LEMO cable, then uses high-speed comparator with LVPECL output to LVPECL/LVDS converter, fed directly into FTSW trigger input (special bPID firmware; but no other firmware modifications required)
bPID / TOP front-end electronics: Outline

- the past
- the present
- the future
bPID / TOP front-end electronics:
Boardstack / PMT testing in Hawaii

- Picosecond laser
- Inside Dark Box
- Module under test w/ reference SL-10 MCP
- FTSW, COPPER, CAMAC
- Stage for x-y control of illumination fiber (picosecond laser)
bPID / TOP front-end electronics: Intermediate boardstack

- for near-term testing
- uses IRS3C ASIC
- same form-factor as final boardstack*
  - *=except for presence of interconnect board and size of spacers between interconnect and SCROD

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bPID / TOP front-end electronics: Outline

- the past
- the present
- the future
bPID / TOP front-end electronics: final boardstack design
bPID / TOP front-end electronics: FEE+DAQ diagram for single bar

- PMTs (x8)
- amplifiers (x128)
- waveform sampling ASICs (x16)
- FPGAs (x5)

Front-end

- PMTs (x8)
- amplifiers (x128)
- waveform sampling ASICs (x16)
- FPGAs (x5)

Back-end
- FTSW
- timing/trigger
- JTAG
- UT3
- trigger fiber
- data fiber
- HSLB (x2)

Diagram of single FEE module on next page
bPID / TOP front-end electronics: Final boardstack diagram

bPID/TOP front-end boardstack schematic diagram
bPID / TOP front-end electronics: Pseudo-boardstack

- **pseudo-carrier (FMC HPC)**
  - ASIC
  - FPGA ZYNQ '030
  - 4 x GTX 14 LVDS
- **FMC HPC**
- **pseudo-SCROD (FMC LPC)**
  - ZC706 (Zynq '045)

- Fiber link for data (to HSLB)
- Fiber link for trigger (to UT3)
- Timing/trigger and JTAG links (to FTSW)
bPID / TOP front-end electronics: DAQ-based feedback loop

controlling of VadjN value implemented as a feedback through recorded files

after each file is recorded, pulse processing calculates new running parameters

current algorithm works on:

- distribution of pulses that cross the 'window' border
- distribution of pulses that do not cross the 'window' border

principle that these two distributions should have the same mean, and they have opposite gradients w.r.t. running parameter → from difference of mean values

a new VadjN is predicted (calibration run is needed to estimate gradients)

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bPID / TOP front-end electronics: Calibration steps

1. Subtract storage cell pedestal (avg. ~2000 ADC +/- 100’s counts)
2. Linearity correction (optional)
3. Individual sample time offset correction

Three sets of calibration constants required:

- **Sample pedestal values**
  - (262144 samples/ASIC)

- **Sample time widths**
  - (128 values per ASIC)

- **Timewalk correction**
  - (~20 values per ASIC)

**Waveform Pedestal Correction**

**Pulse Time Vs Sample Array Bin #**
(used to measure Sample-DTs)

**Pulse Time Vs Height**
(timewalk correction)
bPID / TOP front-end electronics: Proposed in-detector processing steps
bPID / TOP front-end electronics: Status

- will have intermediate boardstack as soon as HV board is fabbed and assembled
- bench-testing DAQ is either through:
  - USB, or
  - fiber+DSP_FIN+COPPER-II+Radisys+copper server
- final boardstack is still in design stage
  - goal is to have this done by the end of March
- need to incorporate trigger output into the firmware for ASIC control/readout
bPID / TOP front-end electronics: Questions (1/2)

- What FTSW revision will TOP get? (need to know wiring for trigger/timing and JTAG)  
  [answer=all FTSWs for production will have the same JTAG wiring; same for FTSW 2.0 as FTSW 3.1 (which is different from the FTSW 2.1 that we already have)]

- What FTSW will sci-KLM get?  [see above answer]

- What will provide the TOP FTSWs with the program to stream over JTAG to the TOP modules? (there is no VME crate controller; does this stream come from upstream FTSWs?)  
  [answer=yes, the stream comes from upstream FTSW]

- Were 127.21 MHz oscillators fabricated for bPID use (for DSP_FIN boards originally)?  
  [answer=yes, there's enough]

- How much control will we have over JTAG through FTSW? Can we send an svf stream to bootstrap a single FPGA, then issue it some chipscope-like commands, then stream another 4 copies of a different svf file?  
  [answer=we will have to test this]

- We're planning to chop the cat7 cables and use nicomatic cmm200 connectors for timing/trigger and JTAG links from FTSW; does anyone see a problem with this?  
  [answer=we must test this and decide for ourselves]

- Can Hawaii have a UT3 board?  
  [answer=Hawaii will buy some]
bPID / TOP front-end electronics: Questions (2/2)

- Does anyone know of a Xilinx Zynq SoC being used successfully in a 1.5T field with active gigabit transceivers? [answer=no]

- Where are the TOP power supply rack(s) located and how many U of vertical space do we have? (assuming a 24m power cable between the e-hut rack for TOP and the furthest TOP module) [answer=e-hut 2F, very near the detector; 64U or so (two racks)]

- Should we sign up for which Tsukuba B4 switchboards we want to reserve? [?]

- Worst case LV power consumption for all TOP is 12.5kW; Best case is 4.5kW
  - includes IR drop in the cables from the e-hut and ~85% inefficiency of supplies, but ignores power supply sequencing
  - plan is to stagger the programming (power up 1 TOP module, program it, 16 times)
  - will there be a command that can cause all TOP modules to become unprogrammed simultaneously? [answer=we must deal with this possibility]
backup
TOP FTSWs in KLM crates (on detector)
Triggered the 2 GeV/c e+ beam with the four trigger counters (two 40 x 40 mm² and two 5 x 5 mm²)

- γ rate: ~30 kHz
- Trigger rate: ~10 Hz
- DAQ rate: ~5 – 10 Hz
# LV power draw details

| Voltage on measured equipment (V) | LV power draw details | LV power draw details | LV power draw details | LV power draw details | LV power draw details | LV power draw details | LV power draw details | LV power draw details | LV power draw details | LV power draw details | LV power draw details | LV power draw details | LV power draw details | LV power draw details | LV power draw details | LV power draw details | LV power draw details |
|----------------------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|
| 1.5V                             | 1.5V                  | 1.5V                  | 1.5V                  | 1.5V                  | 1.5V                  | 1.5V                  | 1.5V                  | 1.5V                  | 1.5V                  | 1.5V                  | 1.5V                  | 1.5V                  | 1.5V                  | 1.5V                  | 1.5V                  | 1.5V                  | 1.5V                  | 1.5V                  |

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