FINESSE/SCROD FPGA Selection
Pin Count

• prerequisites:

<table>
<thead>
<tr>
<th>FPGA on SCROD</th>
<th>zynq '045</th>
<th>zynq '045</th>
<th>settled on '045?</th>
</tr>
</thead>
<tbody>
<tr>
<td>ASIC</td>
<td>IRS3D</td>
<td>IRSX</td>
<td></td>
</tr>
<tr>
<td>FPGA on carrier</td>
<td>zynq '030</td>
<td>none</td>
<td></td>
</tr>
<tr>
<td>calibration constant location</td>
<td>SCROD</td>
<td>carrier</td>
<td></td>
</tr>
<tr>
<td>calibration constant storage type</td>
<td>RAM</td>
<td>FLASH</td>
<td></td>
</tr>
</tbody>
</table>

• required peripherals:
  • temperature sensor per ASIC (i2c)
  • voltage monitor per ASIC (i2c)
  • 16 bit DACs to control sampling speed (i2c)
  • external memory for calibration constants (DDR3 or QSPI)

• pin count estimate from 2013-10-30
Power and Heat
Physical space

• Power and Heat:
  • Q: Have we done a power estimation for the Spartan-6? Zynq?
  • A: spartan6 power spreadsheet

• Physical space:
  • Q: What additional components are necessary for Zynq? / How does that count compare to the Spartan?
  • A: a bunch of capacitors; different regulator voltages
Software support

• What could/would the Zynq ARM cores be used for?
  • ASIC register writes on bootup
  • PID loops - ASIC monitoring and DAC control (internal and external)
  • command packet parsing
  • data packet building
  • pedestal collection and calculation / storage
  • error detection and correction on forward-error correctable calibration constants
  • other miscellaneous (i2c transactions, status packet building, etc)
Multi-FPGA board stack

- What would the carrier FPGA storage requirements be?
  - either none extra, or a DDR RAM on each board

- How would the FPGAs communicate?
  - pair of these? FIFO->OSERDES->ISERDES->FIFO
  - along with (simple) command interpreters / packet routers

- Power estimation?
  - probably something between 2x and 5x of the single-FPGA option (?!?)