boardstack status: schedule

• short-term (by Nov 15th):
  - make mechanical mockup 2-layer PCBs for final form-factor to test-fit with everything else (SCROD, carrier, front, HV)

• medium-term (by Jan 1st):
  - revise carrier board design to use pogo pins so that next deployment can use “intermediate” boardstack with new front and HV boards from Gerard (IU)

• long-term (by March 17th):
  - design/fab/assemble SCROD revB (new FPGA, new connector pattern)
  - design/fab/assemble carrier revE (IRSX ASIC, two-stage amplifiers, sits directly atop SCROD revB)
boardstack status:
mockup of final electronics