IRSX specification review: boardstack constraints

University of Hawaii:
- Gary Varner
- Matt Andrew

Indiana University:
- Gerard Visser

SLAC:
- Kurtis Nishimura
IRSX boardstack constraints: SCROD

- change size of PCB, add thermal structure
- switch to 900 “pin” FPGA (31x31 mm^2)
- move connectors to reduce signal overlap
IRSX boardstack constraints: digital signals

- make global sampling alignment clock point-to-point LVDS instead of single-ended bussed
- remove some test outputs to save pins and FPGA IOs
- switch many other critical signals to LVDS:
  - data outputs change from 12 parallel single-ended (bussed to 4 ASICs) to 4 point-to-point LVDS signal pairs; will make simultaneous read out of individual ASICs possible and reduce deadtime
  - trigger bits (not sure we have enough IOs for that...)
  - WR_ADDR becomes a serial link for each ASIC (not decided yet; would further reduce deadtime)
IRSX boardstack constraints: carriers

- add second stage of amplification
- move connectors around to reduce signal overlap
- add some connector pins (440->480)
IRSX boardstack constraints: analog signal fidelity

- combine “front-front” and “front-back” into single PCB, shortening traces and reducing opportunities for impedance mismatches
- change to two-stage amplification
- split digital signals into new connector positions by function:
  - keep single-ended signals far away from analog signal after first stage of amplification (and very far away from unamplified analog signal)
  - put LVDS signals and amplifier power through upper row of connectors
  - put single-ended signals and ASIC power through lower row of connectors
IRSX boardstack constraints: power

- existing boardstack draws ~35W from LV supplies:
  - ASICs draw ~20W
    - expect this to drop somewhat during conversion as we remove 8*64 ripple counters
  - FPGA / fiber transceivers draw ~5W
  - amplifiers draw ~10W
    - expect this to increase slightly as we switch to two stages of amplification (and a different amplifier)
IRSX boardstack constraints: HV distribution

- 8 PMTs to power:
  - each PMT has own HV input from offboard coax
  - each raw HV must be divided 5 ways to bias MCP
  - active divider circuit dissipates about 4W (so in good shape here)
IRSX boardstack constraints: thermal

- existing boardstack dissipates ~39W
  - no airflow; must conduct heat to walls of iTOP module and then to pipes containing fluid to be brought out of detector
- currently prototyping new thermal wall concept:
  - larger (but fewer) vias on each PCB in thermal contact area to maximize vertical copper
  - significantly more active thermal contact area on each PCB for (thermal) conduction to wall
  - PCB-wall-PCB-wall-PCB concept to “clamp down” on active thermal area on each board
IRSX boardstack constraints: form factor

- existing boardstack does not fit in detector
- need to compress in height:
  - use shorter board-to-board interconnects
  - shrink HV module and integrate it with the “ceiling”
  - combine “front-front” and “front-back” PCBs into single board
- need to ensure the fiber optic cables aren't bent past their specification
- need to ensure we can install the boardstacks on the end of each iTOP module
  - also need to ensure we can service individual boardstacks and PMTs
- need to guarantee PMT alignment stays fixed once installed
  - using pogo pins instead of 2mm connectors
IRSX boardstack constraints: summary

• have an existing boardstack that basically works, but need to:
  • add amplification (signals not large enough)
  • reduce boardstack size (doesn't fit)
  • go to more powerful FPGA (future-proofing the detector)
  • use new thermal wall concept (localized heating)
  • switch many signals to LVDS and rearranging single-ended ones (reducing EMI)