TOP electronics status

- front-end:
  - carrier02 revB layout:
    - still in progress; hope to finish this week; ask for comments on layout; then start fab early next week
- back-end:
  - 8 repaired DSP_FIN revD in HI; mailing 3 to PNNL ASAP
  - tested local bus readout:
    - revamped my pollable memory firmware/software from 2010 and updated for spartan6 pinout (for revD)
      - tested good on all boards
    - used new PNNL firmware with same (old) software
      - results depend on finesse slot used (?!?):
        - slot a, b: ~few hundred byte errors per 100 M transferred bytes
        - slot c: always good
        - slot d: a few byte errors per 100 M transferred bytes
      - is this a known problem with COPPER/FINESSE, or perhaps marginal timing in the PNNL firmware?