1 introduction

This is a report on work performed in 2012 from November 19th through December 9th as a Short-Term Invited Fellow at KEK.

Belle II is an upgrade to the highly successful Belle detector, which was partly responsible for confirming the theory of the mechanism for CP violation posed by Makoto Kobayashi and Toshihide Maskawa in 1972 (for which they received the Nobel prize in physics in 2008). The Time of Propagation (TOP) counter will be the primary Particle IDentification (PID) device in the barrel region of the Belle II detector.

2 TOP / bPID

The front-end electronics for the TOP detector consist of Micro-Channel Plate PhotoMultiplier Tubes (MCP-PMTs), which are amplified and then read out by custom waveform-sampling Application-Specific Integrated Circuits (ASICs), designed specifically for this project. A Field-Programmable Gate Array (FPGA) controls an array of these ASICs and communicates with the back-end Data Acquisition (DAQ) system. These components exist on Printed Circuit Boards (PCBs) that fit together in what we call a “boardstack” (a diagram and photograph is shown in Figures 1(a) and 1(b)). The bottom-most board, “SCROD,” in this boardstack was in the design stage during my last visit to KEK as a Short-term Visiting Scientist in January of 2011.

(a) Diagram of TOP front-end electronics  
(b) Photograph of TOP front-end electronics

Figure 1: First version of the TOP front-end boardstack

Since then, we have designed, fabricated and assembled each of the other PCBs shown, and verified their basic functionality at a beam-test at Fermilab in December 2011. Performance was found to be inadequate in several ways, which is the reason for our current effort. To address this, a new ASIC has been designed and fabricated (IRS3B) and performance validation is underway. We learned many things about programming FPGAs during and since this beam test, and have re-written our firmware to take advantage of this newfound knowledge. Several flaws were discovered in our PCBs and we have put
a lot of effort into redesigning each one to get the best performance possible.
We have solicited the help of Pacific Northwest National Lab (PNNL) for a
COPPER-based back-end DAQ system and Indiana University (IU) for a new
High Voltage (HV) divider system, both of which were necessary steps that we
would have otherwise had to undertake at the University of Hawaii (UH).

Further testing of the front-end electronics (and the TOP concept itself)
requires construction of a Cosmic-Ray Test stand (CRT) that takes advantage
of cosmic-ray muons that continuously bombard the surface of the Earth. This
CRT is to be located in a tent adjacent to a clean room on the B4 level of Fuji
Hall at KEK, and should be completed by the end of January 2013. We aim to
have our new front-end electronics module ready by that time.

3 PCBs

Printed Circuit Boards (PCBs) are a critical component of the TOP detector’s
front-end electronics. The work I performed at KEK during this visit was to
design the next generation “carrier” PCB that contains the discrete amplifiers
and ASICs.

This process consisted of taking the schematic-level components from three
progenitor PCBs, merging them, and then checking for signal conflicts and
resolving them. The three PCBs whose components went into the design of the
one currently being designed are the “carrier2 revA,” the “IRS2_DC revB2” and
the “carrier1 revB.” The carrier2 revA board (Figure 2(c)) was the original PCB
that had board-to-board interconnects to connect to the rest of the boardstack.
The carrier2 revA was able to accept four of the IRS2_DC revB2 boards (Figure
2(a)), each of which held one of the IRS2 waveform-sampling ASICs, along with
some support circuitry. 32 copies of the amplifier circuit layout were prototyped
on the carrier1 revB PCB (Figure 2(b)). A decision was made to place the
ASICs directly on the carrier boards for several reasons: improved thermal
coupling of heat generated by the ASIC to the aluminum sidewalls that are
part of the housing for the boardstack; better signal integrity (shorter length
traces from input signal to ASIC); assembly issues (connectors for daughtercards
are notoriously difficult to solder without introducing shorts and opens); and
reduction of height of carrier boards in the boardstack (the new boardstack can
be shorter, which is a requirement to be able to fit in the detector). In addition,
a calibration signal distribution circuit has been implemented on the carrier02
so that we can inject pulses with well-behaved amplitude, frequency content and
phase into any of the 128 channels of readout to do in-situ calibration.

The next step (which is mostly complete, but still in progress) is to generate
a PCB layout from this merged schematic. This consists of placing and rotating
components to minimize the lengths of sensitive analog signal traces and to
avoid digital trace crossovers as much as possible. After that, one must route
the traces to where they need to go to match the schematic, all the while checking
that the design rules for PCB fabrication have not been violated. The current
status of the PCB design is depicted in Figure 3.
4 collaboration

Working alongside Kurtis Nishimura was immensely valuable during this trip, as he is intimately familiar with the FPGA's firmware that controls the ASICs. His advice on several design choices helped avoid problems that would have otherwise arisen after this PCB was fabricated.

Likewise, overlapping with the visit of Craig Bookwalter from Pacific Northwest National Lab (PNNL) was also quite valuable. His work was getting the COPPER/FINESSE based backend DAQ communicating with our front-end electronics so that the bugs can be worked out of the system before the CRT needs to start taking data.

5 conclusion / future plans

Most of the design of the new carrier02 revB PCB was done while at KEK. This will be a crucial component for the TOP counter for barrel PID in Belle II. The schematics for this PCB are complete, and the layout is nearly finished. Within a few days of returning to Hawaii, I hope to submit the carrier02 PCB for fabrication. Verification of performance will happen soon after that. In late January or early February of 2013, four of these boardstacks will be fitted with 32 SL-10 PMTs from Hamamatsu, and then mated to a quartz bar to complete a TOP module. This will then be placed in the CRT in Fuji Hall at KEK and performance will be checked over the following months. After that, we will again take our TOP counter to a test beam facility and hopefully be able to show our funding agencies and our collaborators that it will work adequately for use in Belle II.

Funding for this visit was provided by KEK, so my great thanks go to KEK management, and also to KEK administration for all their work to prepare for my stay. Since we will be using some of the Time Of Flight (TOF) counter bars from the Belle detector on which I worked during my first visit to KEK in January, 2011, this current effort builds directly upon work done during my previous stay as a Short-term Visiting Scientist. I find the work environment at KEK to be highly conducive to being able to concentrate on work. The KEK campus is beautiful and I look forward to my next visit to this serene place.
(a) IRS2_DC revB2

(b) carrier1 revB

(c) carrier2 revA

Figure 2: The three progenitor PCBs
Figure 3: Current status of layout of carrier02 revB