TOP electronics: status of carrier board designs

- made several design decisions for this round:
  - placing ASICs + amplifiers directly on carrier levels
  - switching to IRS3B ASIC
  - remapping of pins from SCROD for new ASIC
  - remove many unnecessary external DAC channels

- all of these choices have led to delays in finishing board design for carrier2

- should have populated carrier2 boards @ KEK during first week of December
TOP electronics: status of carrier board designs

• prototyped IRS3B control, thermal structure and amplifiers on previous boards:
TOP electronics:
status of new boardstack

- all carriers to be finished as soon as possible
- after that, will move on to new interconnect board with calibration circuit
- new front-front/front-back will follow that
- after beam-test, will design new SCROD & boardstack components to fit in final detector