Belle2link Report: eKLM

• now:
  • working on boards for amplifier test setup
  • simultaneously working on firmware to control ASICs

• short-term:
  • after basic readout functionality is ready:
    − we will test it at a CRT in Fuji Hall in January 2013
    − and test it at a beamtest in Spring 2013

• long-term:
  • after that, we want to integrate Belle2link into readout
    (spartan6 on front-end to HSLB/virtex5 on back-end)
Belle2link Report:
bPID/iTOP

- last year:
  - wrote aurora-based fiber optic command processing and data transmission protocol/framework: used successfully during a beamtest @ Fermilab in 2011

- now:
  - designing new boards for front-end
  - re-writing command interpreter to reduce FPGA resource usage, but keeping within our framework

- short-term:
  - test in CRT @ Fuji Hall in January 2013
  - test at beamtest in Spring 2013
Belle2link Report: bPID/iTOP

- long-term:
  - we are not planning to use Belle2link for bPID/iTOP:
    - must do feature-extraction on back-end for bPID/iTOP
    - not using HSLB (using DSP_FIN)
    - would require porting both front and back end Belle2link firmware (spartan6 on both front and back end hardware)
  - we are planning to make our system behave like Belle2link from the perspective of the DAQ group, so it should be transparent to everyone else