Backend DSPs and Existing Code

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Backend DSPs

- Analog Devices Blackfin 561
- Dual-core, fixed point, 533MHz
- Each DSP is connected to 256MiB of SDRAM
- Interface to FPGA is through a pair of 16 bit wide synchronous “PPI” buses
Existing Circuit Boards

- **DSP_cPCI revB:**
  - 3 Spartan-6 LX45(T)
  - 4 * Blackfin 561

- **DSP_FIN revD:**
  - 1 Spartan-6 LX45T
  - 2 * Blackfin 561
Existing Code

2012-10-12
US Belle II firmware self-review @ SLAC
M. Andrew
Outlook

• Short-term Outlook:
  ● DSP_FIN board designed in 2009
  ● Code developed in 2009-2010
  ● Code not written to process data with current format
  ● FPGA firmware for DMA transfer must be rewritten
  ● Existing combination of FPGA firmware + DSP software has a few bugs...

• Long-term Outlook:
  ● Developing for Blackfin DSPs requires $3500 compiler and $1200 programmer (per seat)
  ● Requires SDRAM, which is now antiquated and difficult to source
  ● After next April, switching to another DSP or microprocessor is tempting (my cell phone has more processing power than these DSPs now)