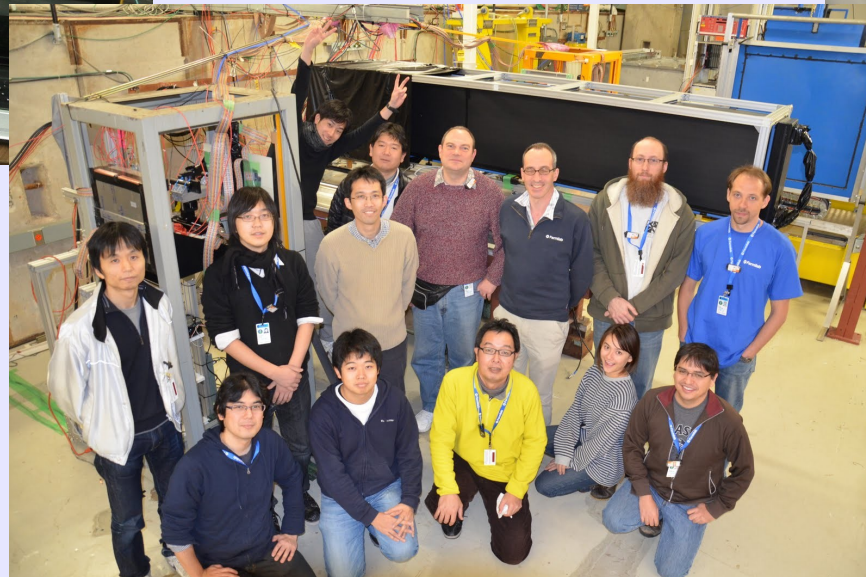
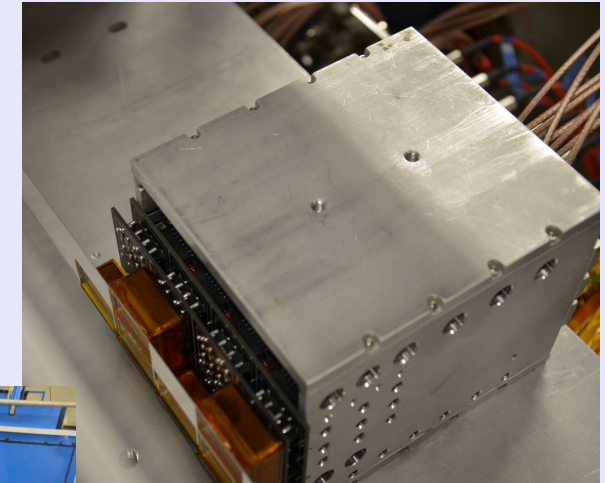
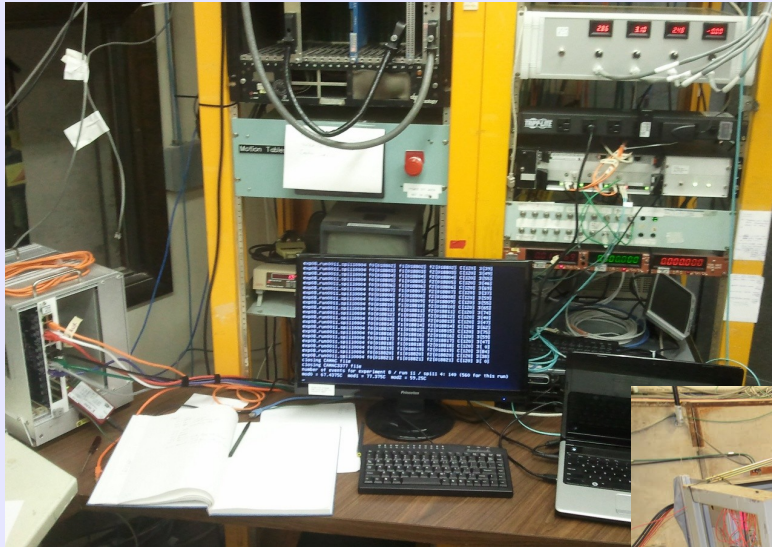


# DAQ at Fermilab T-1019: Belle II bPID (iTOP)



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# DAQ at T-1019

## review of hardware

- front-end:

- SL10 PMT (Hamamatsu)

- only had 20/32 tubes

- IRS2 ASIC (Varner)

- 8 channel; waveform sampling; large analog memory

- boardstack (Ridley/Andrew/Caplett)

- mechanical and electrical interconnects

- SCROD (Ridley/Andrew)

- controller board

- back-end:

- DSP\_cPCI (Ruckman)

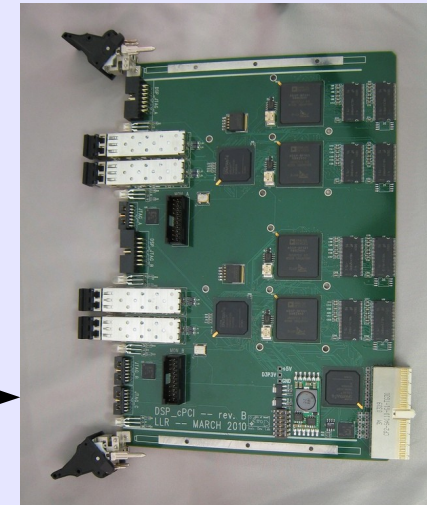
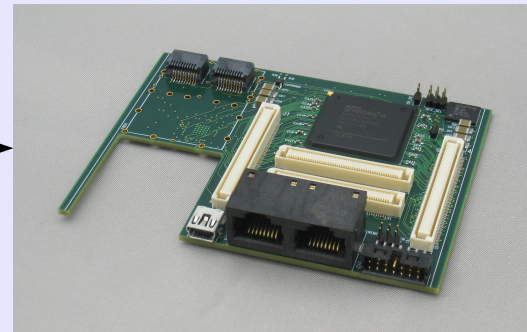
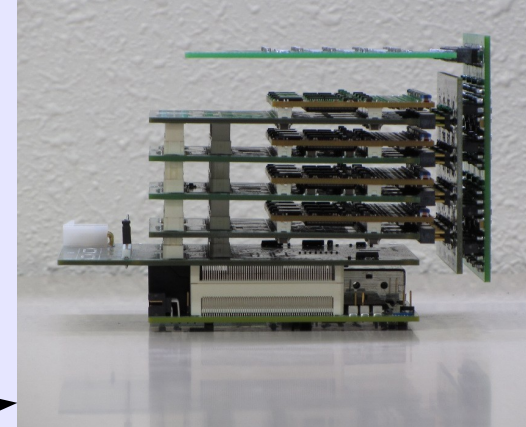
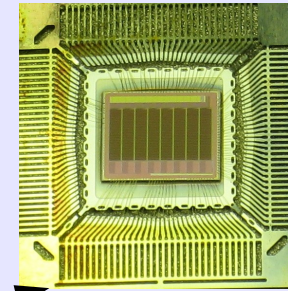
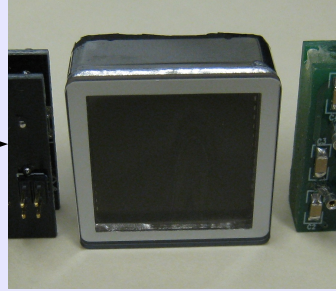
- accepts all data via fiber (Aurora streaming 32 bit) and delivers it to CPU

- FTSW (Nakao)

- allows JTAG programming of front-end

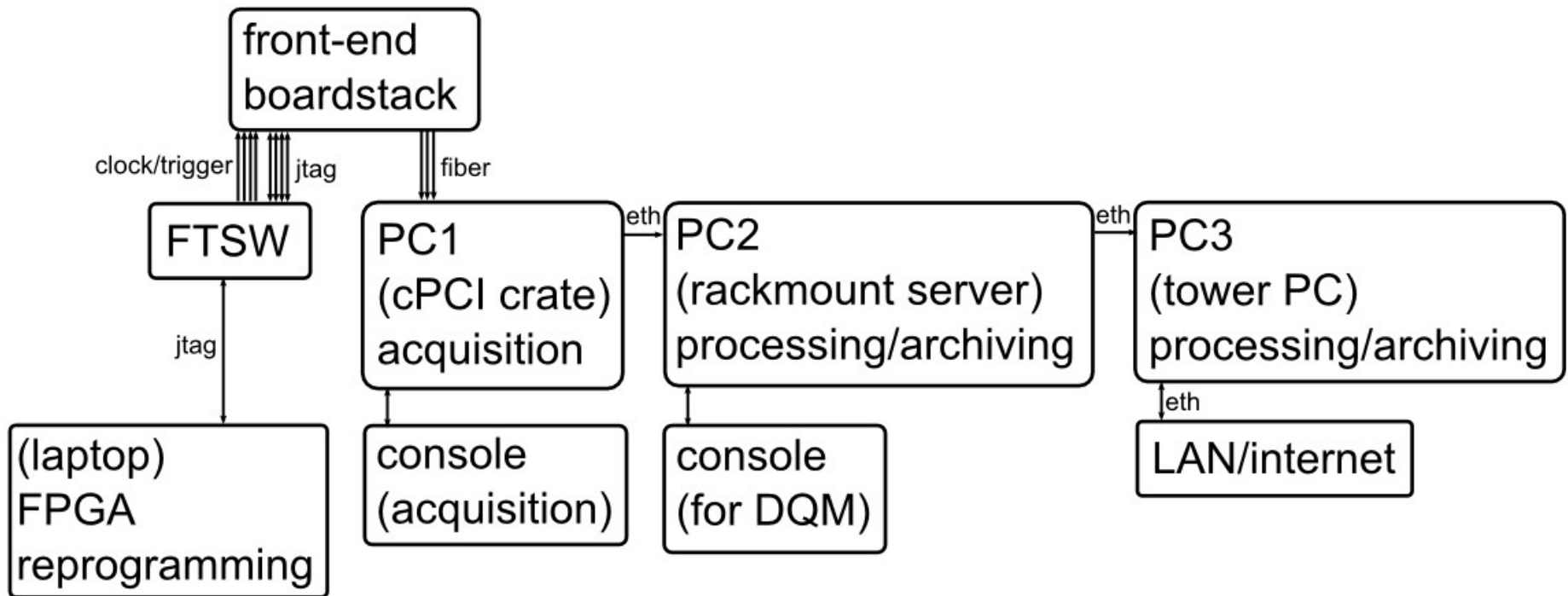
- front-end generates synchronous derived clock from distributed 127.216 MHz clock

- USB CAMAC crate controller (Weiner)



# DAQ at T-1019

## data transfer / processing topology



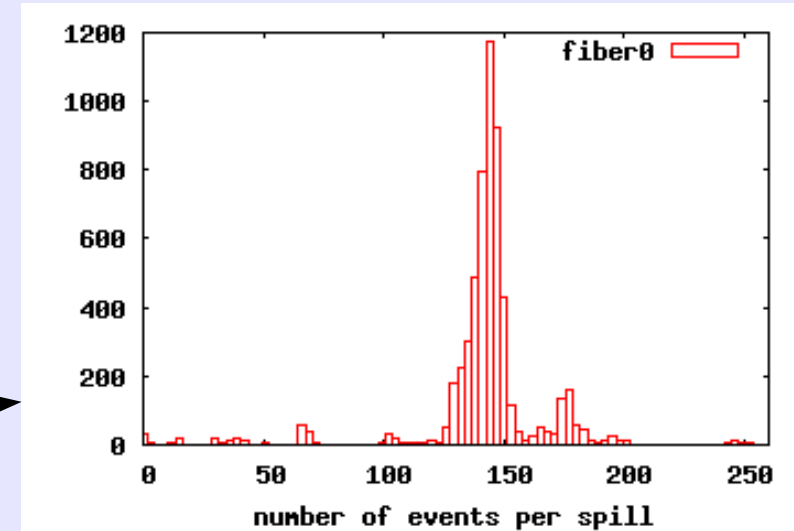
- no zero-suppression (record 256 sample waveforms from all 384 channels)
- trigger causes a gate generator to latch; not cleared until all data is readout

# DAQ at T-1019 problems

- expected to have all computers on Fermilab's network (not possible due to lack of Kerberization)
- FPGAs refused to program (or even identify correctly) for a significant time on two occasions
- lost synchronization of clock derived from FTSW distributed clock ~15 times
- software development was occurring during beam time (cut into overall efficiency)
- configuration of CAMAC ADC/TDCs changed during runs (complicates the data processing scripts)
- for several runs, the LeCroy 3377 module wasn't given enough time to allow its FPGA to load its program (caused overall data rate to suffer)

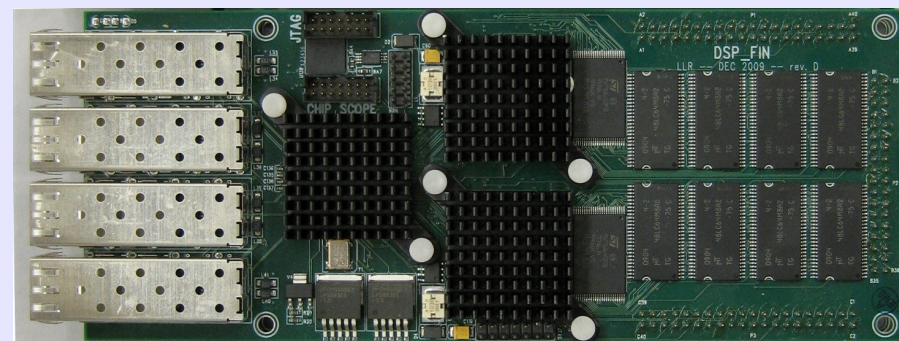
# DAQ at T-1019 statistics

- duration of beam test: 14 days \* 12 hours/day
- spill structure: 4 s / 56 s
- number of spills: 5770 (out of 10080 possible spills)
- uptime: 57% (neglecting accelerator downtime)
- quantity of raw data acquired: 182 GB
- quantity of calibration data acquired: 179 GB
- average data collection rate during spill: ~8 MB/sec
- maximum instantaneous data collection rate: ~14.4 MB/sec (sans CAMAC)
- number of times a front-end module missed a trigger: 41 (99.3% of triggers were seen)
- number of times an FPGA needed to be reprogrammed (other than just after power-up): 18
- quantity of DST1/2/3/4 data: 215GB/319GB/??/??



# DAQ for Belle II bPID status / plans

- process data (an iterative process)
- SCROD revB
  - SPI flash to allow booting on power-up
  - jitter cleaner on-board (plan to distribute 21 MHz)
  - shielded RJ45 connectors (to help with jtag problems)
  - plated edges for thermal coupling
  - other minor changes
- implement trigger in firmware
- implement zero suppression in firmware
- implement waveform processing in DSPs
- switch from cPCI to COPPER/FINESSE
  - may require a new DSP\_FIN revision



# backup slides

- documentation on bPID / TOP electronics/firmware/software:
  - <http://code.google.com/p/idlab-scrod/>
  - <http://code.google.com/p/idlab-scrod/wiki/HowToUseFrontEndElectronics>
  - <http://code.google.com/p/idlab-scrod/wiki/BelleIIbPIDElectronicsDocumentation>
  - <http://code.google.com/p/idlab-daq/>
  - <http://code.google.com/p/idlab-daq/wiki/HowToUseDAQSystem>
- all firmware compiled with Xilinx ISE 13.2