2011 cosmic ray test @ Nagoya electronics status

Matt Andrew / University of Hawai'i
2011-09-26 Belle II bPID cosmic ray test electronics status
# 2011 cosmic ray test @ Nagoya

**PCB status**

<table>
<thead>
<tr>
<th>board name</th>
<th>quantity required for cosmic ray / beam test</th>
<th>quantity we have here in Nagoya</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCROD</td>
<td>4</td>
<td>5</td>
</tr>
<tr>
<td>interconnect</td>
<td>4</td>
<td>5</td>
</tr>
<tr>
<td>carrier0/1/2/3</td>
<td>16</td>
<td>20</td>
</tr>
<tr>
<td>IRS2_DC revB</td>
<td>64</td>
<td>40</td>
</tr>
<tr>
<td>front-front (painted)</td>
<td>4</td>
<td>2</td>
</tr>
<tr>
<td>front-back</td>
<td>4</td>
<td>5</td>
</tr>
<tr>
<td>SL10_HV revA2 (painted)</td>
<td>4</td>
<td>5</td>
</tr>
</tbody>
</table>

The remaining IRS2_DC revB and front-front boards will be shipped to Nagoya sometime next week.
in the design stage for more than a year, we have two complete electronics modules in hand right now
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firmware block-diagram
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firmware tasks/personnel mapping

- Lynn Wood (PNNL)
  - feedback loops for ASIC Wilkinson conversion, sampling rate and trigger width
- Gary Varner (Hawaii)
  - trigger bit stream collection and per-channel scaler accumulation
- Matt Andrew (Hawaii)
  - fiber optic data transfer (raw waveform and sideband data)
  - command decoding and implementation via fiber optic
- Xiaowen Shi (Hawaii)
  - \texttt{i}^2\texttt{c} \texttt{e}^2\texttt{prom} SCROD identity reading/writing
  - \texttt{i}^2\texttt{c} temperature sensor
- Kurtis Nishimura (Hawaii)
  - ASIC sampling control
  - ASIC data readout
  - overall synchronization (with FTSW as clock source)
  - overall firmware integration
2011 cosmic ray test @ Nagoya plans for this week

- **hardware:**
  - solder HV cables from 19” patch panel to SL10_HV revA2 boards
  - procure power supply/supplies that can handle 4 electronics modules, each requiring 5V @ 6A
  - continue debugging remote jtag programming problems

- **firmware:**
  - finish integrating fiber optic readout with Kurtis's ASIC control firmware
  - continue working on fiber optic command interpreter so commands can be sent from back-end to front-end to set modes and DAC values

- **other:**
  - do a LASER scan of an SL10 mounted on a SCROD electronics module (depending on how far development gets)
  - teach someone from Nagoya Daigaku to use Hawaii electronics (because we won't be here for the final integration of QBB + quartz + frame + final batch of SL10s + electronics)
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plans for next week

- hardware:
  - integrate 2 electronics modules with 16 SL10s (depending on how far development gets and whether PMTs are ready)

- firmware:
  - finish adding features to firmware so an almost-final version can be left running to work out bugs

- software:
  - write preliminary version of software to check data quality and extract salient features from raw data to be handed off to Matt Barrett, et al so the analysis framework chain can be further developed

- other:
  - do a LASER scan of several SL10s mounted on a SCROD electronics module (if there is time and everything is ready)
backup
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Block diagram of overall system:

- **20 cm$^2$ trigger scintillator**
- **NIM / trigger coincidence** (coincidence between trigger scintillator signals)
- **NIM / trigger flip-flop** (gate generator with width=latch)
- **CAMAC / TDC and gated ADC / T0 measurement** measures time between raw coincidence trigger and 21MHz synchronous version
- **VME / FTSW**
  - Timing distribution (21MHz clock sent to all SCRODs in-phase)
  - Trigger distribution (synchronous to 21MHz clock)
  - Remote JTAG programming
- **4 x board stack / SCROD**
  - IRS2 ASICs sample continuously into analog memory until trigger arrives
  - Then digitize appropriate parts of analog memory and send data over fiber optic link
- **TTL**
- **4 x fiber optic**
- **USB**
- **cPCI / DSP_cPCI**
  - Takes all data coming in over fiber optic link and from CAMAC TDCs and ADCs
  - After all data for an event accumulated, sends clear signal to NIM trigger flip-flop / gate generator