Belle II bPID front-end / back-end cosmic / beam-test electronics status

Instrumentation Development Lab
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bPID back-end electronics status

firmware tasks (Xin Gao, Serge Negrashov, Kurtis Nishimura, Matt Andrew):
- Aurora/RocketIO data in from fiber optics
- FPGA-FPGA interface
- PCI interface
- DSP interface (skipping this for now)

software tasks (Serge Negrashov & Andrew Wong):
- linux kernel driver
- “userland” library
- “userland” test program
  - “userland” program to raw data dump-to-disk for cosmic run / actual beam-test

overall integration, front-end to back-end:
- only 94% raw data fidelity
- still have some bugs to work out
bPID front-end (BLAB3A version)
electronics board stack status
bPID front-end (BLAB3A version) electronics board stack status

- finding soldering shorts was a problem:
  - decided to teach 4 new people how to solder by having them assemble these boards
  - wrote write/readback firmware to find shorts (called “Get Shorty”)
  - designed dummy board with LEDs to find opens (called “JarJar Blinx”)

- able to write and test state machine firmware for controlling ASICs

- digitization works, but analog performance unacceptable without (a lot of?) further effort
bPID front-end electronics board stack status
bPID front-end (IRS2 version) electronics board stack status

- moved to IRS2 ASIC:
  - same control scheme as BLAB3A
  - no transimpedance gain

- had to redesign ASIC daughtercard to include +36dB of amplification (extends 12mm forward - closer to PMTs)

- had to increase board-stack height to fit these extended daughtercards (each level is now 9mm high vs 6mm high)
bPID front-end (IRS2 version) electronics board stack status

- Being fabricated now (carrier3, IRS2, front-back)
- In hand & assembled; at least partially tested and working (SCROD, interconnect, carrier0, carrier1, carrier2)
- Being redesigned now (front-front, SL10_HV)