iTOP readout electronics status

- IDLAB
- University of Hawai'i
board stack development

2010 November:
concept mechanical design -> mechanical mockup

New Front-end Board Stack

Front
- Connects HV board to PMTs
- Connects PMT output to ASIC input

HV
- High voltage components for PMTs
- Cooling for high voltage components

Standard Control, Read-Out, Data (SCROD)
- FPGA (ASIC control)
  - Virtex4, SpartanII
- 2 Fiber transceivers
- 2 ROAS
  - Clock distribution
  - LVDS (JTAG)
- Mini USB — for easy bench testing

Digitizer Boards (BLAB)
- Carrier card for ASICs
  - 4 ASIC daughter cards per carrier
- ASIC in-situ testing components
  - e.g., pulser for channel checks

ASIC
- 1 BLAB per card
- DACs

Interconnect Board
- Connects SCROD & BLAB
  - Layout of connectors is forced to be unique because of size constraints
  - Power regulation/distribution

2011-04-21 Belle II bPID upgrade meeting
Matt Andrew
University of Hawaii
board stack development

2010 November:
mechanical mockup completed

2011 February:
scaled drawing of most recent iteration

2011 March/April:
blab3a, carrier, interconnect boards being fabricated (should ship this week)
SCROD timeline

2010 November: concept

2010 December to 2011 January: detailed design / schematic entry / layout

2011 February: fabrication & assembly

2011 March/April: FPGA programs and runs!

2011-04-21 Belle II bPID upgrade meeting

Matt Andrew

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