waveform data transfer and back-end processing

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subdetector
MCP-PMT
MPPC
etc

front-end electronics
ASIC -> FPGA

fiber

FPGA -> DSPs

back-end electronics
data storage for archiving and further offline processing
SL10 board stack / front-end module

- each electronics module has:
  - 4 PMTs (SL10)
  - 8 ASICs (BLAB3)
  - 4 DACs to control ASICs
  - 1 FPGA (spartan6t)
  - 2 fiber transceivers:
    - 1 trigger
    - 1 waveform data
DSP_cPCI / Blackfin 561

- **DSP_cPCI board:**
  - 4 fiber-optic inputs for waveform data
  - 4 dual-core DSPs
  - each dual-core DSP has 256MiB RAM
  - (un)processed data sent through PCI bus to linux driver / userland

- **Analog Devices Blackfin 561 DSP:**
  - dual core, fixed-point, 600MHz, parallel execution of some ALU operations (with 16 bit operands)
  - accepts standard c/c++ code
DSP-based fast feature-extraction of time & charge

- preliminary algorithm performs pedestal subtraction, delta-t correction, FFT/iFFT (to filter unwanted frequency components) and a linear interpolation to the leading edge of the pulse
- finds time to a desired fraction of pulse height
- accumulates a value proportional to charge deposited on anode
- each DSP core can handle 60k waveforms per second
CLK_FIN

- FINESSE module that distributes Belle2 RF clock to front-end modules
trigger