documentation:
  the input power connector can be R/A or vertical 3 pin molex mini-fit jr or will fit 16 AWG wires
  signals A+/A- through M+/M- are differential pairs
  signals N-Z and [0]-[5] are single-ended
  signals 0-7 and CL[0]-CL[3] are LEDs
  R/A or vertical coax connectors [0]-[3] will fit LEMO-00 or SMA
  R/A or vertical coax connectors [4]-[5] will fit MMCX
  two pushbuttons can be surface mount or 0.1" headers/wires offboard
  capable of being programmed directly from openocd/wiringpi/bcm_gpio on the rpi
known issues:
  P and Q cannot both be driven by oserdes primitives in more than 4-bit mode
potential things to add for next revision:
  pmod connector
changes since revB:
  removed TRST (actually acted as SRST)

POWER
MOLEX_3PIN_MALE_OR_16AWG
+V GND -V
3 2 1

COAX_LED[0] RC11 1.4k 0402 A C CL[0]
COAX_LED[1] CL[1] C A 1.4k RC8 0402
COAX_LED[2] RC9 1.4k 0402 A C CL[2]
COAX_LED[3] CL[3] C A 1.4k RC10 0402

COAX-RIGHT-ANGLE-THROUGH-HOLE
COAX[0] X[0] 0402 R[0] 50 0805 [0] COAX
COAX-RIGHT-ANGLE-THROUGH-HOLE
COAX[1] X[1] 0402 R[1] 50 0805 [1] COAX
COAX-RIGHT-ANGLE-THROUGH-HOLE
COAX[2] X[2] 0402 R[2] 50 0805 [2] COAX
COAX-RIGHT-ANGLE-THROUGH-HOLE
COAX[3] X[3] 0402 R[3] 50 0805 [3] COAX

CB1 22uF 1210
CB2 22uF 1210
CB3 22uF 1210
CB4 22uF 1210
+RAW
CD1 100uF 10V
-RAW

3.3V
RD1 3.9k 0402
RD2 3.9k 0402
EEP I2C_EEPROM_S0T23-5
SCL SDA VCC GND WP
C13 0.47uF 0402
COAX[3] I2C0_SCL I2C0_SDA

ROT
ROT_1 ROT_2 ROT_4 ROT_8
COMMON
ROTARY-SWITCH-CONNECTOR-5PIN

JTAG14
NC1 GND3 GND5 GND7 GND9 GND11 PRESENT
VREF TMS TCK TDO TDI NC12 NC14
TMS TCK TDO TDI
JTAG_14PIN_2MM

GPIO14 GPIO15 GPIO18 TCK TDO DONE GPIO8_SPI_CE0 GPIO7_SPI_CE1 I2C0_SCL GPIO12 GPIO16 GPIO20 GPIO21

SPARTAN6-LX9-144
TCK TMS TDI TDO
TCK_4_P109 TMS_4_P107 TDI_4_P110 TDO_4_P106
SUSPEND_4_P073 CMPCS_4_P072 PROGRAM_B_4_P037 DONE_4_P071
RESET 1A PUSHBUTTON-NO 1B
DONE
FPGA-F
DONE/PROGRAM_B pullups are not needed

20X2_HEADER_RPI
5V_02 5V_04 GND_06 GND_14 GND_20 GND_25 GND_30 GND_34 GND_39
3V3_01 3V3_17
GPIO2_I2C1_SDA_03 GPIO3_I2C1_SCL_05 GPIO4_GCLK0_07 GPIO14_UART0_TX_08 GPIO15_UART0_RX_10 GPIO18_12 GPIO23_16 GPIO24_18 GPIO10_SPI_MOSI_19 GPIO25_22 GPIO11_SPI_SCLK_23 GPIO8_SPI_CE0_24 GPIO7_SPI_CE1_26 GPIO1_I2C0_SCL_28 GPIO12_32 GPIO16_36 GPIO20_38 GPIO21_40 GPIO9_SPI_MISO_21 GPIO17_11 GPIO27_13 GPIO22_15 GPIO5_29 GPIO6_GCLK2_31 GPIO13_33 GPIO19_35 GPIO26_37 GND_09
RPI

GPIO2_I2C1_SDA GPIO3_I2C1_SCL GPIO4_GCLK0 GPIO17 TDI TMS GPIO10_SPI_MOSI GPIO9_SPI_MISO GPIO11_SPI_SCLK I2C0_SDA GPIO5 GPIO6_GCLK2 GPIO13 GPIO19 GPIO26

8X3_HEADER
C7 C6 C5 C4 C3 C2 C1 C0
Z Y X W V U
BBL-C
B7 B6 B5 B4 B3 B2 B1 B0
B- B+ E- E+
BBL-B
A7 A6 A5 A4 A3 A2 A1 A0
A- A+ C- C+ D- D+ F- F+
BBL-A

GND
X5 MOUNTING-HOLE
X6 MOUNTING-HOLE
MOUNTING-HOLE-4-40-235MILS

3.3V
C4 0.47uF 0402
C5 0.47uF 0402
CA16 4.7uF 0603
VCCO_1_P086 VCCO_1_P076 VCCO_1_P103 86 76 103

bank 1 does NOT support LVDS outputs!
COAX[0] 105 01P_1_RT_P105
COAX_LED[0] 104 01N_1_RT_P104_VREF
GPIO17 102 32P_1_RT_P102
101 32N_1_RT_P101
GPIO14 100 33P_1_RT_P100
COAX_LED[1] 99 33N_1_RT_P099
98 34P_1_RT_P098
97 34N_1_RT_P097
COAX[1] 95 40P_1_RT_P095_GCLK11
94 40N_1_RT_P094_GCLK10
GPIO11_SPI_SCLK 93 41P_1_RT_P093_GCLK9_IRDY1
COAX_LED[2] 92 41N_1_RT_P092_GCLK8
42P_1_RB_P088_GCLK7 88 GPIO4_GCLK0
42N_1_RB_P087_GCLK6_TRDY1 87 GPIO19
43P_1_RB_P085_GCLK5 85 COAX[2]
43N_1_RB_P084_GCLK4 84
45P_1_RB_P083 83 GPIO20
45N_1_RB_P082 82 GPIO8_SPI_CE0
46P_1_RB_P081 81 COAX_LED[3]
46N_1_RB_P080 80 GPIO7_SPI_CE1
47P_1_RB_P079 79 GPIO21
47N_1_RB_P078 78 GPIO12
74P_1_RB_P075_AWAKE 75 COAX[3]
74N_1_RB_P074_DOUT_BUSY 74
SPARTAN6-LX9-144
FPGA-B

3.3V
C2 0.47uF 0402
C3 0.47uF 0402
CA15 4.7uF 0603
VCCO_0_P135 VCCO_0_P125 VCCO_0_P122 135 125 122

bank 0 supports LVDS outputs
ROT_2 144 01P_0_TL_P144_HSWAPEN
143 01N_0_TL_P143_VREF
F+ 142 02P_0_TL_P142
F- 141 02N_0_TL_P141
D+ 140 03P_0_TL_P140
D- 139 03N_0_TL_P139
GPIO2_I2C1_SDA 138 04P_0_TL_P138
GPIO3_I2C1_SCL 137 04N_0_TL_P137
E+ 134 34P_0_TL_P134_GCLK19
E- 133 34N_0_TL_P133_GCLK18
C+ 132 35P_0_TL_P132_GCLK17
C- 131 35N_0_TL_P131_GCLK16
36P_0_TR_P127_GCLK15 127 CLOCK+
36N_0_TR_P126_GCLK14 126 CLOCK-
37P_0_TR_P124_GCLK13 124 B+
37N_0_TR_P123_GCLK12 123 B-
62P_0_TR_P121 121 ROT_4
62N_0_TR_P120_VREF 120 ROT_8
63P_0_TR_P119_SCP7 119 ROT_1
63N_0_TR_P118_SCP6 118 GPIO15
64P_0_TR_P117_SCP5 117 A+
64N_0_TR_P116_SCP4 116 A-
65P_0_TR_P115_SCP3 115 GPIO18
65N_0_TR_P114_SCP2 114
66P_0_TR_P112_SCP1 112 GPIO9_SPI_MISO
66N_0_TR_P111_SCP0 111 GPIO10_SPI_MOSI
SPARTAN6-LX9-144
FPGA-A

3.3V
OSCILLATOR-DIFFERENTIAL-OUTPUT
NC EN/DISABLE VCC GND OUTPUT OUTPUT
CLOCK+ CLOCK-
C12 0.47uF 0402
OSC

these align with rpi zero holes
X1 X2 X3 X4
MOUNTING-HOLE MOUNTING-HOLE-M2.5

3.3V
IIC
GND 3.3V SDA SCL MOUNT1 MOUNT2
GPIO2_I2C1_SDA GPIO3_I2C1_SCL
M1 M2 JST-SH-QWIIC-STEMMA

1X6_BREADBOARD
A4 A5 A6 GND
-RAW +RAW

+RAW 3.3V
3V3 LT1963AES8-3.3
SHDN IN OUT SENSE/ADJ GND3 GND6 GND7
CA3 4.7uF 0603
CA4 4.7uF 0603
3P3

+RAW 1.21V
1V21 LT1963AES8-ADJ
Vout=1.21V(1+RJ/RK)+3uA*RJ
CA5 4.7uF 0603
CA6 4.7uF 0603
1P21

MMCX_RIGHT_ANGLE_THROUGH_HOLE
COAX[4] BUTTON
R[4] [4] COAX
PUSHBUTTON-NO 1A 1B PB
RC7 RC6 RC5 RC4 RC3 RC2 RC1 RC0 1.4k 0402
orange=1.9V@1mA from 3.3V bank
MMCX_RIGHT_ANGLE_THROUGH_HOLE
COAX[5] R[5] 50 0805

ug380: LX9 has 2,724,832 configuration bits, so a 4M flash is enough

3.3V
C6 0.47uF 0402
C7 0.47uF 0402
CA17 4.7uF 0603
VCCO_2_P063 VCCO_2_P042 63 42

master serial / SPI
M0 = 1
M1 = 0

FLASH
VCC 2.3-3.6V CLK CS DI/IO0 DO/IO1 WP/IO2 HOLD/IO3 GND
C1 0.47uF 0402
RB1 100 0402
RB2 100 0402
IS25LP016D-JNLE 16Mbit

bank 2 supports LVDS outputs
GPIO5 70 01P_2_BR_P070_CCLK
69 01N_2_BR_P069_M0_CMPMISO
67 02P_2_BR_P067_CMPCLK
66 02N_2_BR_P066_CMPMOSI
65 03P_2_BR_P065_D0_DIN_MISO_MISO1
GPIO26 64 03N_2_BR_P064_MOSI_CSI_B_MISO0
GPIO13 62 12P_2_BR_P062_D1_MISO2
61 12N_2_BR_P061_D2_MISO3
GPIO16 60 13P_2_BR_P060_M1
59 13N_2_BR_P059_D10
M+ 58 14P_2_BR_P058_D11
M- 57 14N_2_BR_P057_D12
K+ 56 30P_2_BR_P056_GCLK1_D13
K- 55 30N_2_BR_P055_GCLK0_USERCCLK
31P_2_BL_P051_GCLK31_D14 51 GPIO6_GCLK2
31N_2_BL_P050_GCLK30_D15 50 T
48P_2_BL_P048_D7 48 L+
48N_2_BL_P047_RDWR_B_VREF 47 L-
49P_2_BL_P046_D3 46 J+
49N_2_BL_P045_D4 45 J-
62P_2_BL_P044_D5 44 H+
62N_2_BL_P043_D6 43 H-
64P_2_BL_P041_D8 41 G+
64N_2_BL_P040_D9 40 G-
65P_2_BL_P039_INIT_B 39
65N_2_BL_P038_CSO_B 38
3.9K RD3 0402
SPARTAN6-LX9-144
FPGA-C

3.3V
C8 0.47uF 0402
C9 0.47uF 0402
CA18 4.7uF 0603
VCCO_3_P004 VCCO_3_P031 VCCO_3_P018 4 31 18

bank 3 does NOT support LVDS outputs!
P 35 01P_3_LB_P035
34 01N_3_LB_P034_VREF
COAX[5] 33 02P_3_LB_P033
32 02N_3_LB_P032
N 30 36P_3_LB_P030
0 29 36N_3_LB_P029
R 27 37P_3_LB_P027
1 26 37N_3_LB_P026
S 24 41P_3_LB_P024_GCLK27
2 23 41N_3_LB_P023_GCLK26
Q 22 42P_3_LB_P022_GCLK25_TRDY2
3 21 42N_3_LB_P021_GCLK24
43P_3_LT_P017_GCLK23 17 Z
43N_3_LT_P016_GCLK22_IRDY2 16 4
44P_3_LT_P015_GCLK21 15 Y
44N_3_LT_P014_GCLK20 14 5
49P_3_LT_P012 12 X
49N_3_LT_P011 11 6
50P_3_LT_P010 10 W
50N_3_LT_P009 9 7
51P_3_LT_P008 8 V
51N_3_LT_P007 7
52P_3_LT_P006 6 COAX[4]
52N_3_LT_P005 5
83P_3_LT_P002 2 U
83N_3_LT_P001_VREF 1 BUTTON
SPARTAN6-LX9-144
FPGA-D

1.21V 3.3V
C10 0.47uF 0402
C14 0.47uF 0402
CA9 4.7uF 0603
CA7 4.7uF 0603
CA8 4.7uF 0603
VCCINT_P128 VCCINT_P019 VCCINT_P028 VCCINT_P052 VCCINT_P089
GND_P108 GND_P113 GND_P013 GND_P130 GND_P136 GND_P025 GND_P003 GND_P049 GND_P054 GND_P068 GND_P077 GND_P091 GND_P096
VCCAUX_P129 VCCAUX_P020 VCCAUX_P036 VCCAUX_P053 VCCAUX_P090
C11 0.47uF 0402
CA14 4.7uF CA5 4.7uF CA11 4.7uF CA13 4.7uF
CA2 4.7uF CA12 4.7uF CA10 4.7uF
SPARTAN6-LX9-144
FPGA-E

institution:	University of Hawaii at Manoa High Energy Physics Group Instrumentation Development Lab
title:	althea
revision:	BL
IDLAB design #:	IDL_20_024
circuit design:	mza
PCB design:	mza
sheet #:	1 of 1
sheet description:	FPGA
date last modified:	2020-10-26