2014-11-17 fabricated carrier revE
2014-12-18 assembled 36 carrier revE
2015-02 started work on carrier revE2
  pull MIO6 down instead of up to get PLL to start on bootup with default xilinx autogenerated scripts
2015-04-20 carrier revE3:
  fixed wiring for ADCs
  pin D4 (MIO36) shorted to GND to identify this as the revE3
  answer record 52013 implies that it may be the fact that carrier0's PS_SRST_B stays low after PS_POR_B goes inactive that is the problem
2016 sometime: carrier "revE4" was fabbed by modifying the gerbers directly, which resulted in a bunch of unwanted circular copper features on the fabbed boards
2017-01-09 carrier revE5:
  pin D4 (MIO36) shorted to 2.5V to identify this as the revF
2018-05:
  replaced pogo pin assemblies with ERF8-040 connectors
  removed first stage of amplification/shaping
  replaced vped buffer with a simpler circuit
  take a spare output from the second fanout and put it through a lvds-to-ttl buffer and then to a test point

http://www.phys.hawaii.edu/~mza/PCB/TOP/carriers/index.html#carrierrevE2
http://www.phys.hawaii.edu/~mza/PCB/XRM/index.html

C =	0.1	uF	
CA =	4.7	uF	
CB =	47	uF	???
CC =	10	nF	
CD =	100	uF	???
CF =	330	uF	polarized "E"/"D"
CG =	0.1	uF	
CH =	10	uF	0603
CJ =	270	pF	
CK =	12	pF	
CL =	22	uF	0603
CM =	100	pF	
CN =	0.47	uF	
CP =	1	nF	
CQ =	1	uF	
CR =	220	pF	
CS =	47	nF	
CT =	10	nF	0201

this list needs to be revised

R =	10k		
RA =	23.2		
RB =	100		
RC =	2		
RD =	28k,	24.4k, 12k, 13.7k, e	
RE =	300		
RF =	40.2k		
RG =	121k		
RH =	12k		
RJ =	16k		
RK =	7.150k		
RL =	1k		
RM =	196k		
RN =	61.9k		
RP =	20k		
RQ =	174		
RR =	13.7k		
RS =	4.7k		
RT =	50		
RU =	7.5k		
RV =	69.8		
RW =	14k		
RY =	350		
RZ =	604		
RAA =	5		
RAB =	5		
RAC =	1k		
RAD =	1k		
RAE =	69.8		
RAF =	50		
RAG =	20		
RAH =	365		
RAJ =	54.9		
RAK =	499		
RAL =	23.2		
RAM =	3.57k		
RAN =	5.76k		

some are 0201 now... - this list needs to be revised

reminders / notes:
   we consider ourselves "carrier0" and the board below to be "SCROD" and the board above to be "carrier1" etc

common pitfalls:
  can program S818 fanout, but never see SST clocks - SCROD revB needs jumper from AG24 (in breadboard area) to T3.92

institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	carrier
revision:	F
IDLAB design #:	IDL_18_001
circuit design:	MZA, GV, KAN, GSV
PCB design:	MZA, GV
sheet #:	1 of 16
sheet description:	NOTES
date last modified:	2017-06-19

things to do for next carrier revision: _____
  add zero ohm resistor to bussed reset_carriers line so we can have the option of not installing it
  R6 should pull up to 2V5 instead of 2P5PSPL to stop POR/SRST shenanigans

  0.47uF cap on each FPGA bank voltage, as well as the three GTX supply lines

  drive mio[2] (jtag mode select) appropriately (independent mode at power-up so PL can deliver PS_CLOCK)

0_SHOULD_POWER_UP

RAW1

LT3086 DFN16+1-5MMX4MM — 1P0

CH9 22uF 1210 X7R 16V

RH1 12k 0402 · CC8 10nF 0402 · R2 10k 0402 · CH10 15uF 0805 · RL7 976 0402 · RM4 196k 0402

CJ2 270pF 0402 · RZ3 300 0402 · 110 NP0 50V

1P0 → 1V0 TEST-POINT-SURFACE-MOUNT-OCTAGONAL

DBUF3-B BUFFER-OPEN-DRAIN-SN74LVC2G07

RAW2

LT3086 DFN16+1-5MMX4MM — 1P8PL

CH3 22uF 1210 X7R 16V

RD1 28k 0402 · CC2 10nF 0402 · RD3 24.3k 0402 · CH4 15uF 0805 · RL3 976 0402 · RM5 196k 0402

CJ3 270pF 0402 · RZ4 300 0402 · 118PL NP0 50V

1P8PL → 1V8PL TEST-POINT-SURFACE-MOUNT-OCTAGONAL

DBUF3-C BUFFER-OPEN-DRAIN-SN74LVC2G07

CARRIER0_IS_POWERED

RAW3

Rset=66.5k; V_AMPS=3.725V

LT3086 DFN16+1-5MMX4MM — 3P7_VAMPS01

CH37 22uF 1210 X7R 16V

RD5 66.5k 0402 · CC9 10nF 0402 · RD6 60.4k 0402 · CH38 15uF 0805 · RL5 976 0402

CJ13 270pF 0402 · RZ1 300 0402 · 3I7_VAMPS01 NP0 50V

VAMPS01 → 3V7_VAMPS01 TEST-POINT-SURFACE-MOUNT-OCTAGONAL

POWERBAD_VAMPS01

these are pulled up elsewhere

these are pulled down elsewhere

REG_EN_VAMPS01

RAW2

LT3086 DFN16+1-5MMX4MM — 1P8PS

CH1 22uF 1210 X7R 16V

RD2 28k 0402 · CC1 10nF 0402 · RD4 24.3k 0402 · CH2 15uF 0805 · RL2 976 0402

CJ1 270pF 0402 · RZ2 300 0402 · 118PS NP0 50V

1P8PS → 1V8PS TEST-POINT-SURFACE-MOUNT-OCTAGONAL

CG3 0.1uF 0402 X7R 16V

RAW2

Rset=42.4k; V_2P5PSPL=2.51V

LT3086 DFN16+1-5MMX4MM — 2P5PSPL

CH5 22uF 1210 X7R 16V

RD7 42.2k 0402 · CC3 10nF 0402 · RD8 37.4k 0402 · CH6 15uF 0805 · RL4 976 0402

CJ4 270pF 0402 · RZ5 300 0402 · 2I5PSPL NP0 50V

2P5PSPL → 2V5PSPL TEST-POINT-SURFACE-MOUNT-OCTAGONAL

RAW3

LT3086 DFN16+1-5MMX4MM — 3P7_VAMPS23

CH12 22uF 1210 X7R 16V

RD10 66.5k 0402 · CC5 10nF 0402 · RD11 60.4k 0402 · CH18 15uF 0805 · RL8 976 0402

CJ6 270pF 0402 · RZ7 300 0402 · 3I7_VAMPS23 NP0 50V

VAMPS23 → 3V7_VAMPS23 TEST-POINT-SURFACE-MOUNT-OCTAGONAL

POWERBAD_VAMPS23

REG_EN_VAMPS23

RAW1

LT3086 DFN16+1-5MMX4MM — 1P2

CH7 22uF 1210 X7R 16V

RJ2 16k 0402 · CC4 10nF 0402 · RD9 13.7k 0402 · CH8 15uF 0805 · RL6 976 0402

CJ5 270pF 0402 · RZ6 300 0402 · 1I2 NP0 50V

1P2 → 1V2 TEST-POINT-SURFACE-MOUNT-OCTAGONAL

CG5 0.1uF 0402 X7R 16V

2V5

DBUF3-A BUFFER-OPEN-DRAIN-SN74LVC2G07

CG86 0.1uF 0402 X7R 16V

wait for SCROD (or lower carrier) to power up before we do

2V5

AND1 SN74AUP1G08DCKR

SCROD_HAS_BEEN_POWERED

ALL_RAW_VOLTAGES_PRESENT

CG12 0.1uF 0402 X7R 16V

CARRIER0_SHOULD_POWER_UP

institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	carrier
revision:	F
IDLAB design #:	IDL_18_001
circuit design:	MZA, GV, KAN, GSV
PCB design:	MZA, GV
sheet #:	2 of 16
sheet description:	VOLTAGE_REGULATORS_SEQUENCING
date last modified:	2017-06-19

notes on cap counts are from cap count from ug933 (sept '13), but the recommendations changed by the december '13 version

cap count from ug933 z-7045 ffg900 (pages 13-14)

voltages from ds191 page 3

MGT cap count from ug476 page 307

zynq 045 quiescent currents from ds191 page 7

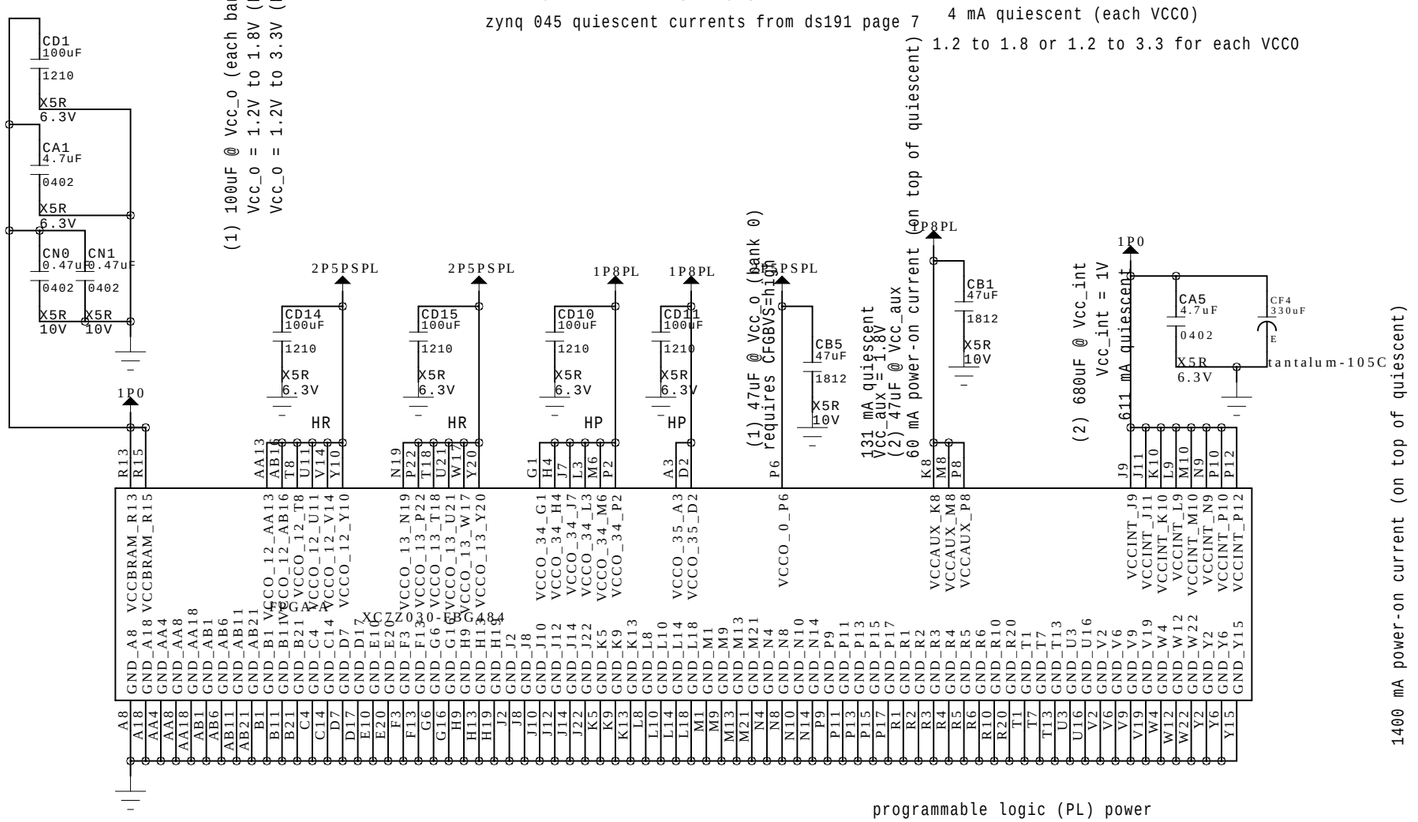
90 mA power-on current per bank (on top of quiescent)

4 mA quiescent (each VCCO)

1.2 to 1.8 or 1.2 to 3.3 for each VCCO

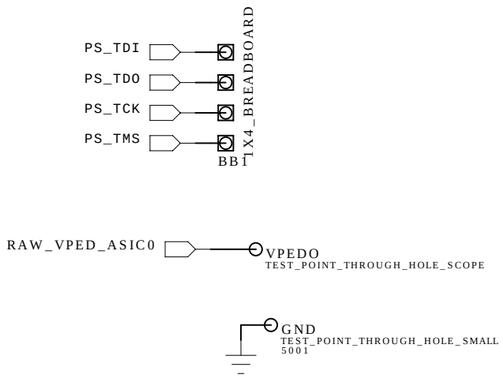
90 mA power-on current (on top of quiescent)
23 mA quiescent
(2) 100uF @ Vcc_bram
(1) 47uF @ Vcc_bram
(6) 4.7uF @ Vcc_bram
(12) 0.47uF @ Vcc_bram
Vcc_bram = 1V

(1) 100uF @ Vcc_o (each bank)
Vcc_o = 1.2V to 1.8V (HP)
Vcc_o = 1.2V to 3.3V (HR)



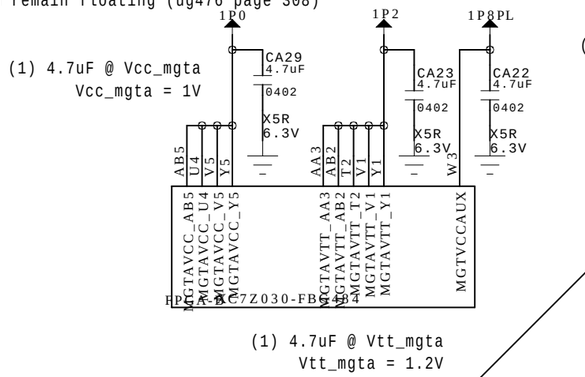
programmable logic (PL) power

1400 mA power-on current (on top of quiescent)



MGTAVCC = 1V; 489 mA for "4 channels @ 3.125 Gb/s" (which is overkill)
MGTAVTT = 1.2V; 428 mA for "4 channels @ 3.125 Gb/s" (which is overkill)
unused quad supply lines can remain floating (ug476 page 308)

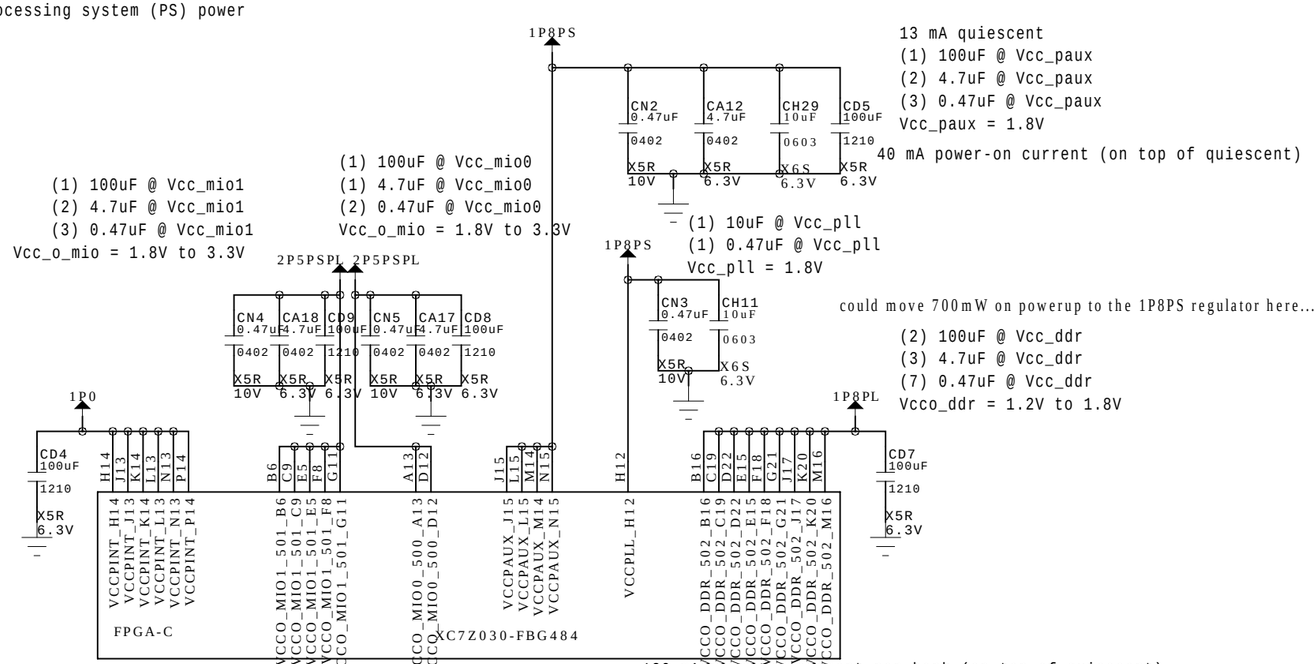
multi-gigabit transceivers (MGT) power



122 mA quiescent
(1) 100uF @ Vcc_pint
(3) 4.7uF @ Vcc_pint
(5) 0.47uF @ Vcc_pint
Vcc_pint = 1V

70 mA power-on current (on top of quiescent)

processing system (PS) power



130 mA power-on current per bank (on top of quiescent)

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PCB design:	MZA, GV
sheet #:	3 of 16
sheet description:	FPGA_POWER_BREADBOARD
date last modified:	2017-06-19

key=gnd for vertical position detection by carrier

carrier presence detect for SCROD

we are "carrier0"

carrierN will get:

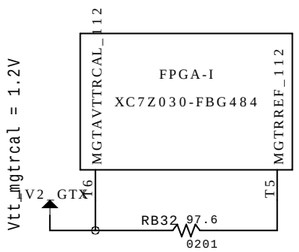
c0	c1	c2	c3
0	1	1	1
1	0	1	1
1	1	0	1
1	1	1	0

GTX-CLOCK-FROM-CARRIER; probably won't be used for TOP

pulled up to 2V5_PSP
open drain; pulled to RAW2
open drain; pulled to 2.5V

IDL_18_001
2017-06-19

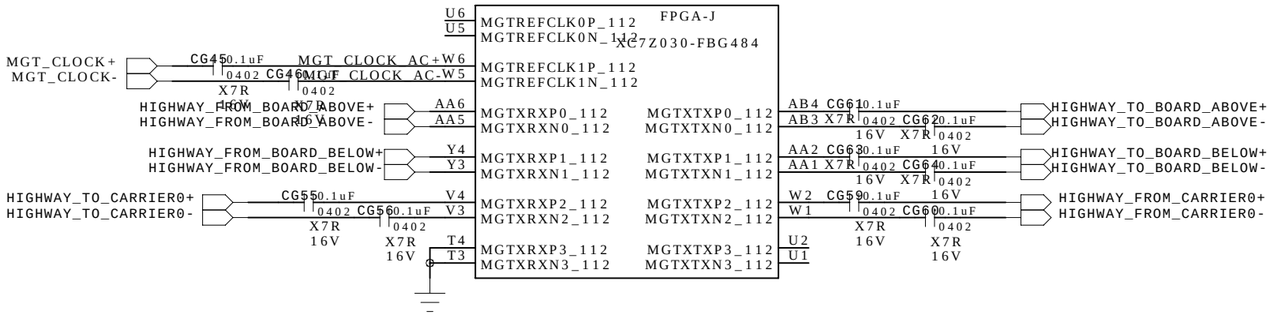
T1, T2, T3 = connectors on top of board; B1, B2, B3 = bottom

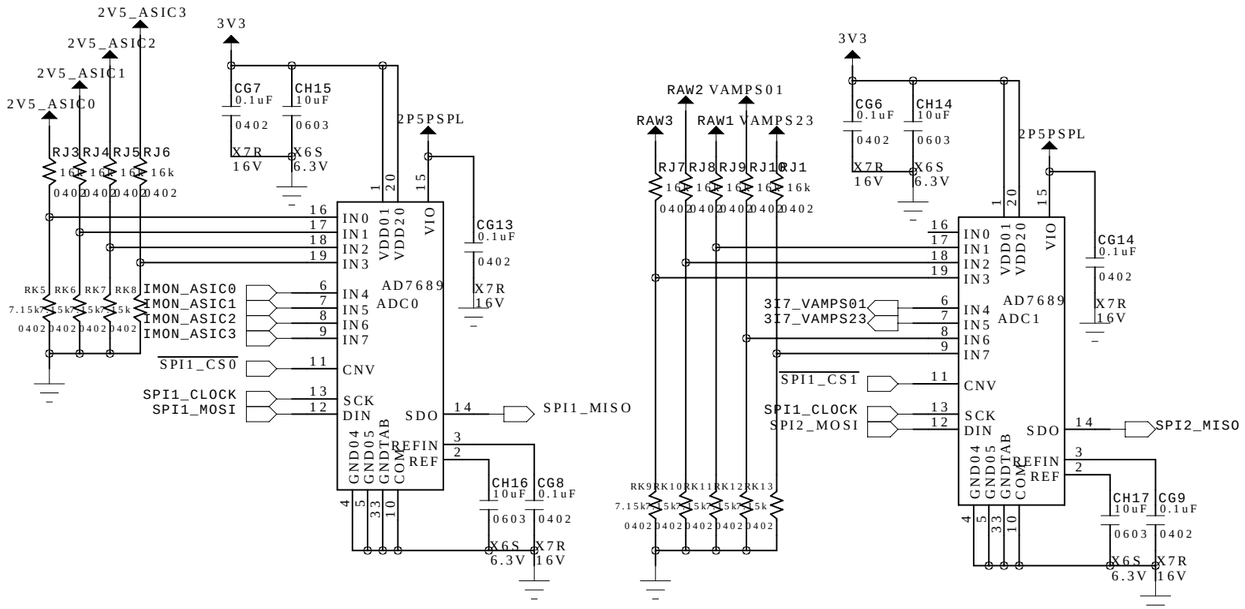


these two traces must be equal length (ug476 page 295)

ug476 page 294 says quad/bank 112 must be powered

GTX clocks via fabric are not recommended due to noise on VccINT and VccAUX
http://www.xilinx.com/support/answers/53500.htm
ug476 page 304 says we should leave unused gtx clock inputs floating
GTX clock must be AC coupled through 100nF caps (ug476 page 307)





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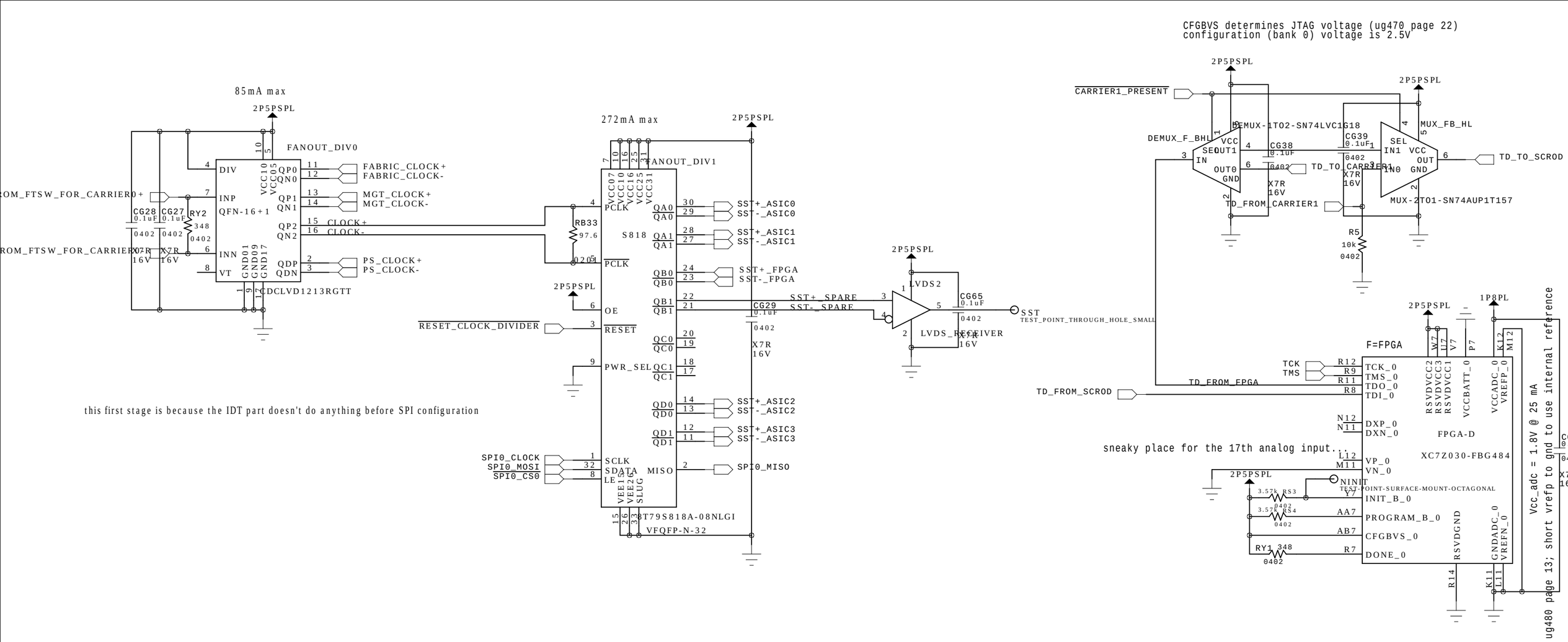
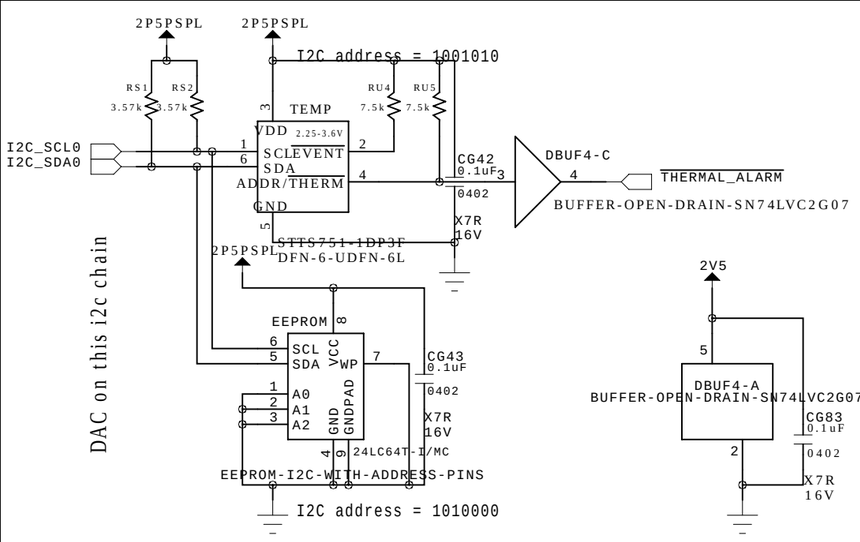
IDLAB design #:	IDL_18_001
circuit design:	MZA, GV, KAN, GSV
PCB design:	MZA, GV
sheet #:	5 of 16
sheet description:	GIGABIT_TRANSCEIVER_ANALOG_INPUT
date last modified:	2017-06-19

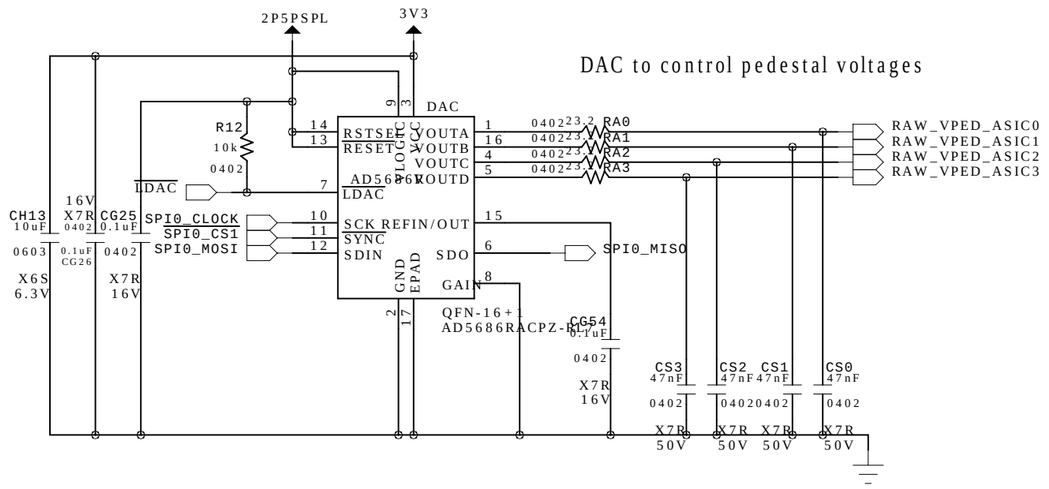
analog inputs for current monitors:
LT3055s drive 1/500th of the current through 150 Ohm resistors
LT3086s drive 1/1000th of the current through 300 Ohm resistors
both of these go into 12 bit ADCs with a 2.5V full-range input
so both give approximately 2mA/ADC count

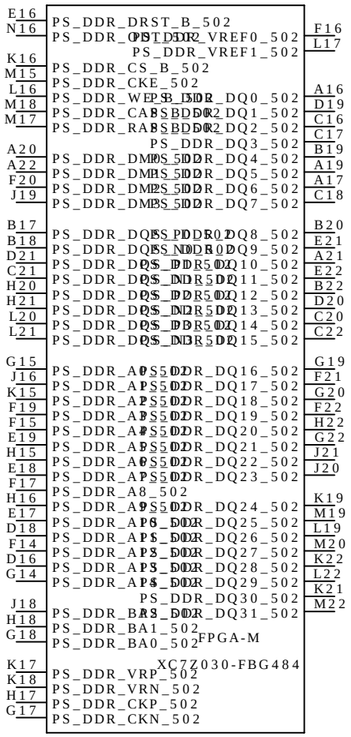
analog inputs for voltage monitors:
the inputs are divided with a 16k/7.15k voltage divider into a 2.5V / 12 bit ADC
so this gives approximately 2mV/ADC count

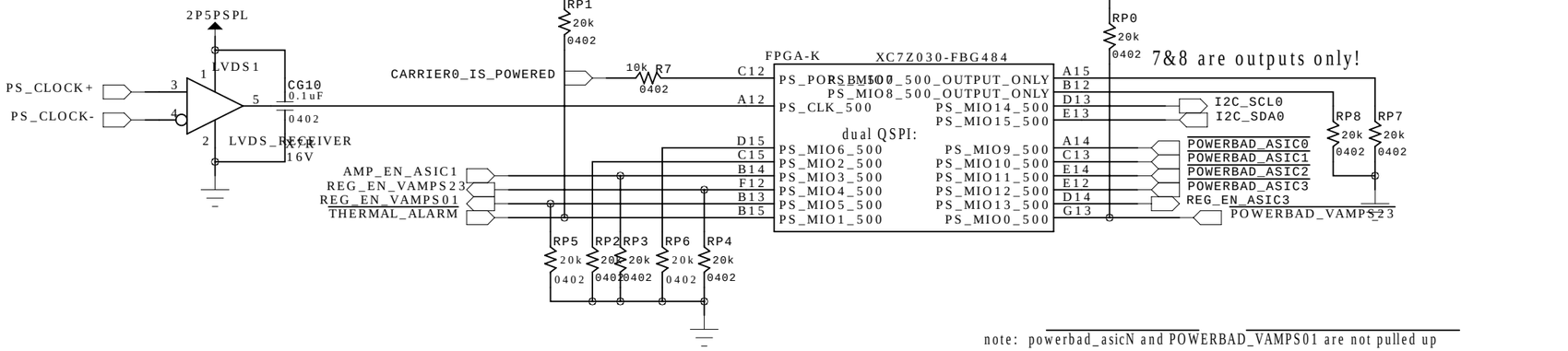


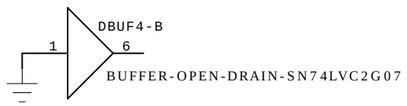
institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	carrier
revision:	F
IDLAB design #:	IDL_18_001
circuit design:	MZA, GV, KAN, GSV
PCB design:	MZA, GV
sheet #:	6 of 16
sheet description:	JTAG_MISCELLANEOUS
date last modified:	2017-06-19

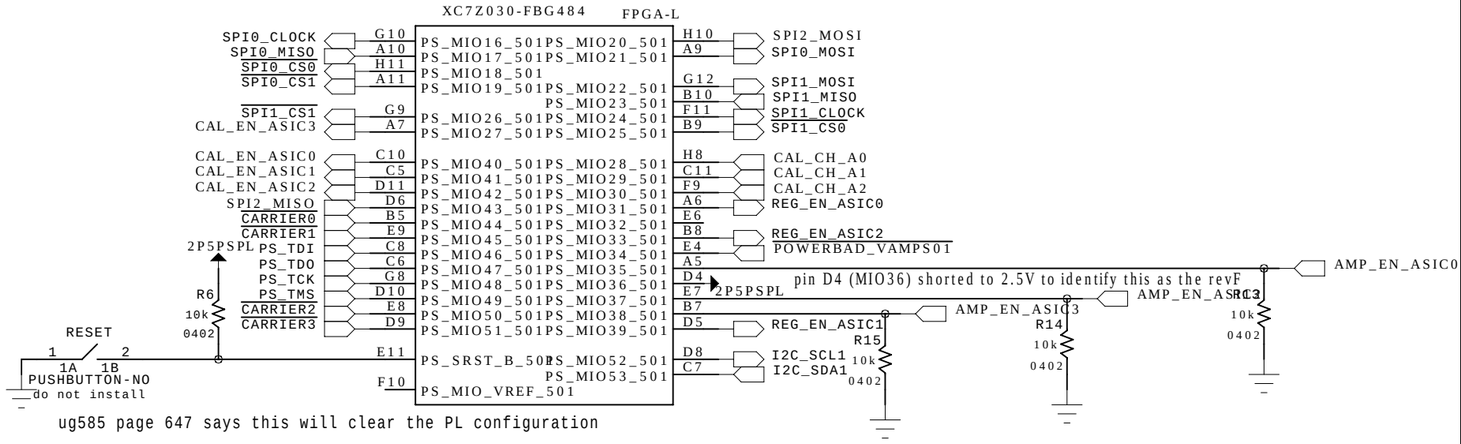












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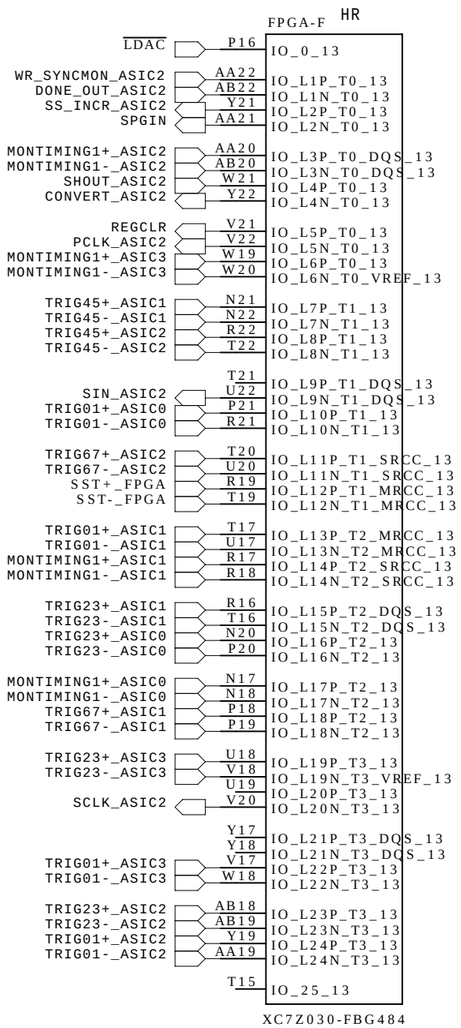
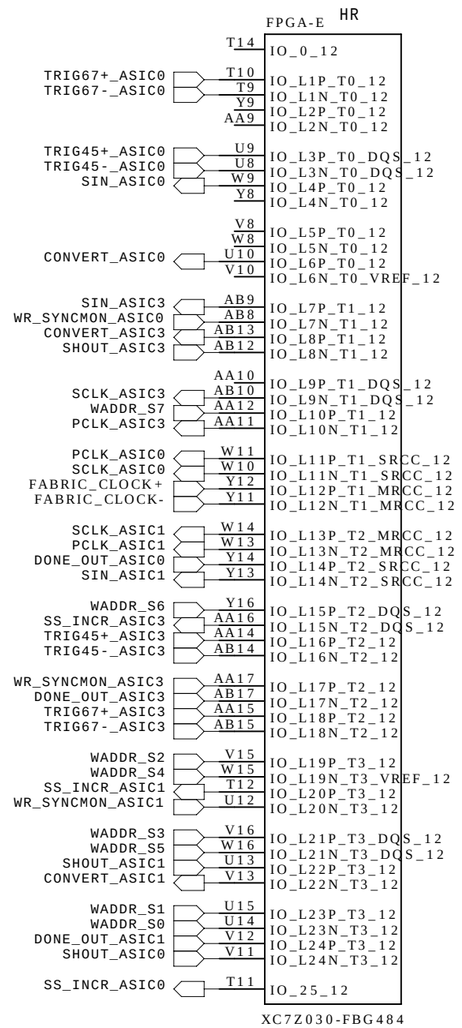
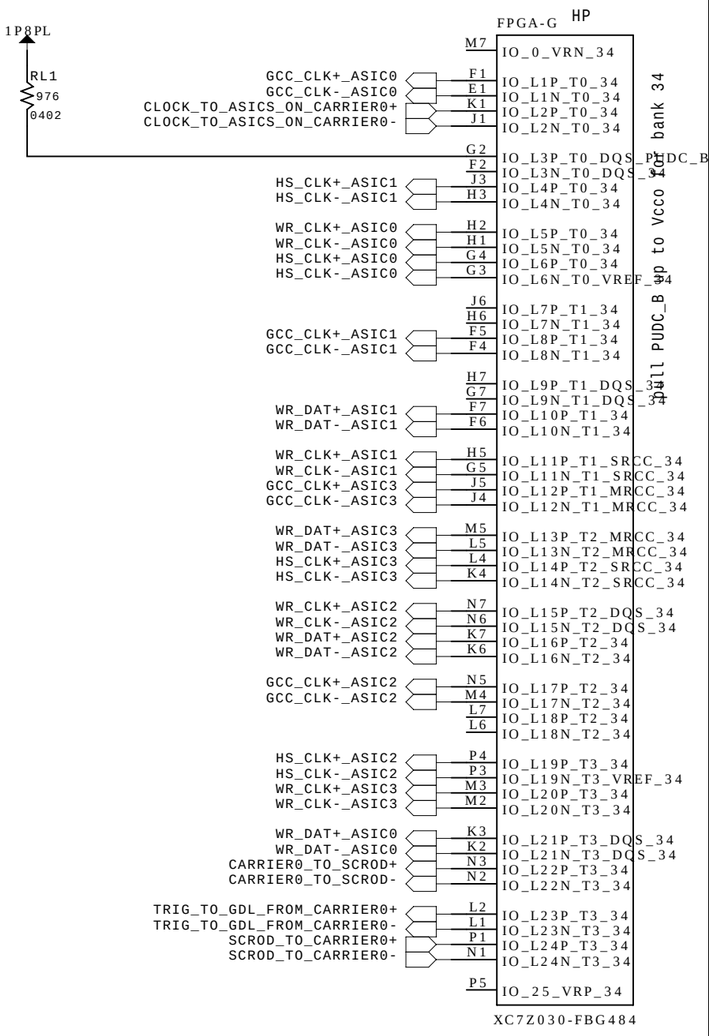
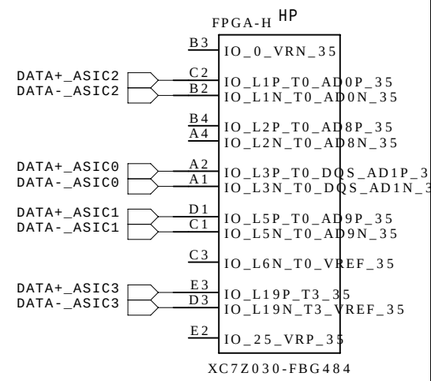
IDLAB design #:	IDL_18_001
circuit design:	MZA, GV, KAN, GSV
PCB design:	MZA, GV
sheet #:	7 of 16
sheet description:	PS_CONNECTIONS_ARM_IIC_DAC
date last modified:	2017-06-19

banks 34, 35 are 1.8V; the rest are 2.5V









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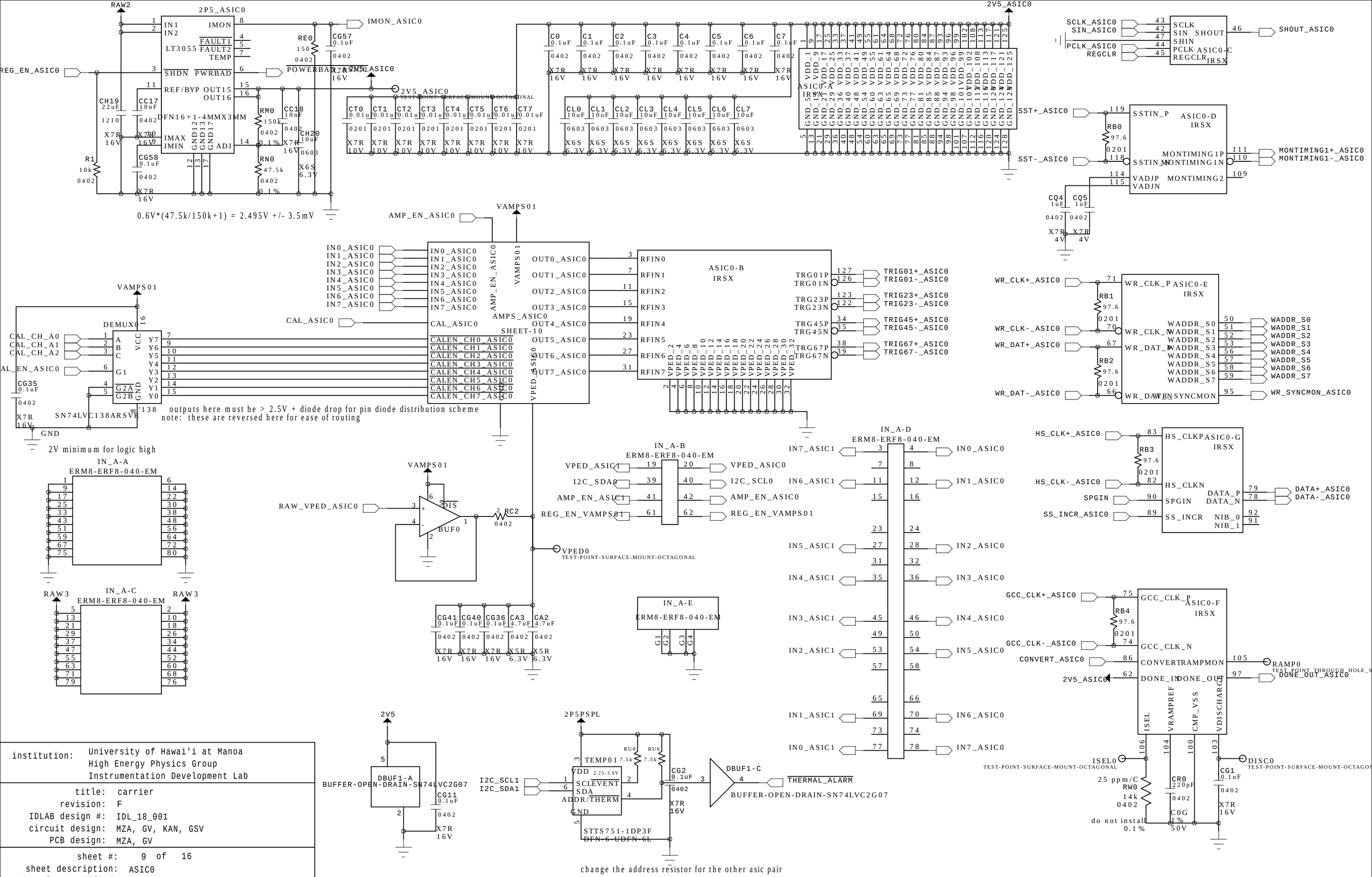
IDLAB design #:	IDL_18_001
circuit design:	MZA, GV, KAN, GSV
PCB design:	MZA, GV
sheet #:	8 of 16
sheet description:	PL_CONNECTIONS_FPGA
date last modified:	2017-06-19

ug480 page 21 says Vccint, Vccaux, Vccbram, Vccpint, Vccpaux, Vcddr are monitored internally



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title:	carrier
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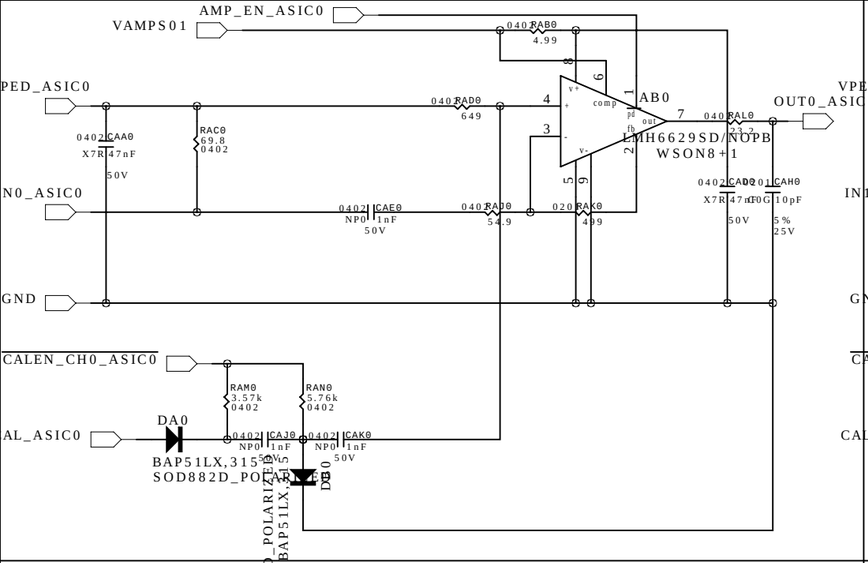
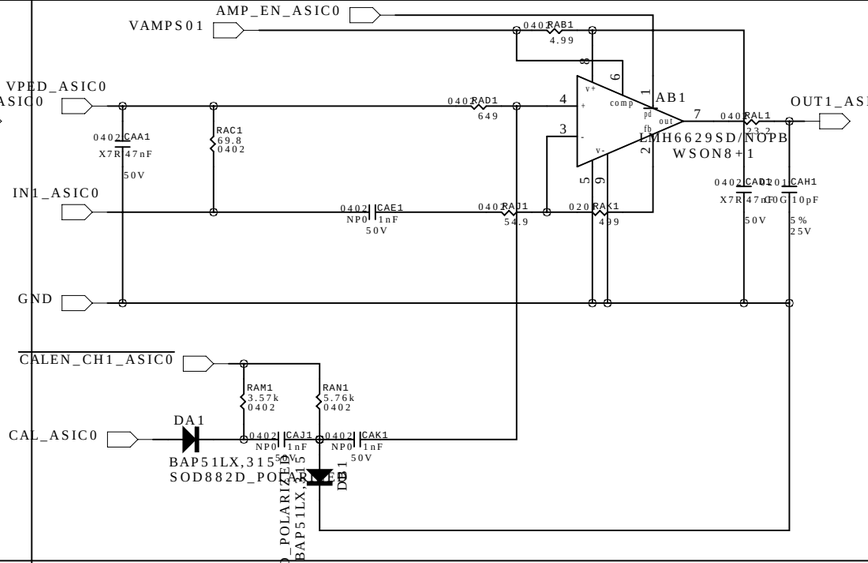
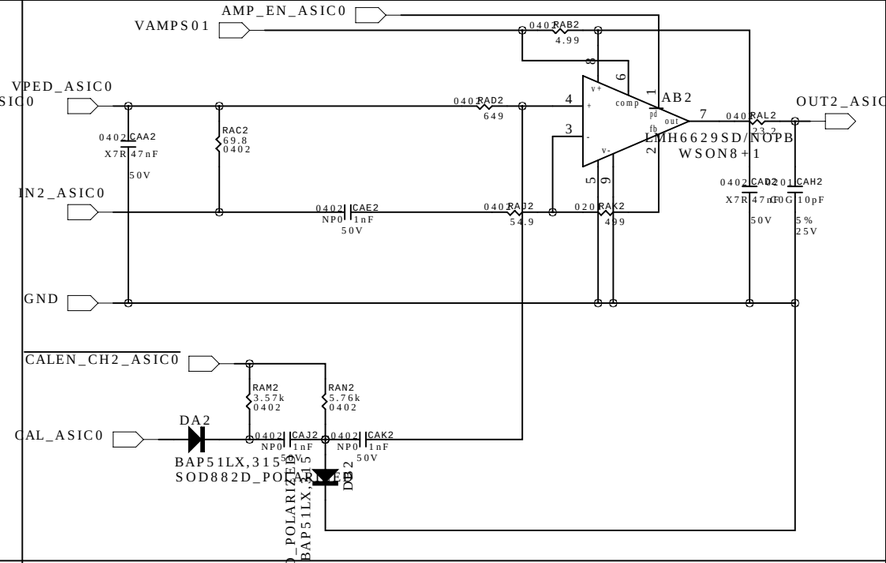
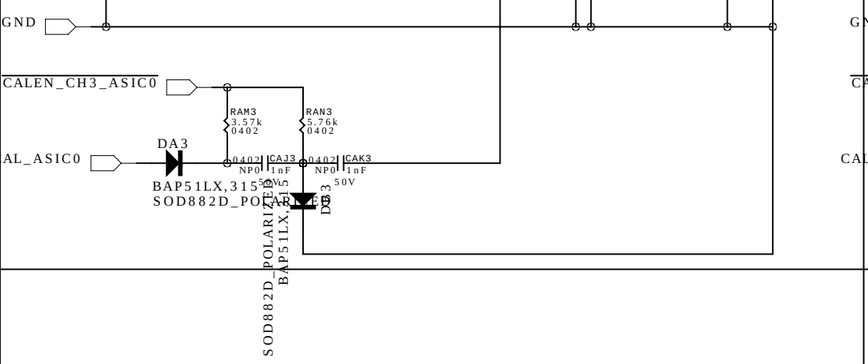
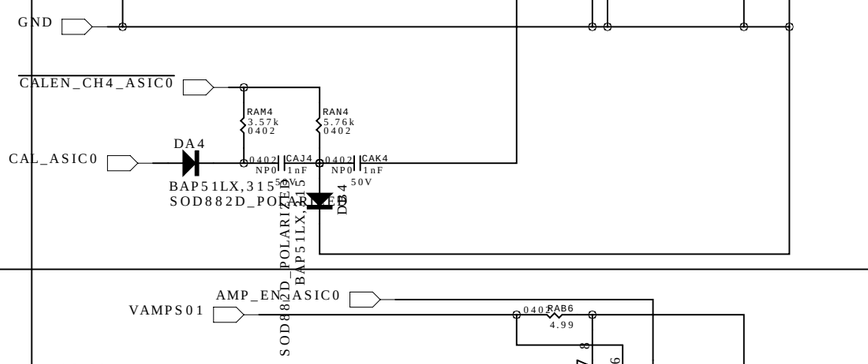
IDLAB design #:	IDL_18_001
circuit design:	MZA, GV, KAN, GSV
PCB design:	MZA, GV
sheet #:	9 of 16
sheet description:	ASIC0
date last modified:	2017-06-19

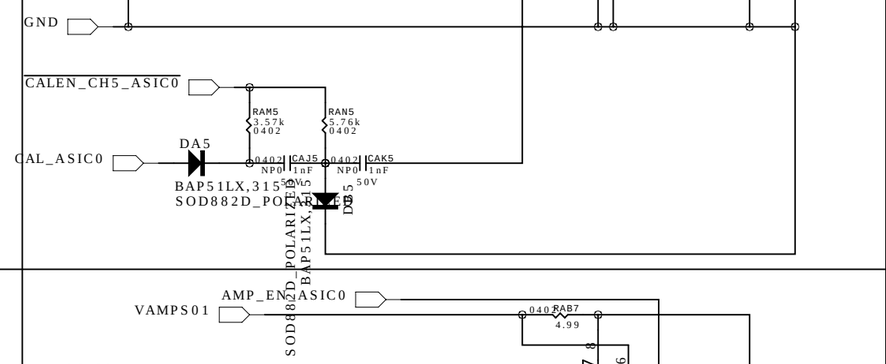


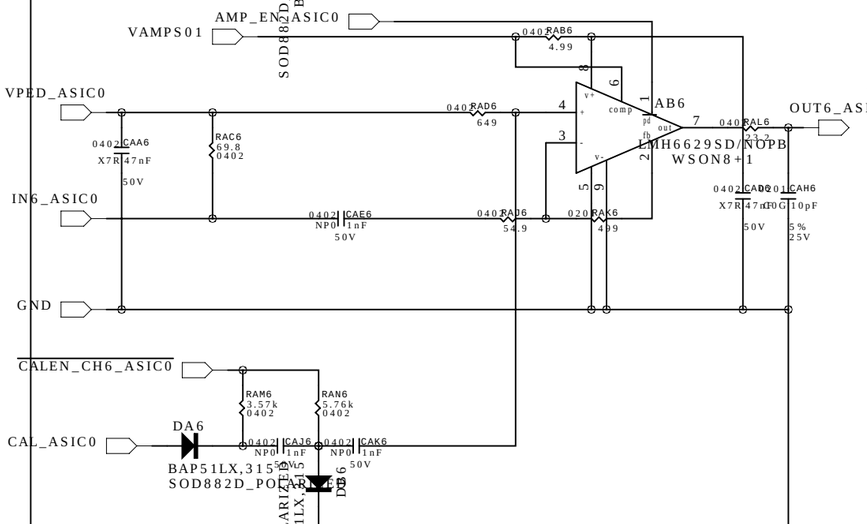


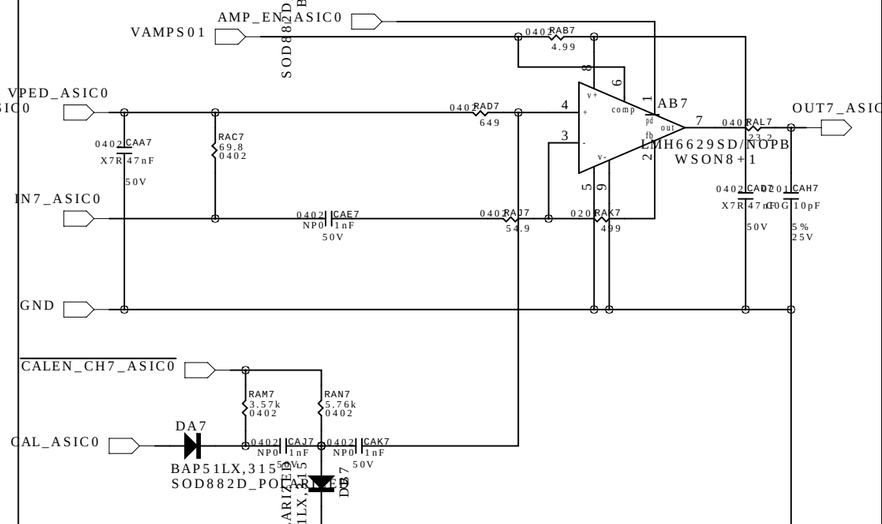


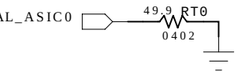




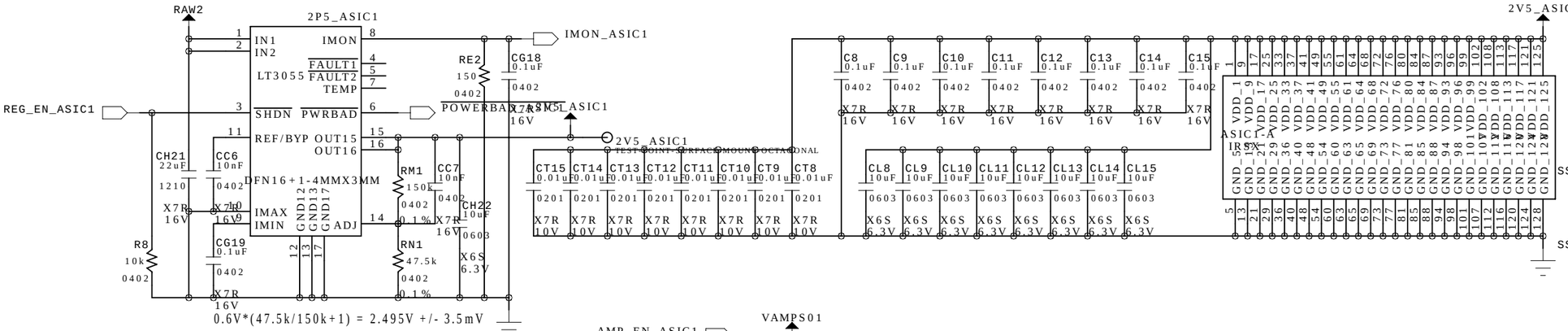




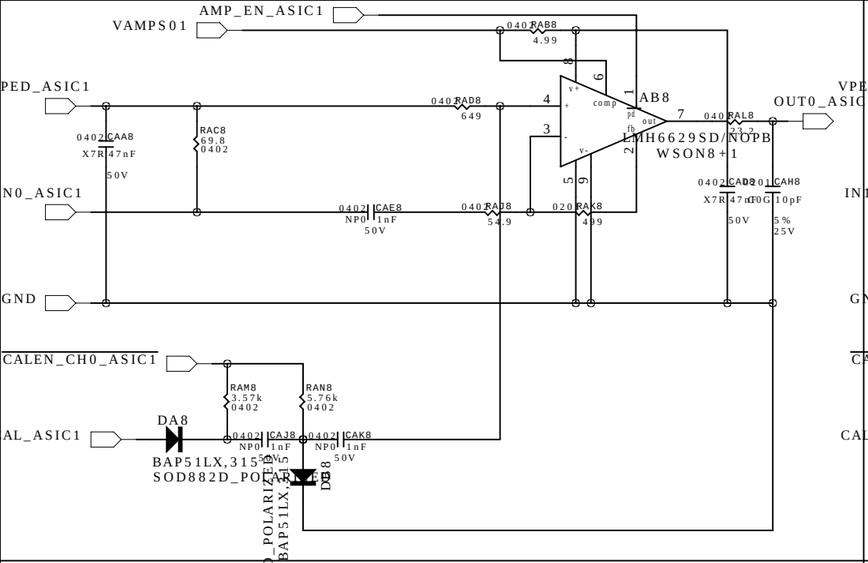


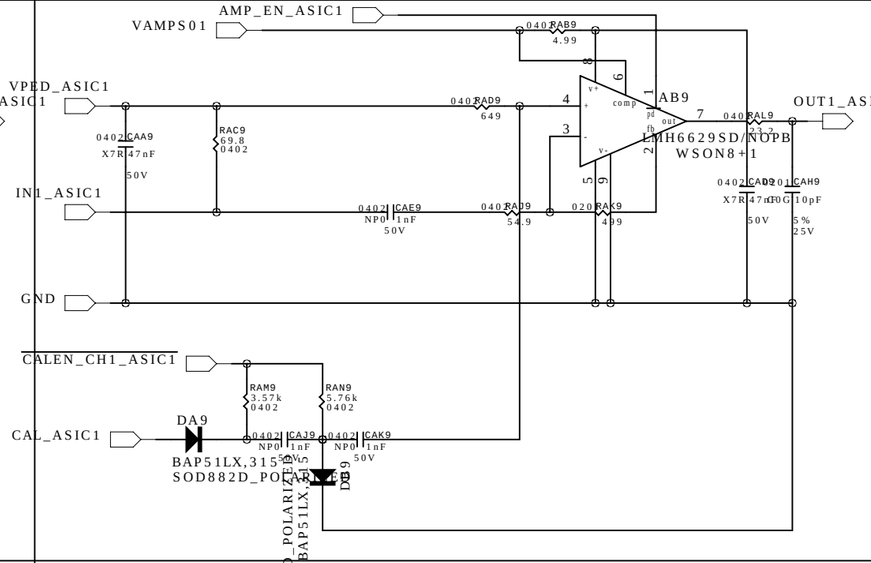


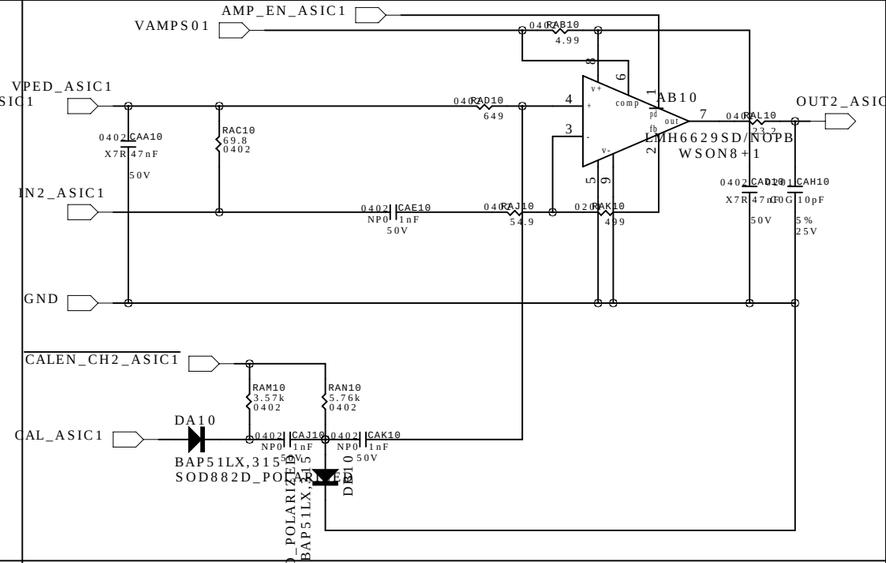
institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	carrier
revision:	F
IDLAB design #:	IDL_18_001
circuit design:	MZA, GV, KAN, GSV
PCB design:	MZA, GV
sheet #:	10 of 16
sheet description:	AMPS_ASIC0
date last modified:	2017-06-19

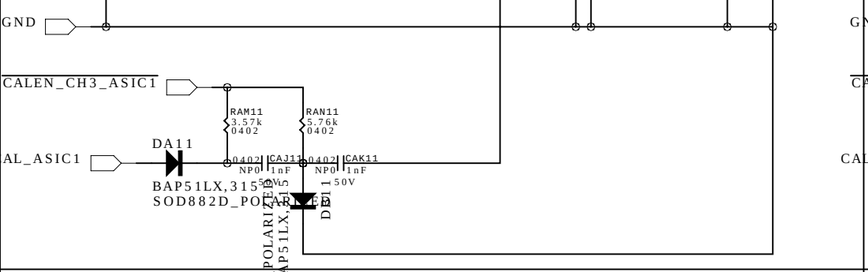


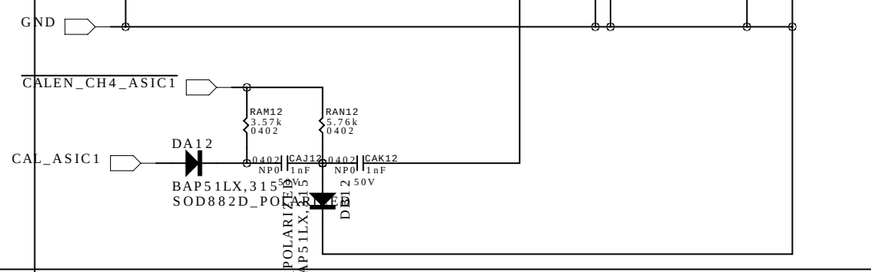
institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	carrier
revision:	F
IDLAB design #:	IDL_18_001
circuit design:	MZA, GV, KAN, GSV
PCB design:	MZA, GV
sheet #:	11 of 16
sheet description:	ASIC1
date last modified:	2017-06-19

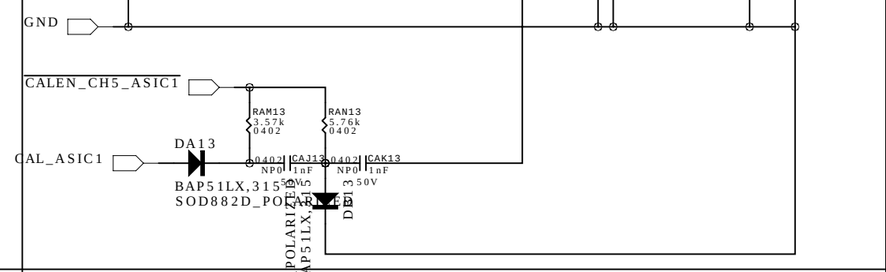


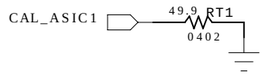


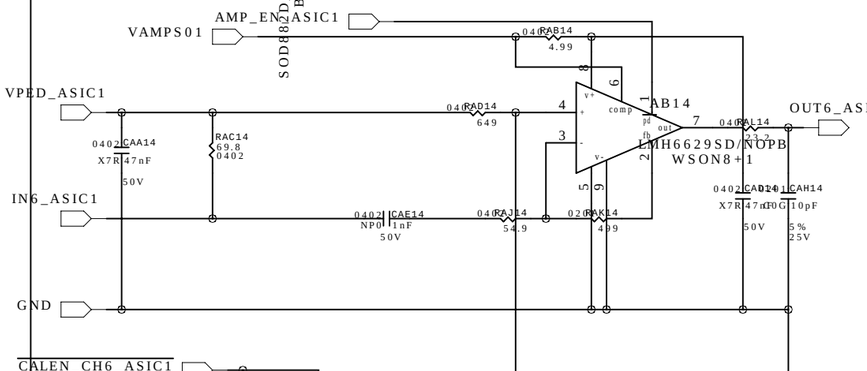


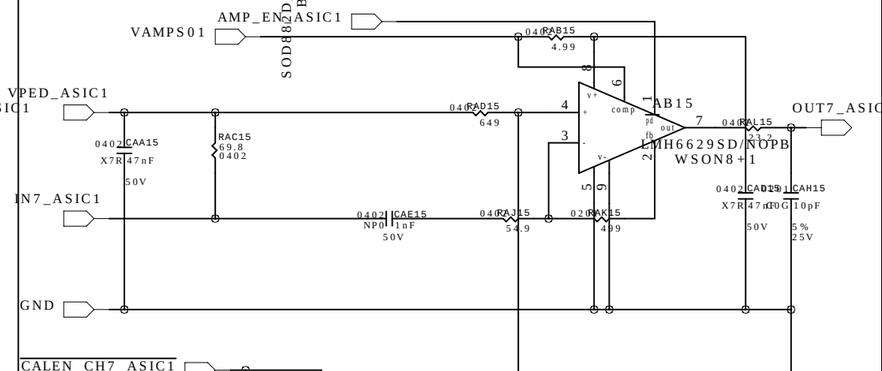












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IDLAB design #:	IDL_18_001
circuit design:	MZA, GV, KAN, GSV
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RAW2
2P5_ASIC2
IN1
IN2
IMON
FAULT1
LT3055
FAULT2
TEMP
SHDN
PWRBAD
REF/BYP
OUT15
OUT16
DFN16+1-4MMX3MM
IMAX
IMIN
GND12
GND13
GND17
ADJ
IMON_ASIC2
RE4
150
0402
CG30
0.1uF
0402
X7R
16V
POWERBAD_ASIC2
REG_EN_ASIC2
CH23
22uF
1210
X7R
16V
CC10
10nF
0402
X7R
16V
CG31
0.1uF
0402
X7R
16V
R3
10k
0402
RM2
150k
0402
0.1%
CC11
10nF
0402
X7R
16V
RN2
47.5k
0402
0.1%
CH24
10uF
0603
X6S
6.3V
0.6V*(47.5k/150k+1) = 2.495V +/- 3.5mV
2V5_ASIC2
C16 C17 C18 C19 C20 C21 C22 C23
0.1uF
0402
X7R
16V
2V5_ASIC2
TEST-POINT-SURFACE-MOUNT-OCTAGONAL
CT23 CT22 CT21 CT20 CT19 CT18 CT17 CT16
0.01uF
0201
X7R
10V
CL16 CL17 CL18 CL19 CL20 CL21 CL22 CL23
10uF
0603
X6S
6.3V
ASIC2-A
IRSX
GND_1 GND_9 GND_17 GND_25 GND_33 GND_37 GND_41 GND_49 GND_55 GND_61 GND_64 GND_68 GND_72 GND_76 GND_80 GND_84 GND_87 GND_93 GND_96 GND_99 GND_102 GND_108 GND_113 GND_117 GND_121 GND_125
GND_5 GND_13 GND_21 GND_29 GND_36 GND_40 GND_48 GND_54 GND_60 GND_63 GND_65 GND_69 GND_73 GND_77 GND_81 GND_85 GND_88 GND_94 GND_98 GND_101 GND_107 GND_112 GND_116 GND_120 GND_124 GND_128
SCLK_ASIC2
SIN_ASIC2
PCLK_ASIC2
REGCLR_ASIC2
SCLK
SIN
SHOUT
SHIN
PCLK
REGCLR
IRSX
SHOUT_ASIC2
SST+_ASIC2
SST-_ASIC2
ASIC2-D
IRSX
SSTIN_P
SSTIN_N
RB16
97.6
0201
MONTIMING1P
MONTIMING1N
MONTIMING2
VADJP
VADJN
MONTIMING1+_ASIC2
MONTIMING1-_ASIC2
CQ3 CQ6
1uF
0402
X7R
4V
VAMPS23
AMP_EN_ASIC2
IN0_ASIC2
IN1_ASIC2
IN2_ASIC2
IN3_ASIC2
IN4_ASIC2
IN5_ASIC2
IN6_ASIC2
IN7_ASIC2
AMP_EN_ASIC2
VAMPS23
AMPS_ASIC2
SHEET-14
CAL_ASIC2
CALEN_CH0_ASIC2
CALEN_CH1_ASIC2
CALEN_CH2_ASIC2
CALEN_CH3_ASIC2
CALEN_CH4_ASIC2
CALEN_CH5_ASIC2
CALEN_CH6_ASIC2
CALEN_CH7_ASIC2
OUT0_ASIC0
OUT1_ASIC0
OUT2_ASIC0
OUT3_ASIC0
OUT4_ASIC0
OUT5_ASIC0
OUT6_ASIC0
OUT7_ASIC0
VPED_ASIC2
ASIC2-B
IRSX
RFIN0
RFIN1
RFIN2
RFIN3
RFIN4
RFIN5
RFIN6
RFIN7
VPED_4 VPED_6 VPED_8 VPED_10 VPED_12 VPED_14 VPED_16 VPED_18 VPED_20 VPED_22 VPED_24 VPED_26 VPED_28 VPED_30 VPED_32
TRG01P
TRG01N
TRG23P
TRG23N
TRG45P
TRG45N
TRG67P
TRG67N
TRIG01+_ASIC2
TRIG01-_ASIC2
TRIG23+_ASIC2
TRIG23-_ASIC2
TRIG45+_ASIC2
TRIG45-_ASIC2
TRIG67+_ASIC2
TRIG67-_ASIC2
VAMPS23
DEMUX2
'138
SN74LVC138ARSVR
CAL_CH_A0
CAL_CH_A1
CAL_CH_A2
AL_EN_ASIC2
CG37
0.1uF
0402
X7R
16V
GND
2V minimum for logic high
outputs here must be > 2.5V + diode drop for pin diode distribution scheme
note: these are reversed here for ease of routing
IN_1-A
ERM8-ERF8-040-EM
IN_1-B
ERM8-ERF8-040-EM
VPED_ASIC2
I2C_SDA0
AMP_EN_ASIC2
REG_EN_VAMPS23
VPED_ASIC3
I2C_SCL0
AMP_EN_ASIC3
REG_EN_VAMPS23
IN_1-C
ERM8-ERF8-040-EM
RAW3
RAW3
VAMPS23
RAW_VPED_ASIC2
BUF2
DIS
RC3
0402
VPED2
TEST-POINT-SURFACE-MOUNT-OCTAGONAL
IN_1-E
ERM8-ERF8-040-EM
G1 G2 G3 G4
CG34 CG33 CG32 CA8 CA7
0.1uF 0.1uF 0.1uF 4.7uF 4.7uF
0402
X7R 16V 16V 16V 6.3V 6.3V
IN_1-D
ERM8-ERF8-040-EM
IN7_ASIC2
IN6_ASIC2
IN5_ASIC2
IN4_ASIC2
IN3_ASIC2
IN2_ASIC2
IN1_ASIC2
IN0_ASIC2
IN0_ASIC3
IN1_ASIC3
IN2_ASIC3
IN3_ASIC3
IN4_ASIC3
IN5_ASIC3
IN6_ASIC3
IN7_ASIC3
2P5PSPL
RP9
TEMP23
7.5k
0402
VDD
2.25-3.6V
SCLEVENT
SDA
ADDR/THERM
GND
STTS751-1DP3F
DFN-6-UDFN-6L
RU1
20k
CG17
0.1uF
0402
X7R
16V
I2C_SCL1
I2C_SDA1
DBUF1-B
BUFFER-OPEN-DRAIN-SN74LVC2G07
THERMAL_ALARM
change the address resistor for the other asic pair
WR_CLK+_ASIC2
WR_CLK-_ASIC2
WR_DAT+_ASIC2
WR_DAT-_ASIC2
ASIC2-E
IRSX
WR_CLK_P
WR_CLK_N
WR_DAT_P
WR_DAT_N
RB17
RB18
97.6
0201
WADDR_S0
WADDR_S1
WADDR_S2
WADDR_S3
WADDR_S4
WADDR_S5
WADDR_S6
WADDR_S7
SYNCMON
WR_SYNCMON_ASIC2
HS_CLK+_ASIC2
HS_CLK-_ASIC2
SPGIN
SS_INCR_ASIC2
ASIC2-G
IRSX
HS_CLKP
HS_CLKN
SPGIN
SS_INCR
RB19
97.6
0201
DATA_P
DATA_N
NIB_0
NIB_1
DATA+_ASIC2
DATA-_ASIC2
GCC_CLK+_ASIC2
GCC_CLK-_ASIC2
CONVERT_ASIC2
2V5_ASIC2
ASIC2-F
IRSX
GCC_CLK_P
GCC_CLK_N
CONVERT
DONE_IN
DONE_OUT
RB20
97.6
0201
RAMP2
TEST POINT THROUGH HOLE_S
DONE_OUT_ASIC2
ISEL
VRAMPREF
CMP_VSS
VDISCHARGE
ISEL2
TEST-POINT-SURFACE-MOUNT-OCTAGONAL
DISC2
TEST-POINT-SURFACE-MOUNT-OCTAGON
25 ppm/C
RW2
14k
0402
do not install
0.1%
CR2
220pF
0402
C0G
1%
50V
CG16
0.1uF
0402
X7R
16V

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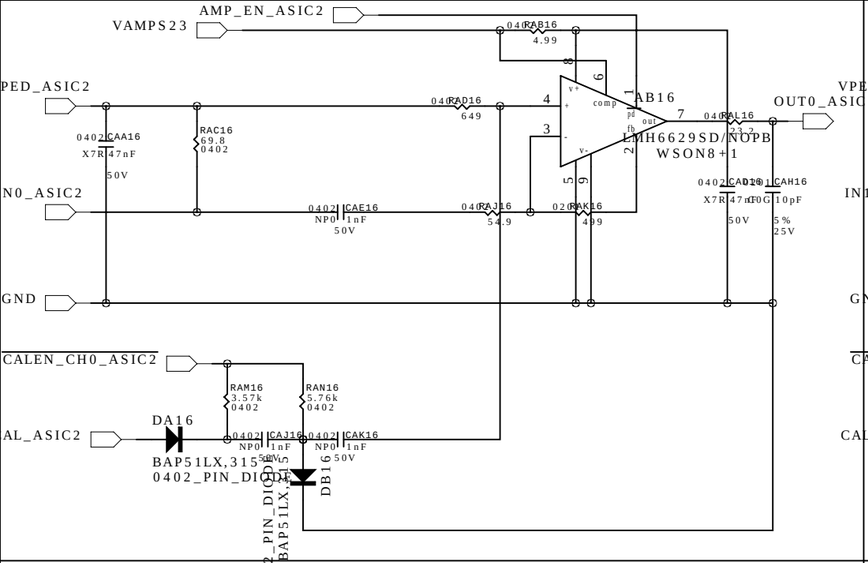
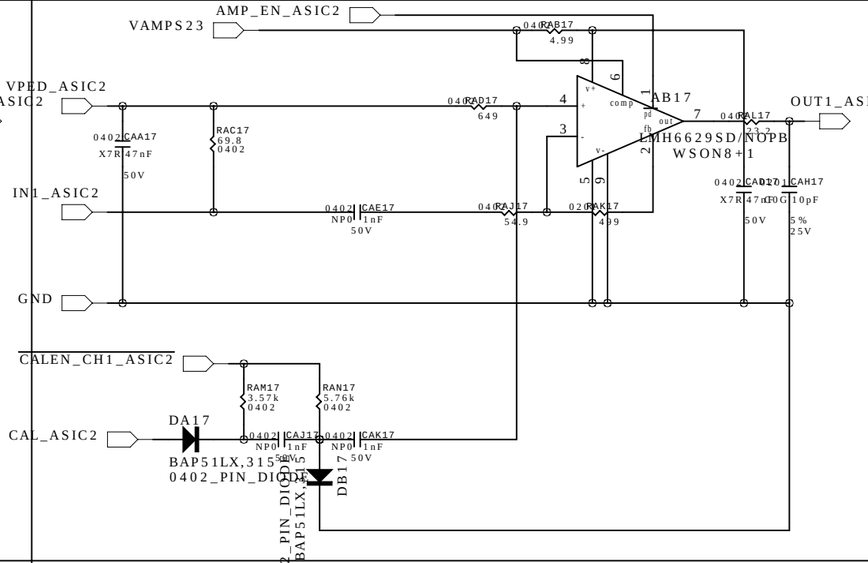
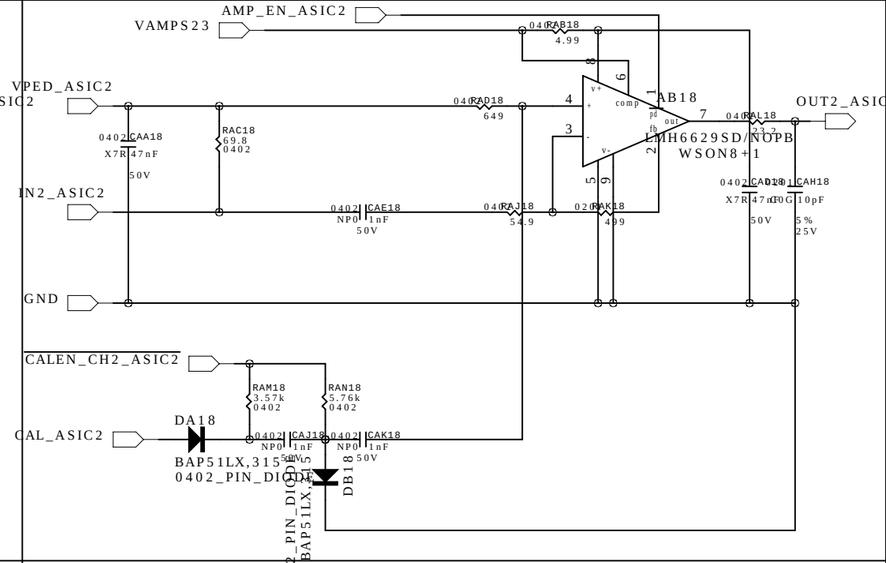
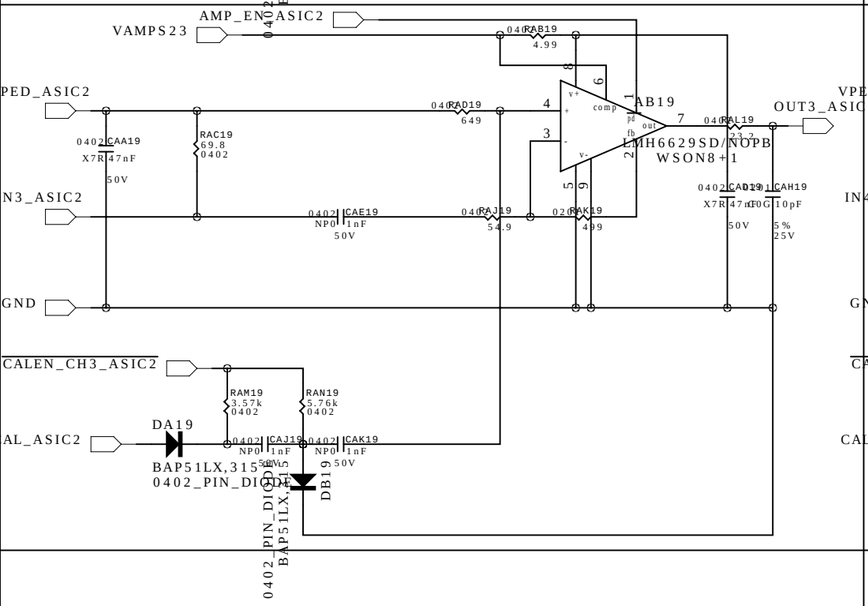
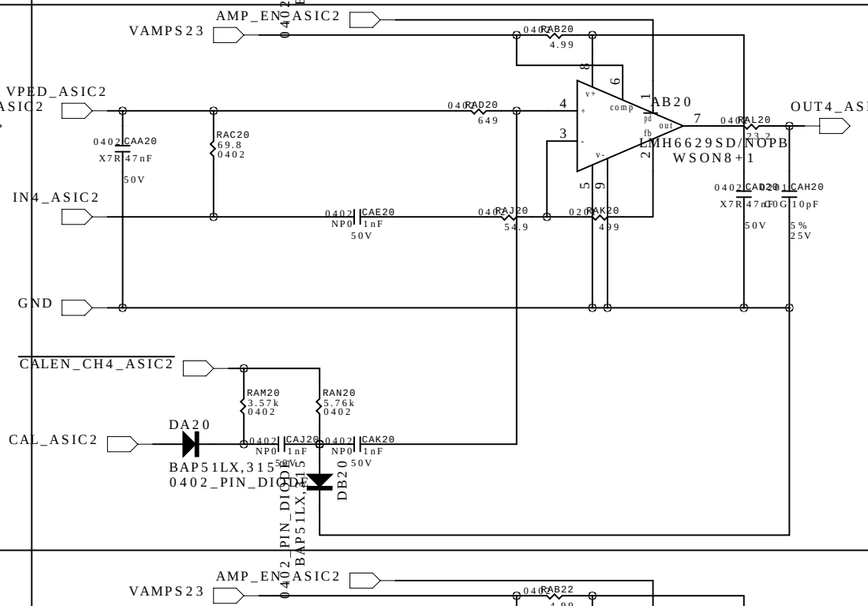
IDLAB design #:	IDL_18_001
circuit design:	MZA, GV, KAN, GSV
PCB design:	MZA, GV
sheet #:	13 of 16
sheet description:	ASIC2
date last modified:	2017-06-19

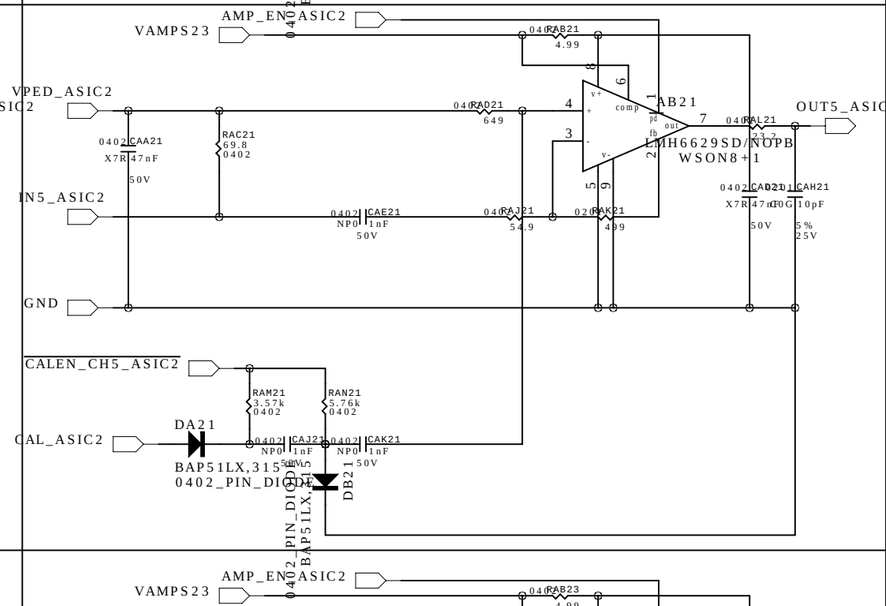


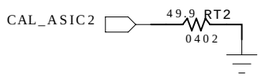


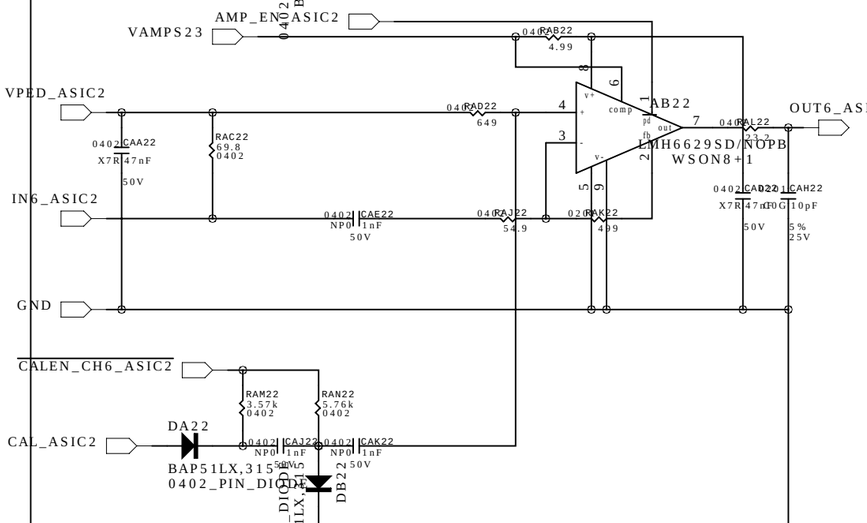


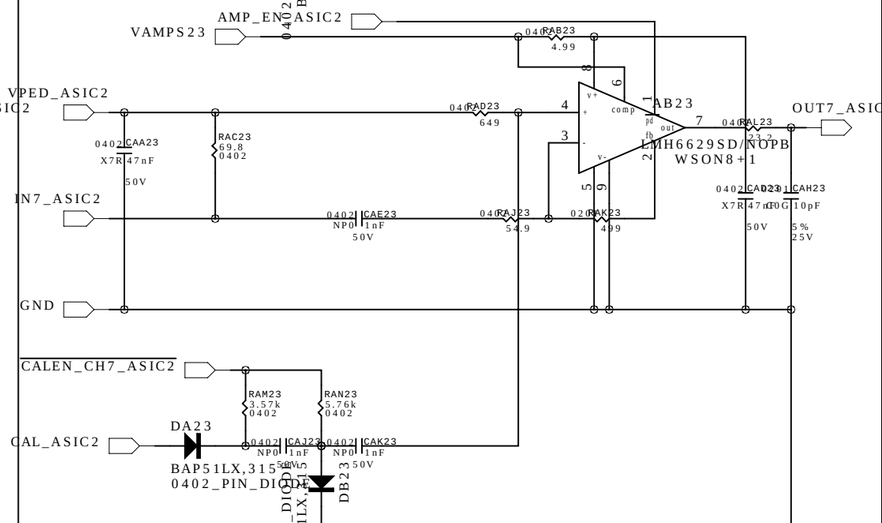












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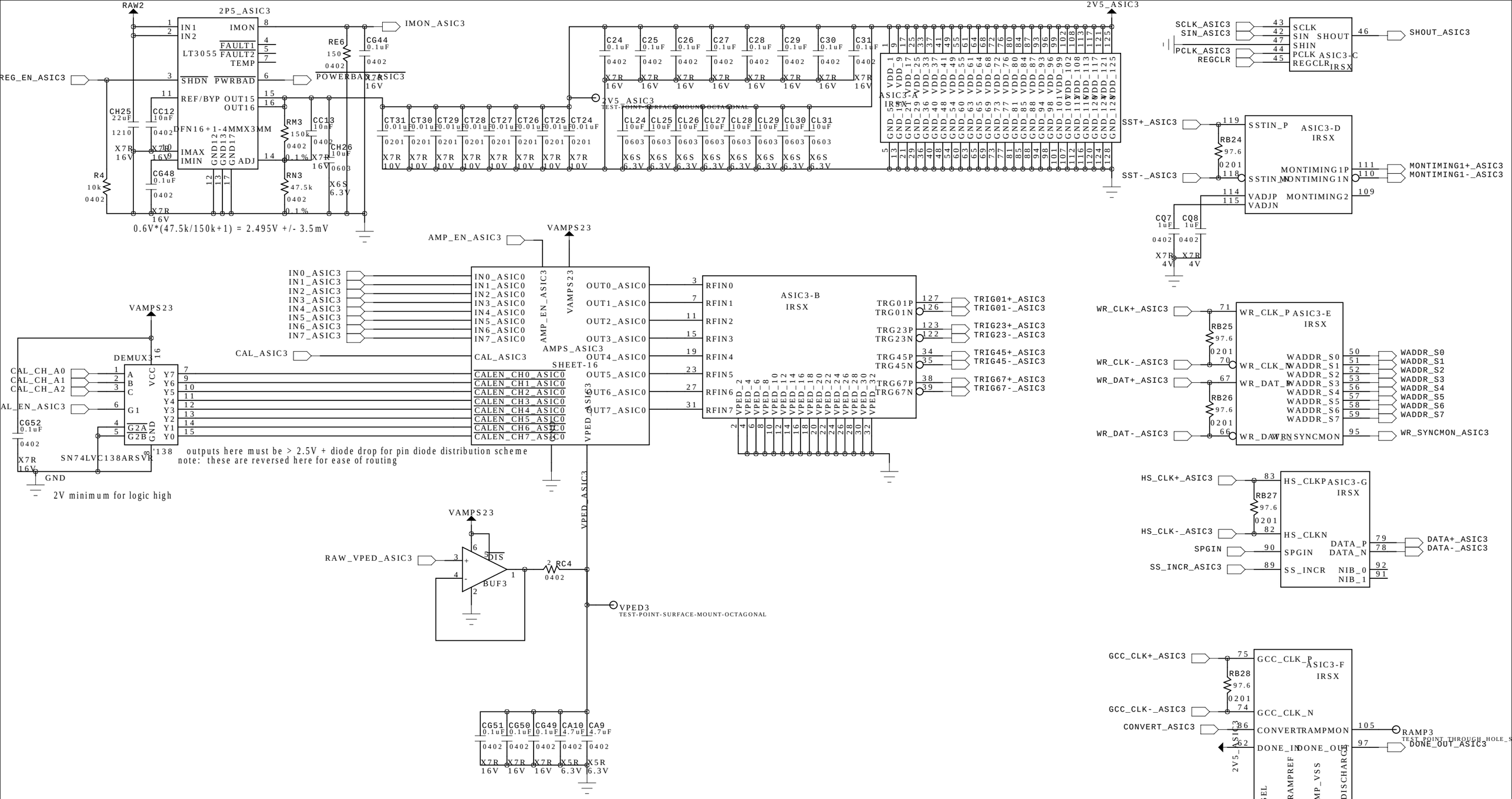
IDLAB design #:	IDL_18_001
circuit design:	MZA, GV, KAN, GSV
PCB design:	MZA, GV
sheet #:	14 of 16
sheet description:	AMPS_ASIC2
date last modified:	2017-06-19



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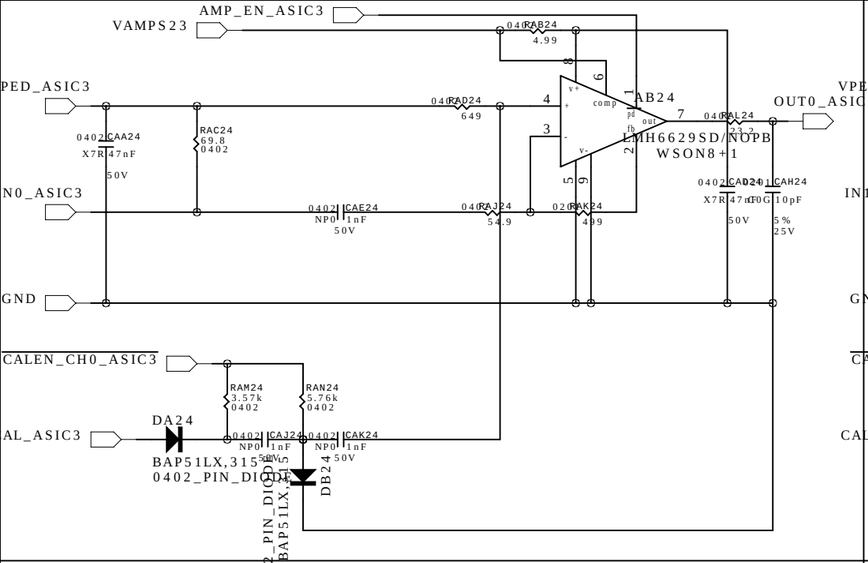
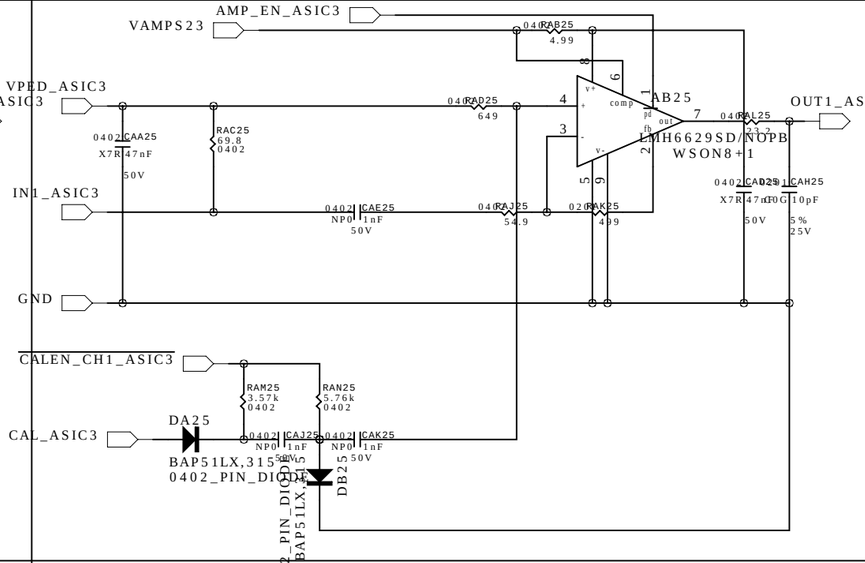
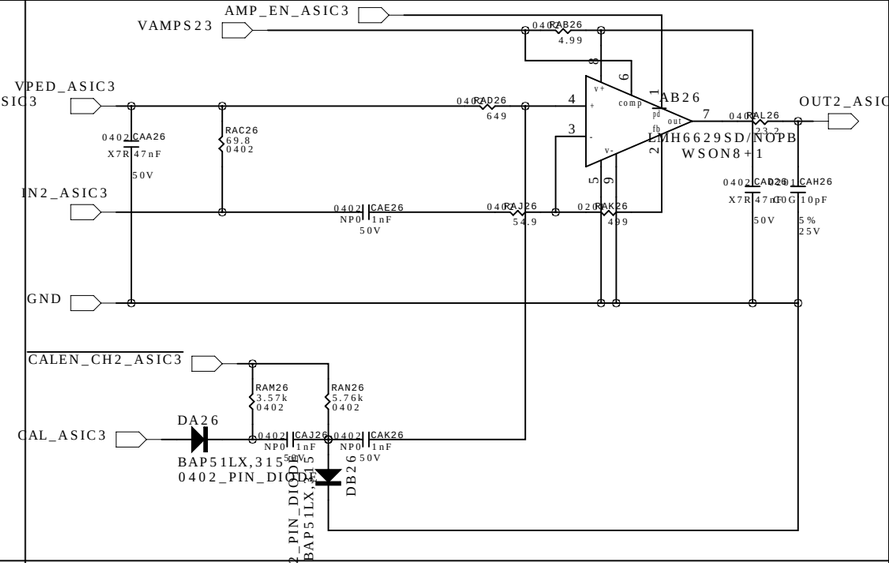
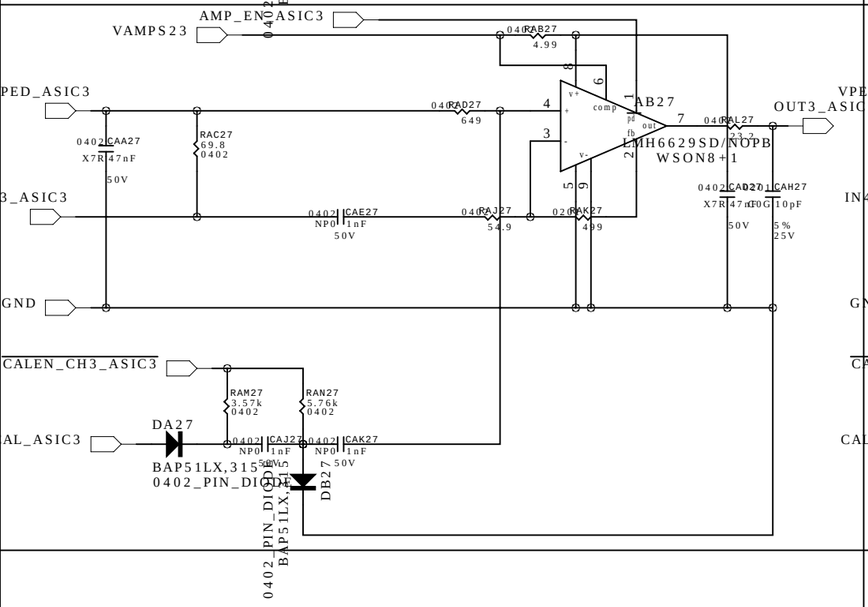
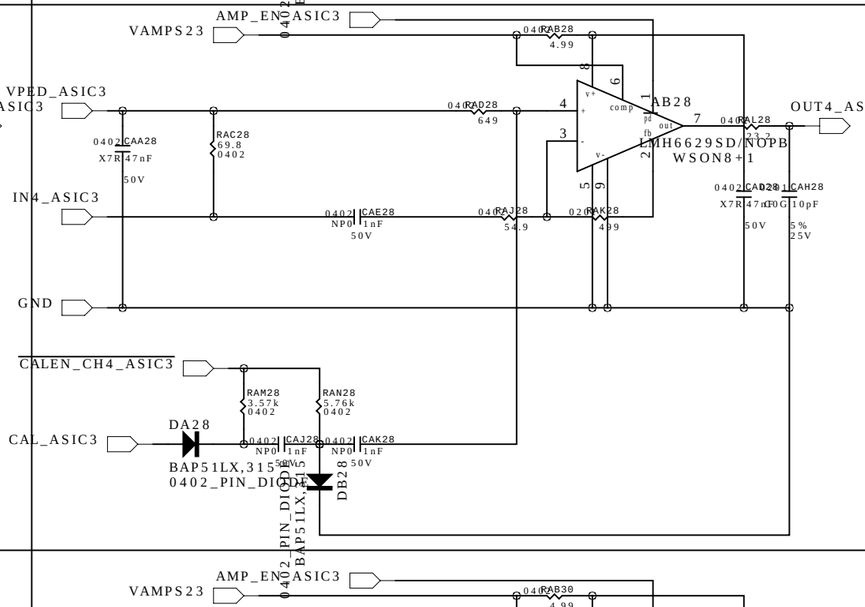
IDLAB design #:	IDL_18_001
circuit design:	MZA, GV, KAN, GSV
PCB design:	MZA, GV
sheet #:	15 of 16
sheet description:	ASIC3
date last modified:	2017-06-19

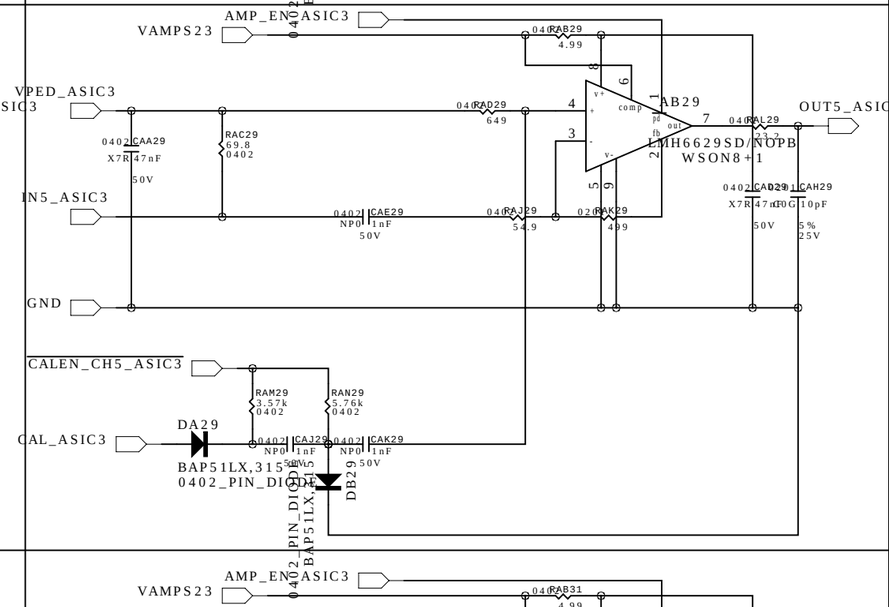


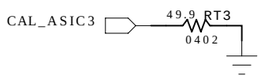


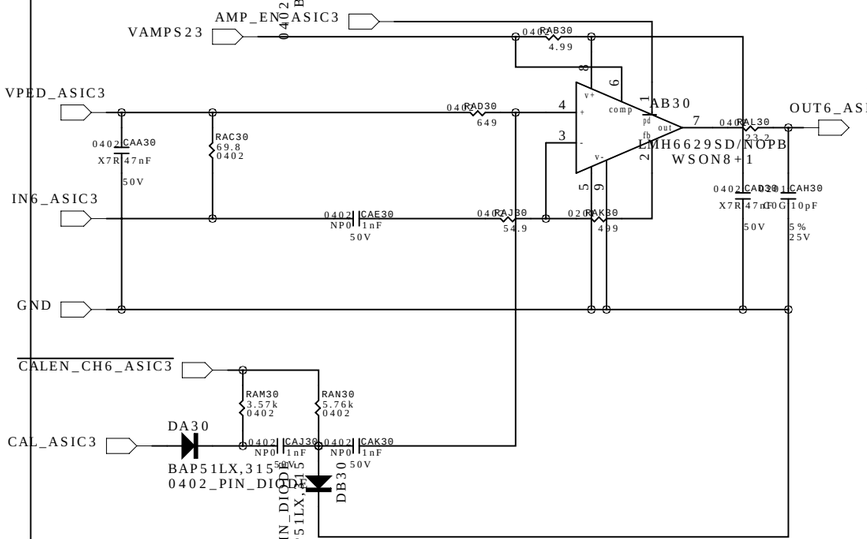


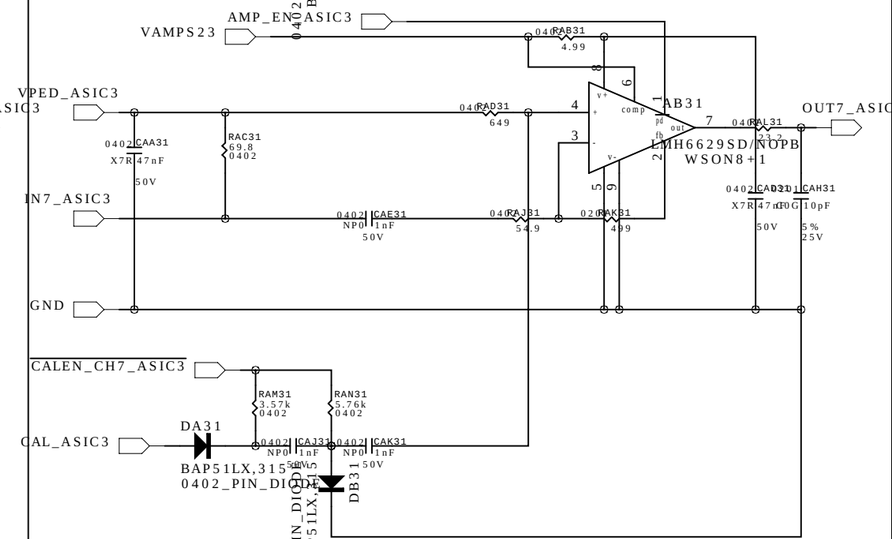












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