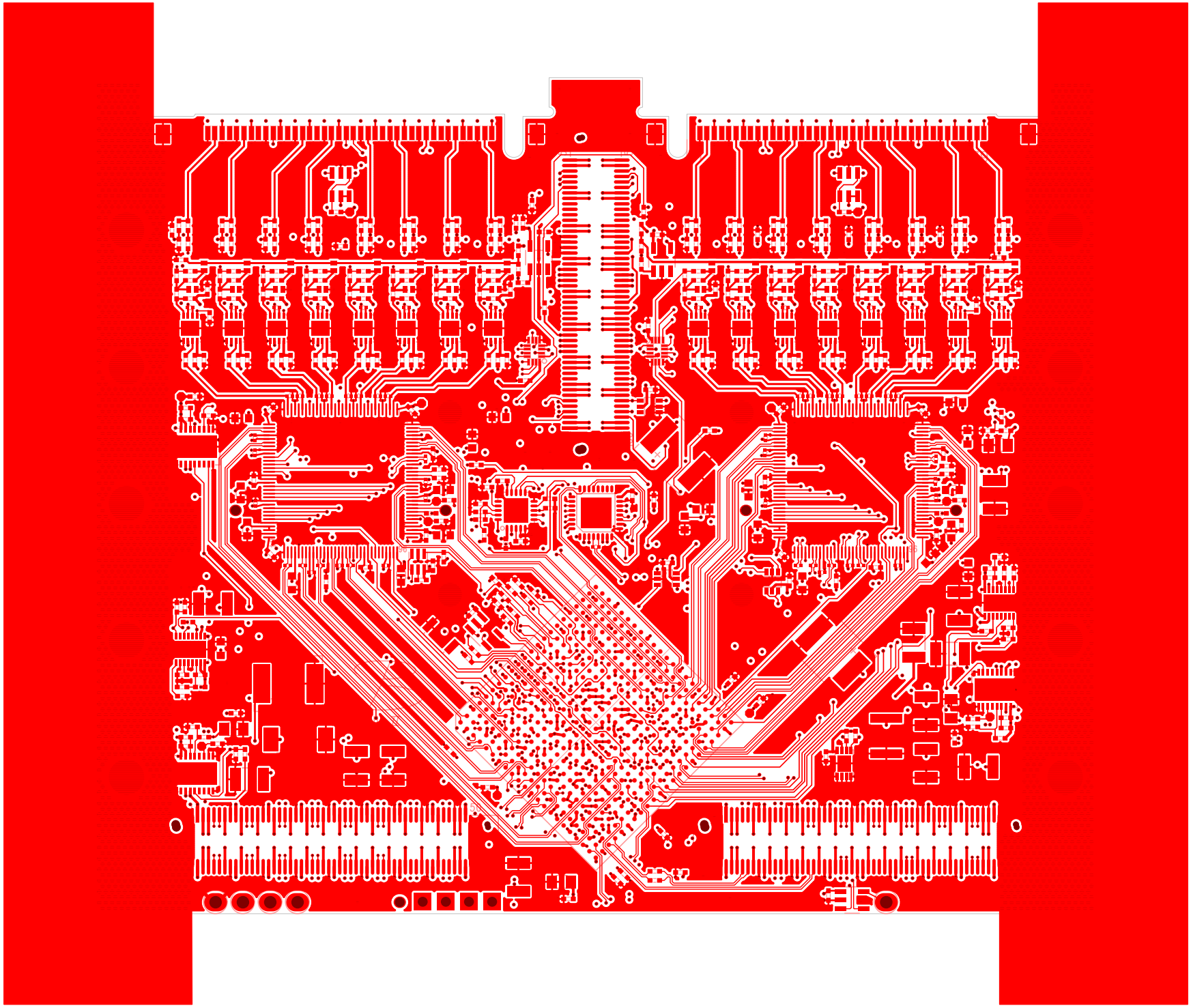
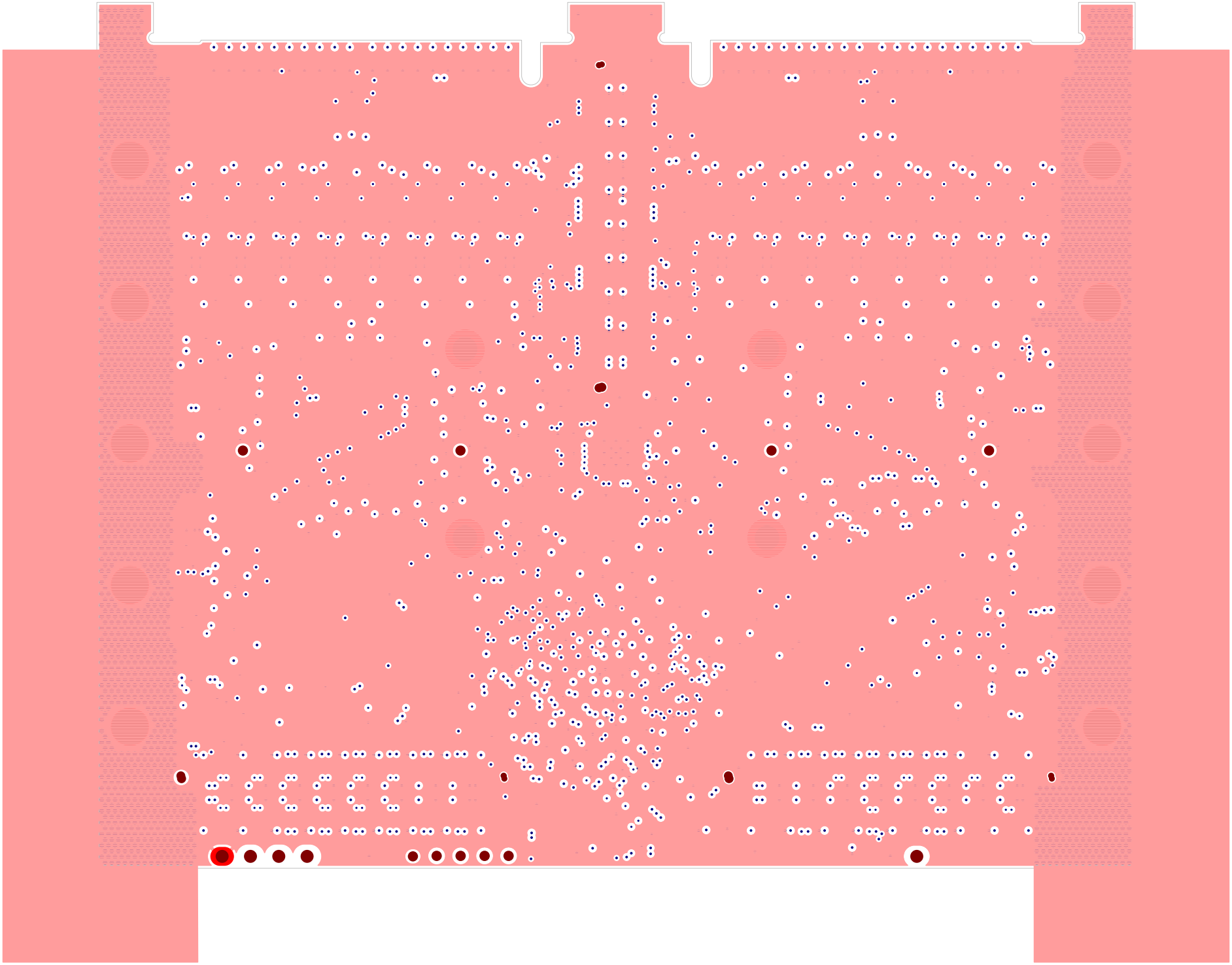
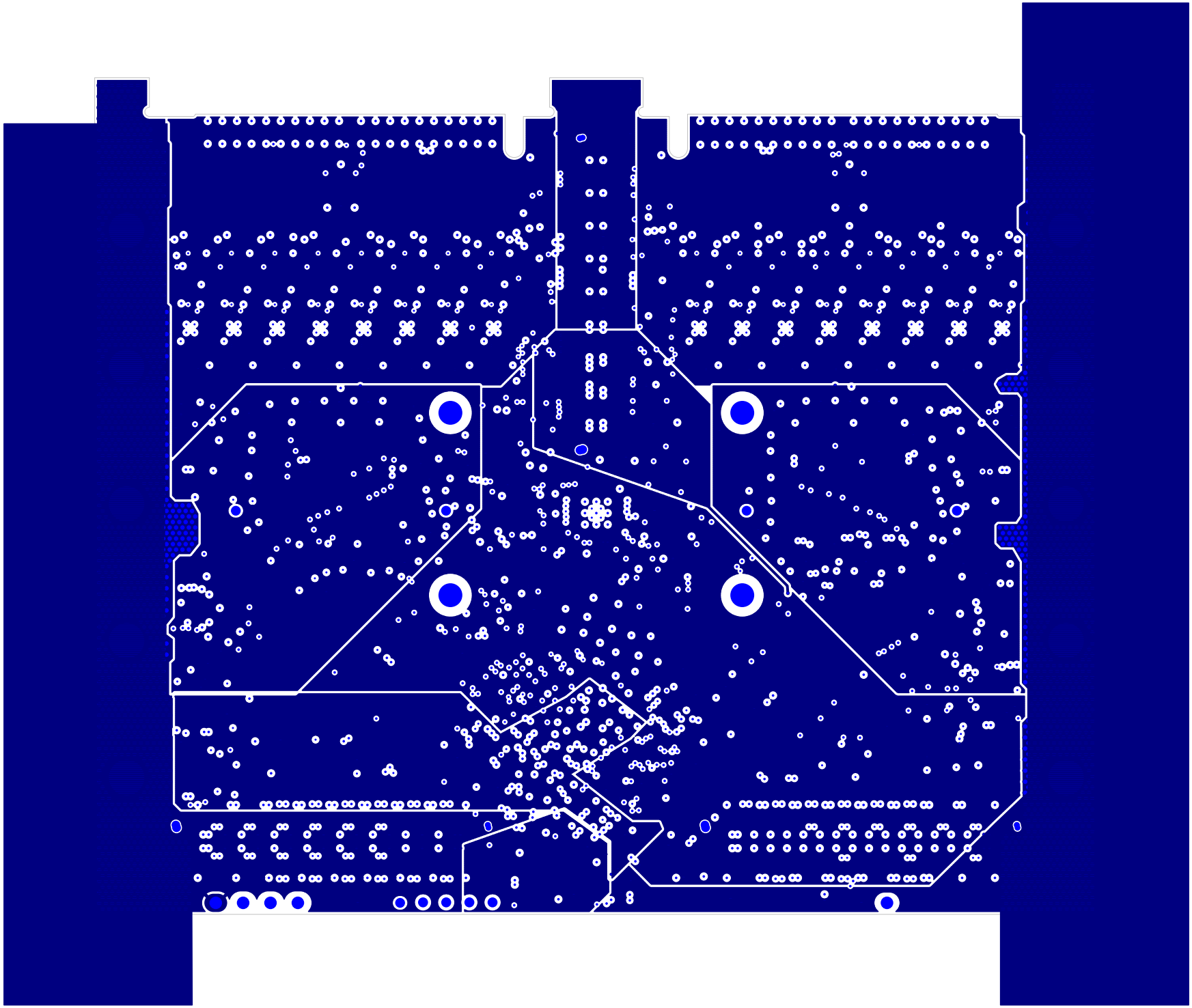


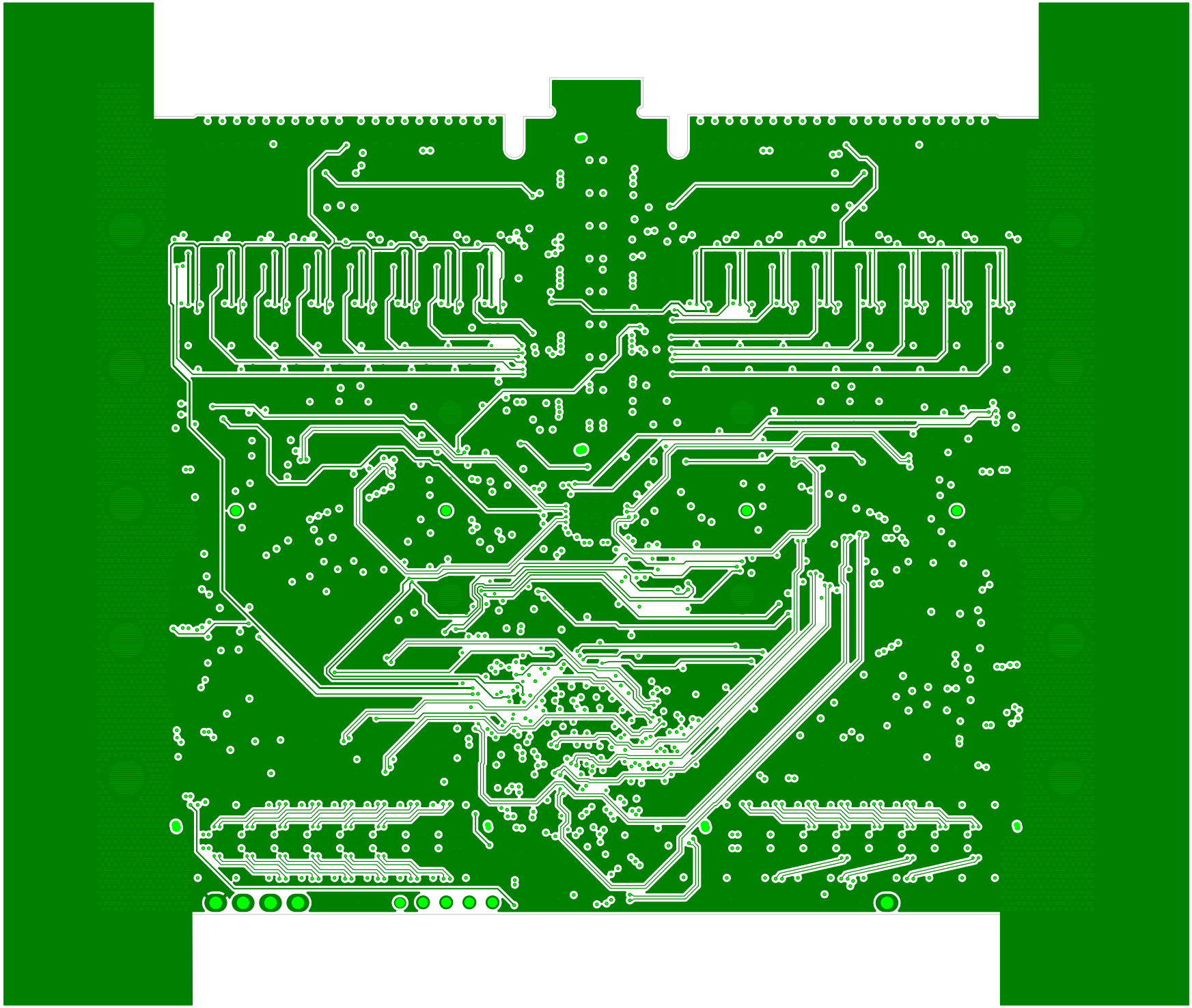
top



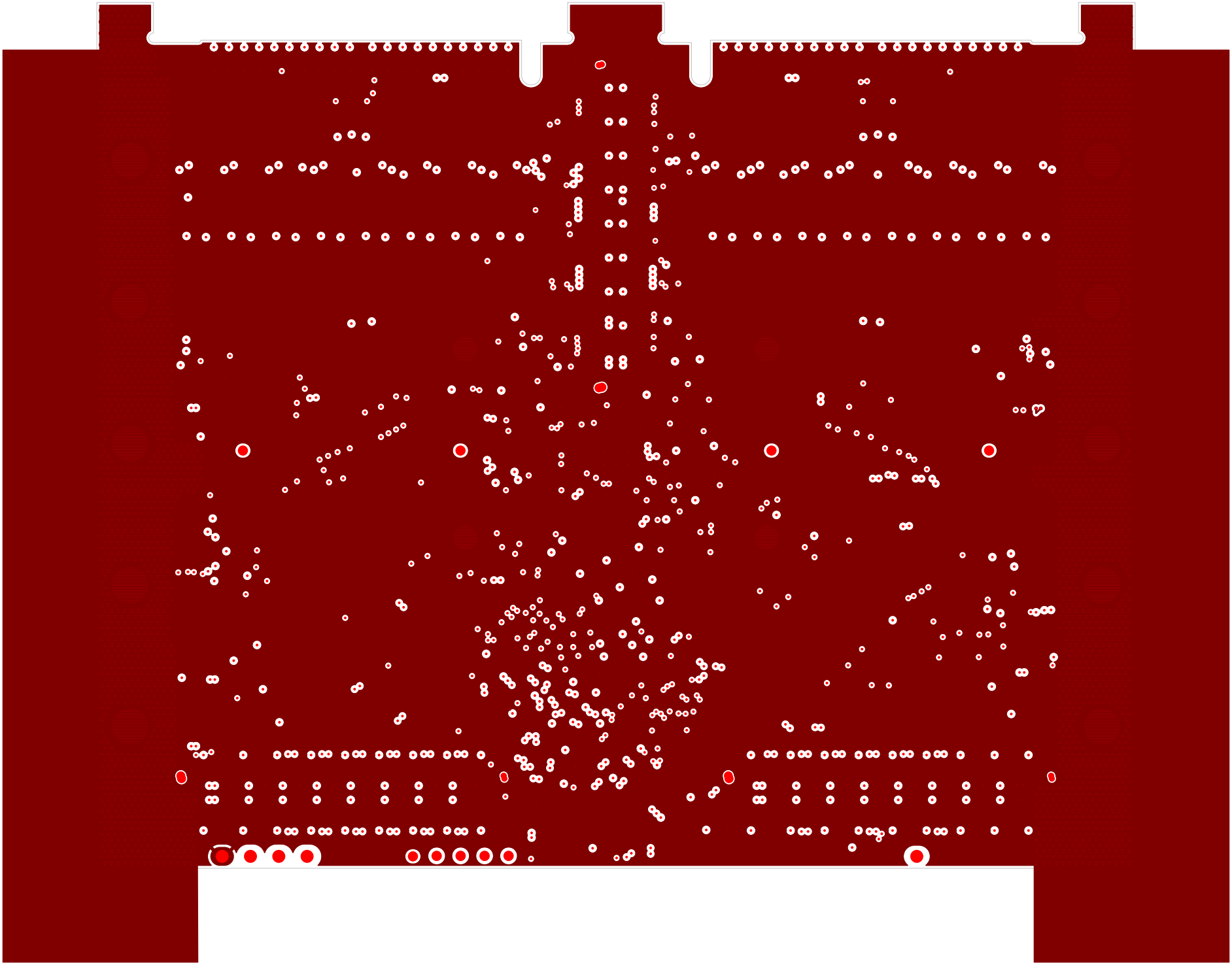
02-GND



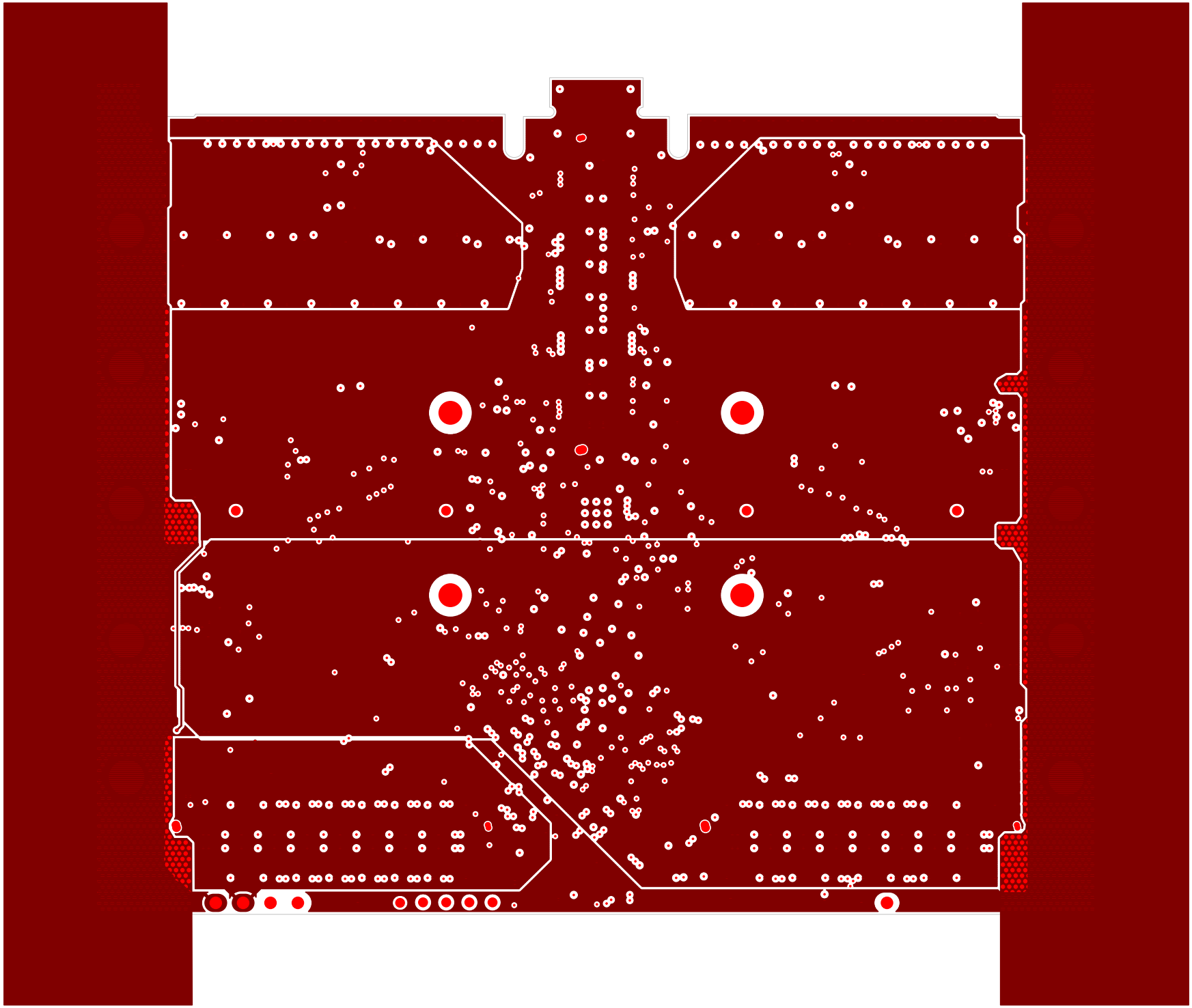
03-power



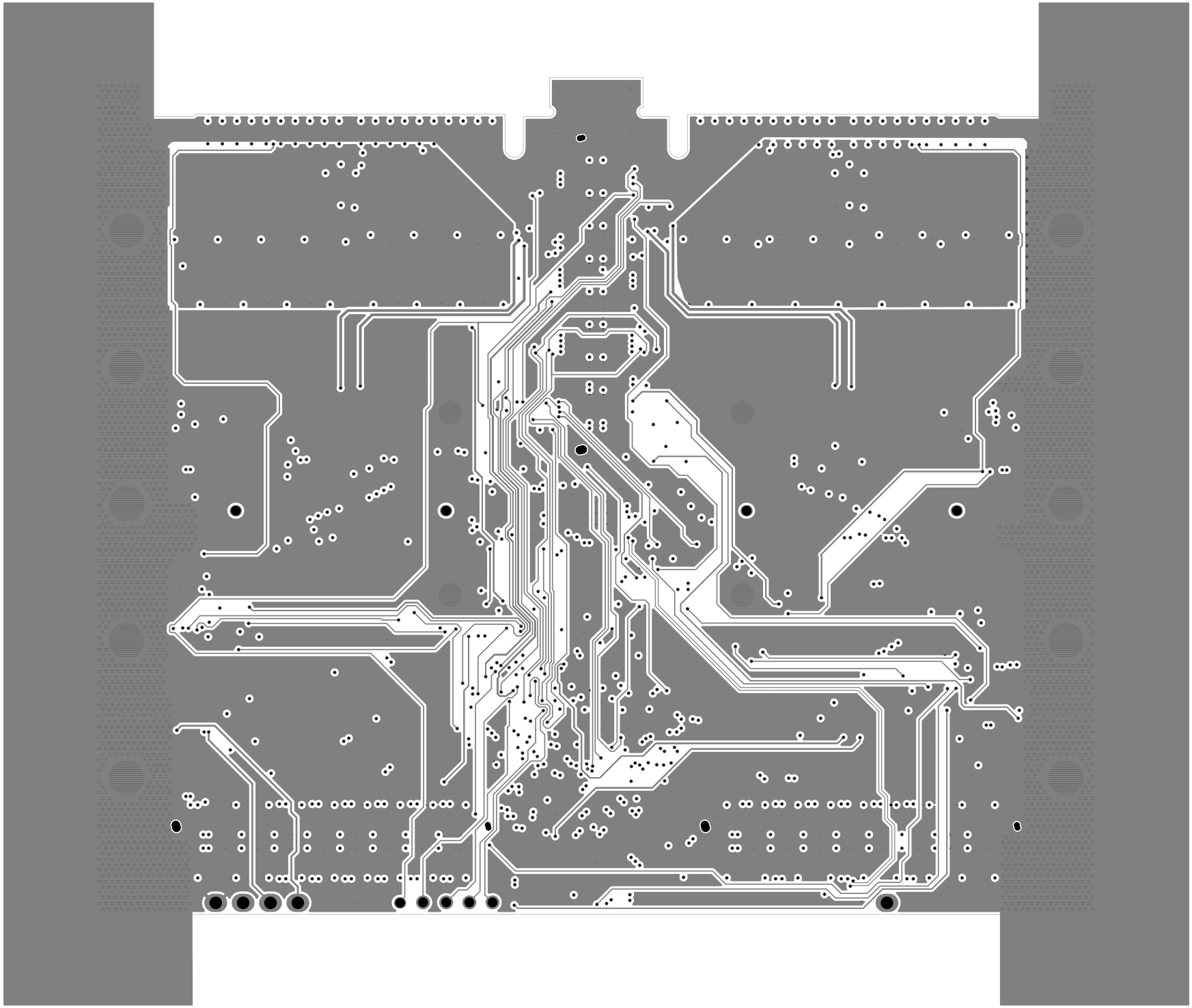
04-routing



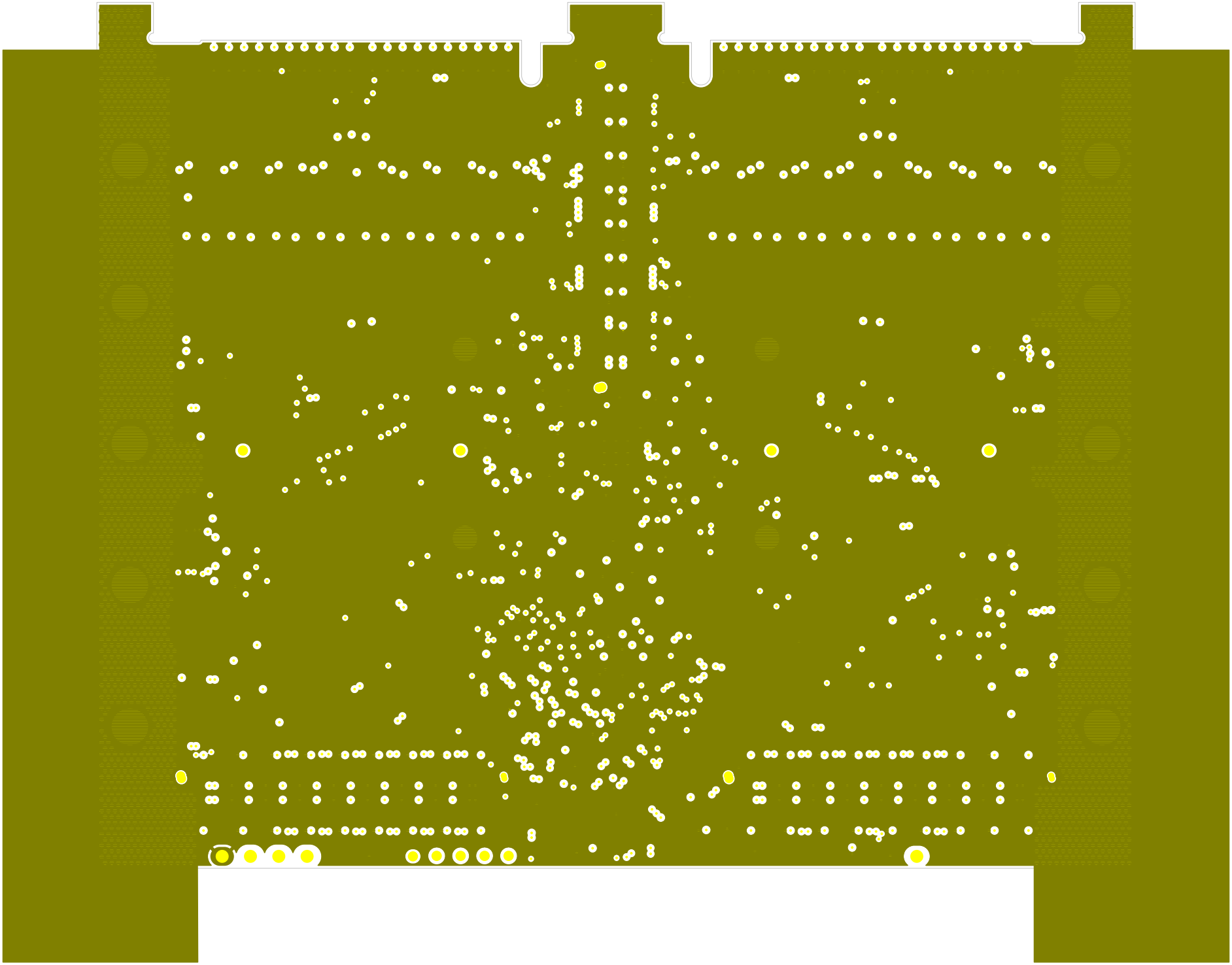
05-GND



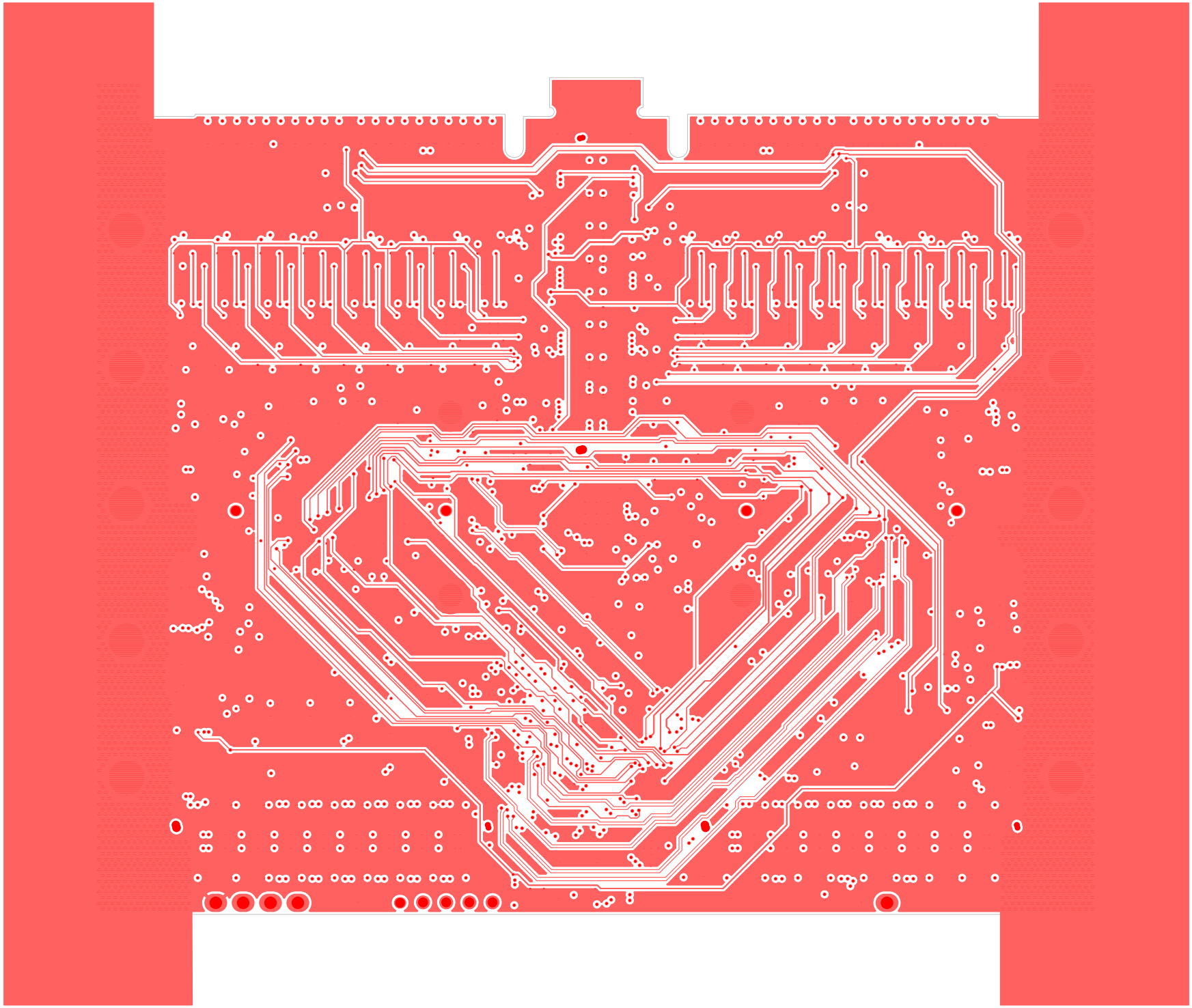
06-power



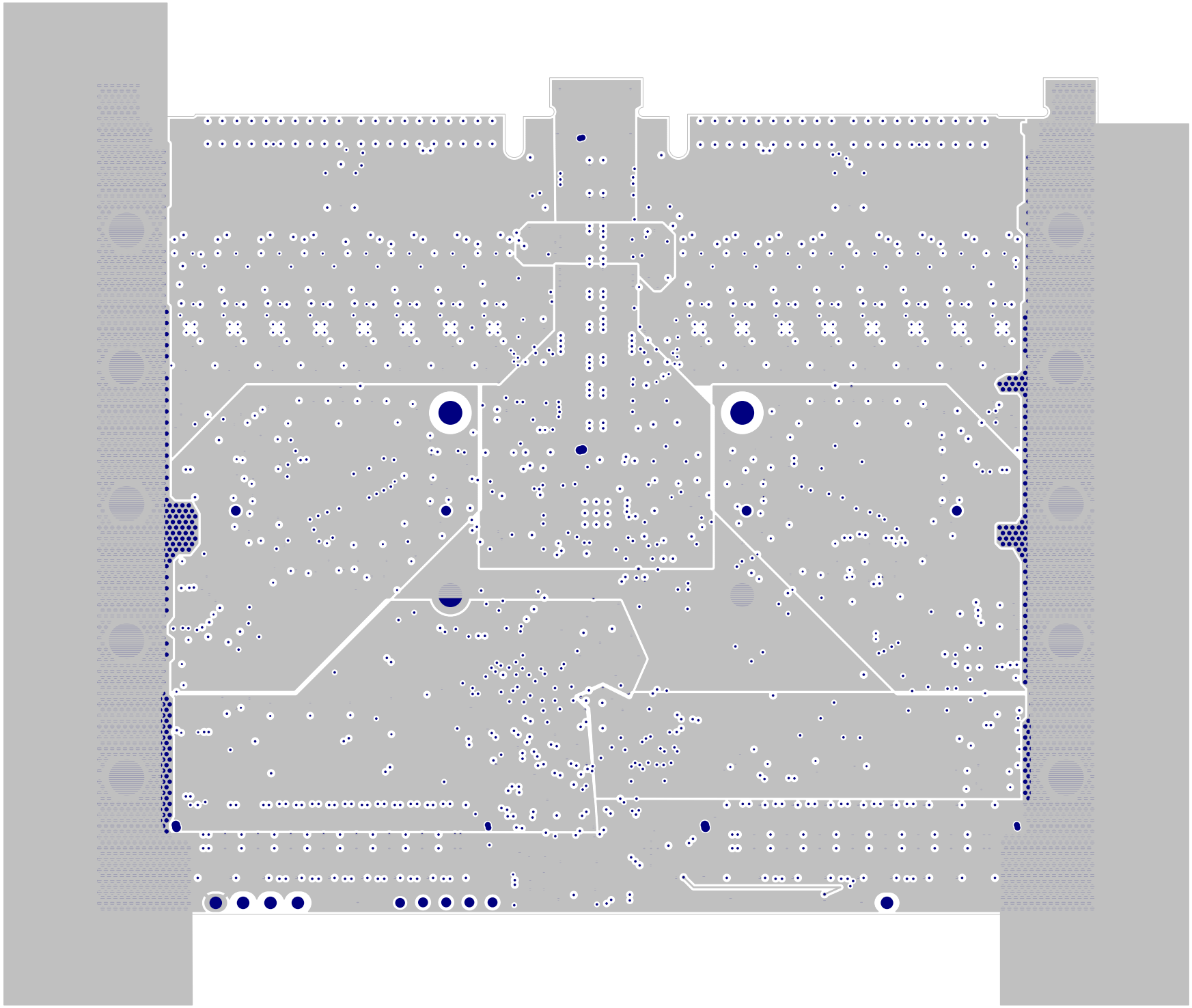
07-routing



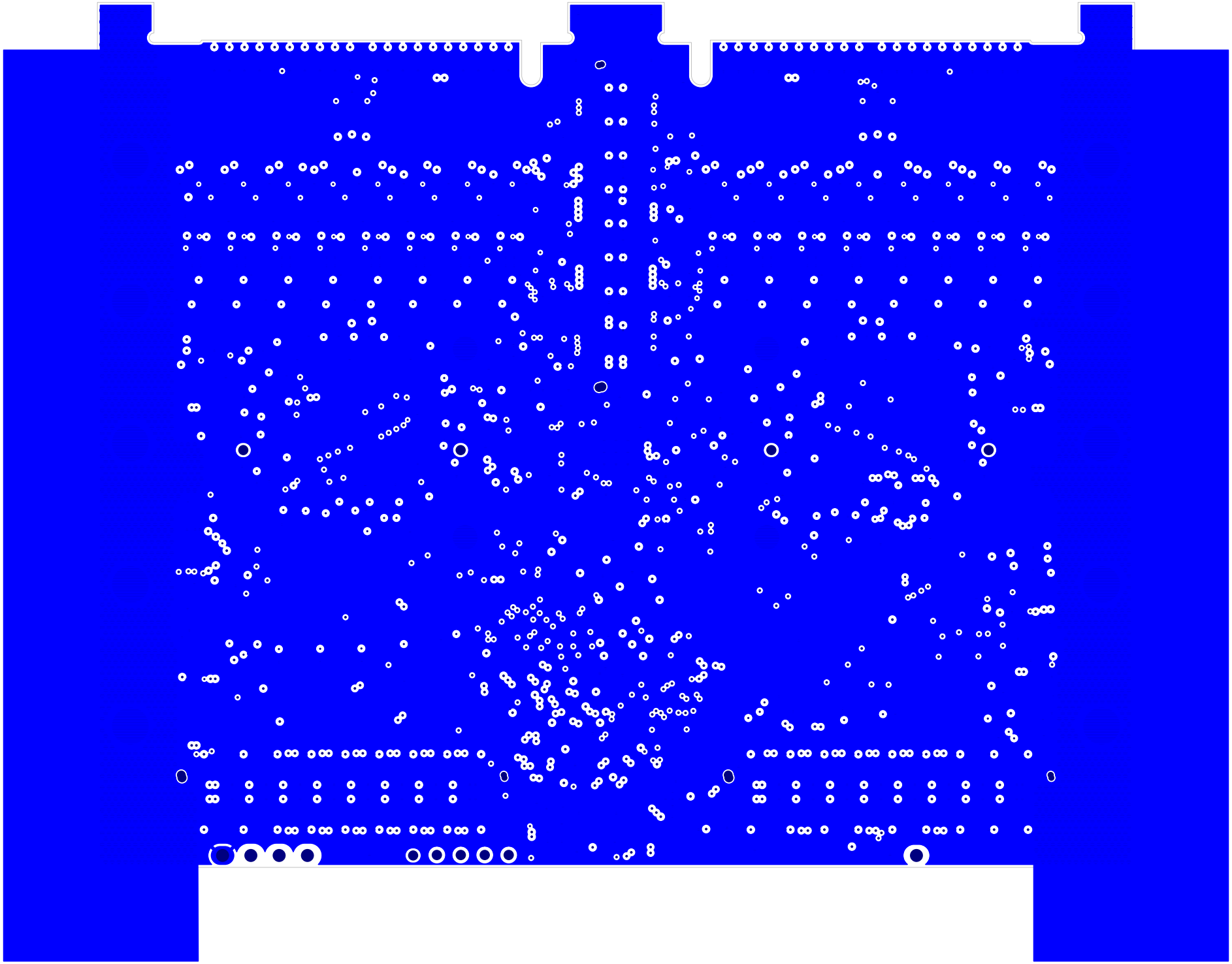
08-GND



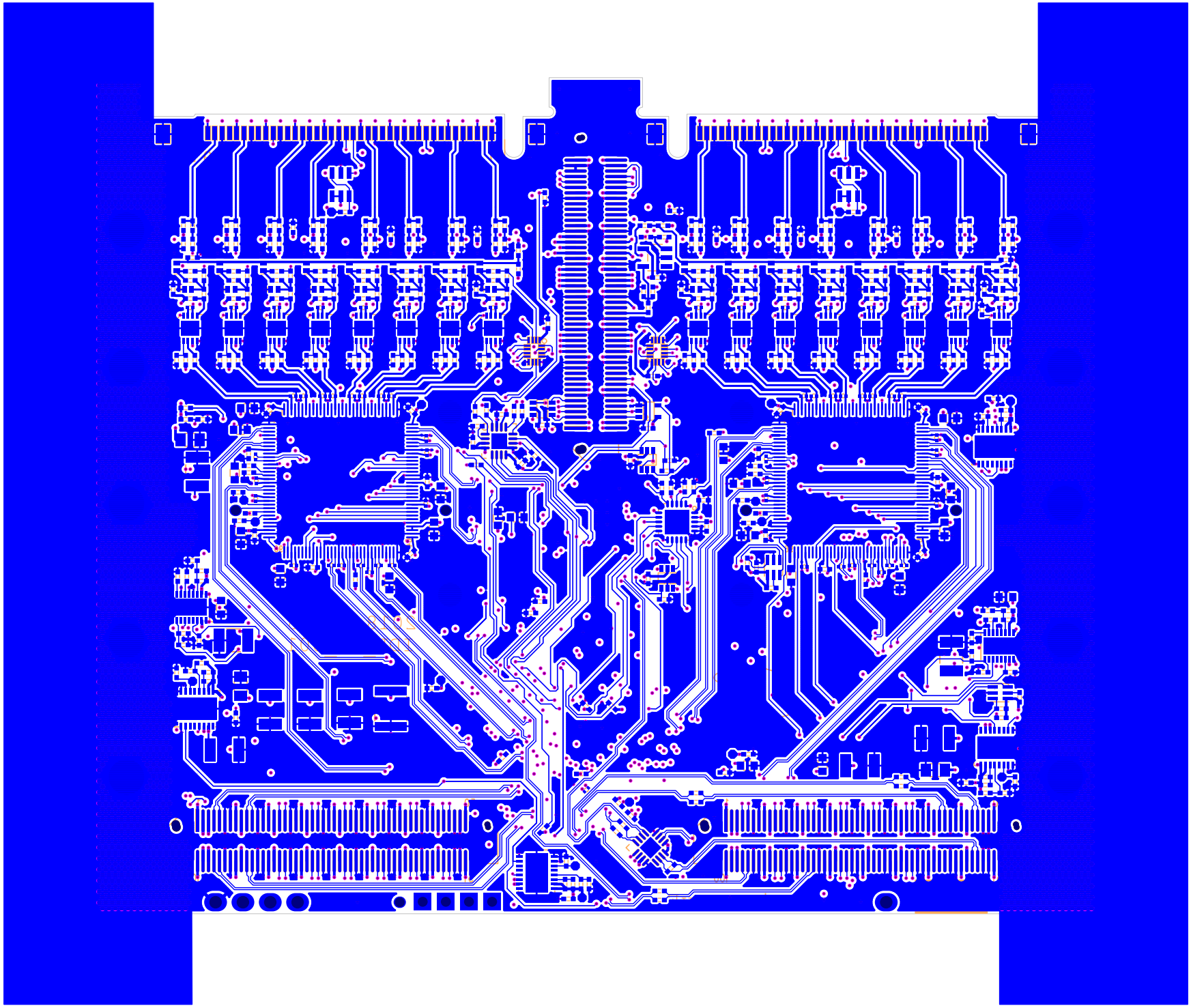
09-routing



10-power



11-GND



bottom

board material = FR4 180 C Tg
overall board dimensions = 110 mm * 91.75 mm
soldermask color = red
silkscreen color = white
plating = ENIG
plated edges:  left and right (see file edge-plating.gerber)
left/right edge plating should connect electrically to all inner layers
all plated holes plated to at least 1 mil copper wall thickness, or more if possible
**via-in-PAD plating on top and bottom layers (see files top-via-in-pad.gerber and bottom-via-in-pad.gerber for locations)**
**board to be fabricated using sequential lamination (layers 1-4, layers 9-12, then entire board)**

dielectric thicknesses:

| | |
|---|---|
| prepreg | 0.127 mm |
| core | 0.080 mm |
| prepreg | 0.152 mm |
| prepreg | 0.152 mm |
| core | 0.080 mm |
| prepreg | 0.051 mm |
| core | 0.080 mm |
| prepreg | 0.152 mm |
| prepreg | 0.152 mm |
| core | 0.080 mm |
| prepreg | 0.127 mm |

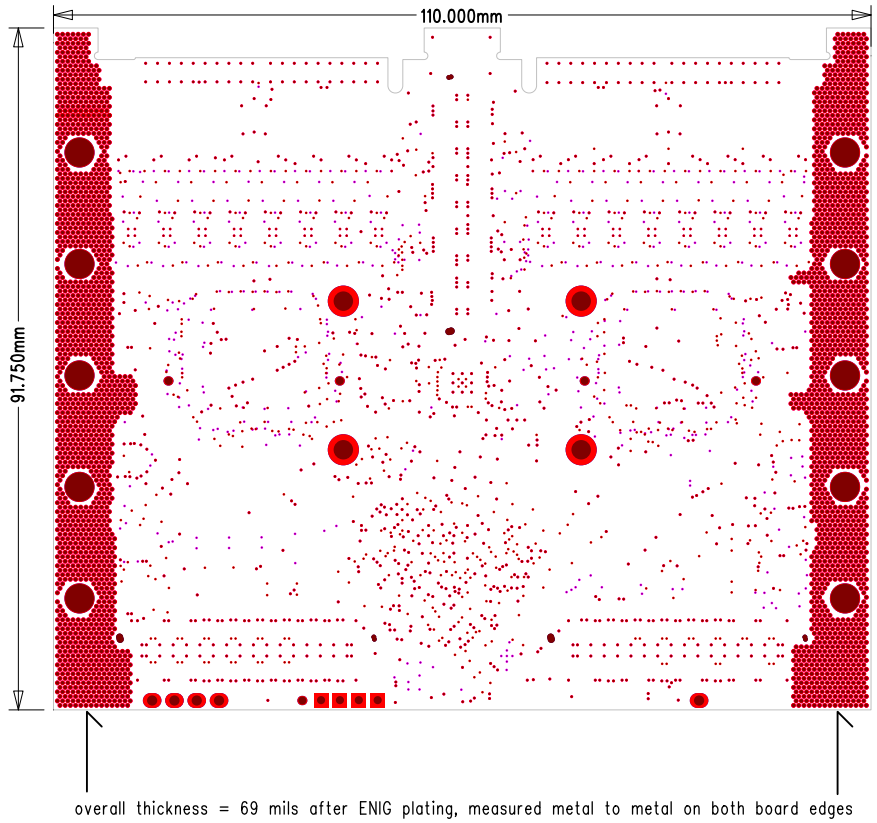
copper gerber layers:
top-copper.GTL - copper foil (1 oz finished)
2-copper.G2L - copper (2 oz)
3-copper.G3L - copper (2 oz)
4-copper.G4L - copper foil (0.5 oz finished)
5-copper.G5L - copper (1 oz)
6-copper.G6L - copper (1 oz)
7-copper.G7L - copper (1 oz)
8-copper.G8L - copper (1 oz)
9-copper.G9L - copper foil (0.5 oz finished)
10-copper.G10L - copper (2 oz)
11-copper.G11L - copper (2 oz)
bottom-copper.GBL - copper foil (1 oz finished)

silkscreen gerber layers:
top-silkscreen.GTO
bottom-silkscreen.GBO

soldermask gerber layers:
top-soldermask.GTS
bottom-soldermask.GBS

other gerber layers:
board-outline.GKO - showing outline of board
drill-drawing.gerber - this file
edge-plating.gerber - showing where edge plating should be added (see note to left
top-via-in-pad.gerber
bottom-via-in-pad.gerber
soldermask-plugged-vias.top.gerber - shows location where we want vias plugged with soldermask

drill files:
drill-through.DRL - plated through holes/vias
drill-01-04.DRL - blind vias (layers 1 to 4 inclusive)
drill-09-12.DRL - blind vias (layers 9 to 12 inclusive)
drill-unplated-pins.top.DRL - unplated blind holes (see note below)
drill-unplated-pins.bottom.DRL - unplated blind holes (see note below)




* controlled-depth drill on bottom side drilled to 0.8763 mm depth
* controlled-depth drill on top side drilled to 0.8763 mm depth
* controlled-depth drill on bottom side drilled to 0.8763 mm depth
* controlled-depth drill on top side drilled to 0.8763 mm depth

# drill drawing