progress / timeline:

http://www.phys.hawaii.edu/~mza/PCB/SCROD/index.html

2013-11 (mechanical mockup):
2014- fabricated 20 boards
2014- assembled 4 boards (2 sans FPGA)
2014- assembled 12 more boards
2014-12-23 started on SCROD revB2 (see SCROD revB schematic for older notes)

things done for SCROD revB2:
- change R40 to DNI and R41 to 10k; DNI R39 and Q30; install 0603 0 Ohm from G to D of Q30; this changes the polarity of the signal going to the carrier
- add 0.1uF cap to DDR_VREF0 and DDR_VREF1 (could potentially throw down a cap for two of the resistors RL8-11...)
- disable 4V regulator unless all three RAW voltages are present; or just add pull-down to the shutdown pin
- wire QSPI RESET pins to the PS_AND_PL_ARE_POWERED signal
- add decoupling caps near LVDS and FFs feeding PS_CLOCK input
- wire reset_clock_divider signal to a PL pin to synchronize clocks (AG24)
- change VCCO for all HR banks to 2.5V
- add bulk capacitance on input lines (tantalum E-case 16V)
- maybe add a way to disable the cal signal from propagating - turning off the 4v0 regulator does this
- tie the oscillator enable to the clock_select line on the fanout (checked this by removing RC17 on SCROD revB #010 and jumpering to clock_select)
- could remove bypass resistor from JTAG chain (one that skips SCROD in the chain)
- add capacitance near LPDDR2 ram (on 2 voltages)
- add silkscreen for J1 (a-d, and an a-d for J2)
- move test point for 4p0 to bottom side of board
- remove silkscreen arrow for 24MHz
- add BelleII logo?
- to keep the device reliable for 10 years, we might need a heatsink (ug865 page 65) to couple the die temperature to the board
- change MIO6 to be a pulldown (even if a software solution can be shown to work)
- remove PL reset button; the PS one should be named, "RESET"
- tie one pin of mgt cal resistor to 1.2V (ug476 page 191)
- change solder connection points for CLK_TRG/JTAG to nicomatic connectors, and move them to align with features on daughtercard with cat7 cable connections
- change outline of board to put vertical male positronic 7 pin dragonfly connector on board
- extend board outline and add mounting hole locations for cableway cover
- can use smaller pads for 0402, 0603 and 1210
- just install test points in the RAW voltages and ground, 4 different colors
- move existing temperature sensor near the thermal wall
- change humidity sensor to the SIP one
- add silkscreen for what the jumpers do
- add 6 niobium oxide 100uF caps, 2 to each raw voltage
- silkscreen outline for mmcx can be smaller
- maybe shrink boss holes for 100 pin connectors? take from carrier revE but change part # to SV5
- put FMC mgt clock into 111 and a new diff 125 MHz osc into 112 and put the mgtclk from carrier to 112 - this will require firmware changes for FMC card firmware (moot, as we are not populating this connector)
- remove GTX clock coming from fabric; consolidate all mgt links into quads 111 and 112 - this will require firmware changes
- add rectangle for board #
- JTAG connector holes can be smaller
- double-check pins on SFP connectors against the standard (matches list on wikipedia 2015-03-13, except for RateSelect pin which is NC in our decal)
- check the voltage ratings and capacitance over temperature for the input/output caps for all the voltage regulators
- change reference designators on R, C so we have contiguous lists (RC1-12, etc); consolidate letters for parts with few instances
- move DATA_DISABLE and DATA_RX_LOS to a HR bank (the bank they were on is now a 2.5V bank)
- removed cap from CLOCK_SELECT line; replaced 50 Ohm terminators with a 100 Ohm terminator for the DC-coupled oscillator
- changed R23 from a pullup to a pulldown so by default the remote clock is selected at power-up (needed to drive PS_CLOCK so JTAG will function)
- added R39 pullup, marked as "do not install" for cases where there is a local oscillator present
- marking several other things "do not install:" USB, LEDs, oscillators, FMC, QSPI flash
- added surface-mount test points for current monitoring
- added copper cut-out to top layer under FPGA; added new layer for soldermask plugged vias on top
- brought North end of board in by 1mm
- connect the thermal_alarm signal to the FPGA
- wire LPC C2M and M2C clocks somewhere (just implementing FMC->fabric)
- 0.47uF cap on each FPGA bank voltage, as well as the three GTX supply lines
- connect the thermal_alarm signal to the reset_carriers signal
- removed FET driving init after power-up, as PS_POR is doing what we want anyway
- exchanged 18 pin nicomatic/harwin part for the 20 pin
- added surface-mount test points for RAW1+,2+,3+ and two power-supply sequencing signals
- connected another TJ pin to 3.3V
- changed diameters and annular rings of 4 cover plate mounting holes to match, and to be good for both M2.5 and 4-40, depending on what we pick for the cover plate
- connected another TJ pin to an FPGA pin (TJ_EXTRA1; on a HP bank)
- connected the last TJ pin to a test point (TJ_EXTRA2)
- added clearance from power/ground copper pours to vias, traces and smd pads
- changed protection diode to shunt to 4V0 instead of 3V3
- changed R40 to install (or jtag chain is not reliable)
- on second batch of assembled SCROD revB2's, RV5 is marked as "do not install"

outstanding questions:
- need to look into termination for the JTAG signals (ug470 page 60 says TCK must be terminated, but we have a distribution amplifier driving a copy of the raw signal)
- add signals down boardstack to indicate power-up status (this didn't get added to the carrier revE2 design, so ...)
- add dual 100 Ohm resistors (one to power, other to gnd) near LPDDR2 memory for address lines? (and maybe control lines too?)

reminders / notes:
- we will take the (wire-ORed) thermal_alarm signal and drive the reset_carriers signal from it, so if the boardstack goes overtemperature, all 4 carriers will get reset (which will immediately drive the ASIC and AMP regulators into shutdown)

capacitors:

C =	0.47	uF	0402	10V	X5R 10%
CA =	4.7	uF	0402	6.3V	X5R 20%
CB =	47	uF	1812	10V	X5R 10%
CC =	10	nF	0402	16V	X7R 10%
CD =	100	uF	1210	6.3V	X5R 20%
CG =	0.1	uF	0402	16V	X7R 10%
CH =	10	uF	0603	16V	X6S 20%
CJ =	270	pF	0402	50V	NP0 5%
CK =	12	pF	0402	50V	NP0 5%
CM =	100	pF	0402	50V	NP0 5%
CN =	22	uF	0805	10V	X7S 20%
CP =	22	uF	1210	16V	X7R 10%
CQ =	100	uF	E niobium oxide 105C		
CR =	100	uF	E tantalum 125C		
CS =	680	uF	E tantalum 125C		

resistors:

all 0402 1% unless noted

R =	10k	
RB =	100	
RC =	196k	
RD =	60.4k	0.1%
RE =	121	
RF =	40.2k	
RG =	121k	
RH =	12k	
RJ =	16k	
RK =	7.150k	
RL =	1k	
RM =	196k	
RN =	61.9k	
RQ =	340k	
RR =	13.7k	
RS =	4.7k	
RT =	50	
RU =	7.5k	
RV =	1	1/6W
RW =	8.06k	
RY =	40.2	
RZ =	240	
RAA =	330	
RAB =	57.6k	
RAC =	16k	
RAF =	50	(1/2W 1206)
RAH =	174	
RAJ =	69.8	

layer stackup:
- 1.4 mils copper (top; components and routing)
- 3.15 mils
- 1.4 mils copper (ground plane)
- 8 mils
- 1.4 mils copper (routing)
- 8 mils
- 1.4 mils copper (ground plane)
- 3.15 mils
- 1.4 mils copper (power plane)
- 3.15 mils
- 1.4 mils copper (power plane)
- 3.15 mils
- 1.4 mils copper (power plane)
- 3.15 mils
- 1.4 mils copper (ground plane)
- 8 mils
- 1.4 mils copper (routing)
- 8 mils
- 1.4 mils copper (ground plane)
- 3.15 mils
- 1.4 mils copper (bottom; components and routing)

not doing this:
- change CAL fanout to use single mini-circuits ERA-2+ amplifier? (maybe?)

SCROD revB3:
- implement fabric->FMC clock link
- add test points for thermal_alarm and reset_carriers
- change RV5 to do not install

notes for end-user:
- RAW1 should be set to 1.87 V measured at the board (which is ~8.1 V at the other end of a 24 m long 18 AWG cable)
- RAW2 should be set to 3.15 V measured at the board (which is ~7.6 V at the other end of a 24 m long 16 AWG cable)
- RAW3 should be set to 4.33 V measured at the board (which is ~8.1 V at the other end of a 24 m long 20 AWG cable)

the 2mm jumpers on SCROD revB are closed=
- to run the board in Belle-II mode, all jumpers should be removed/open; see other sheets for more info on benchtop use

jumper settings:

J2 (when jumper present)		J1 (when jumper present)	
J2-A	PS MIO27 = 0	J1-A	PS disabled
J2-B	PL AE26 = 0	J1-B	PS waits for PL
J2-C	QSPI mode	J1-C	PL boots before PS
J2-D	LEDs enabled	J1-D	PL disabled

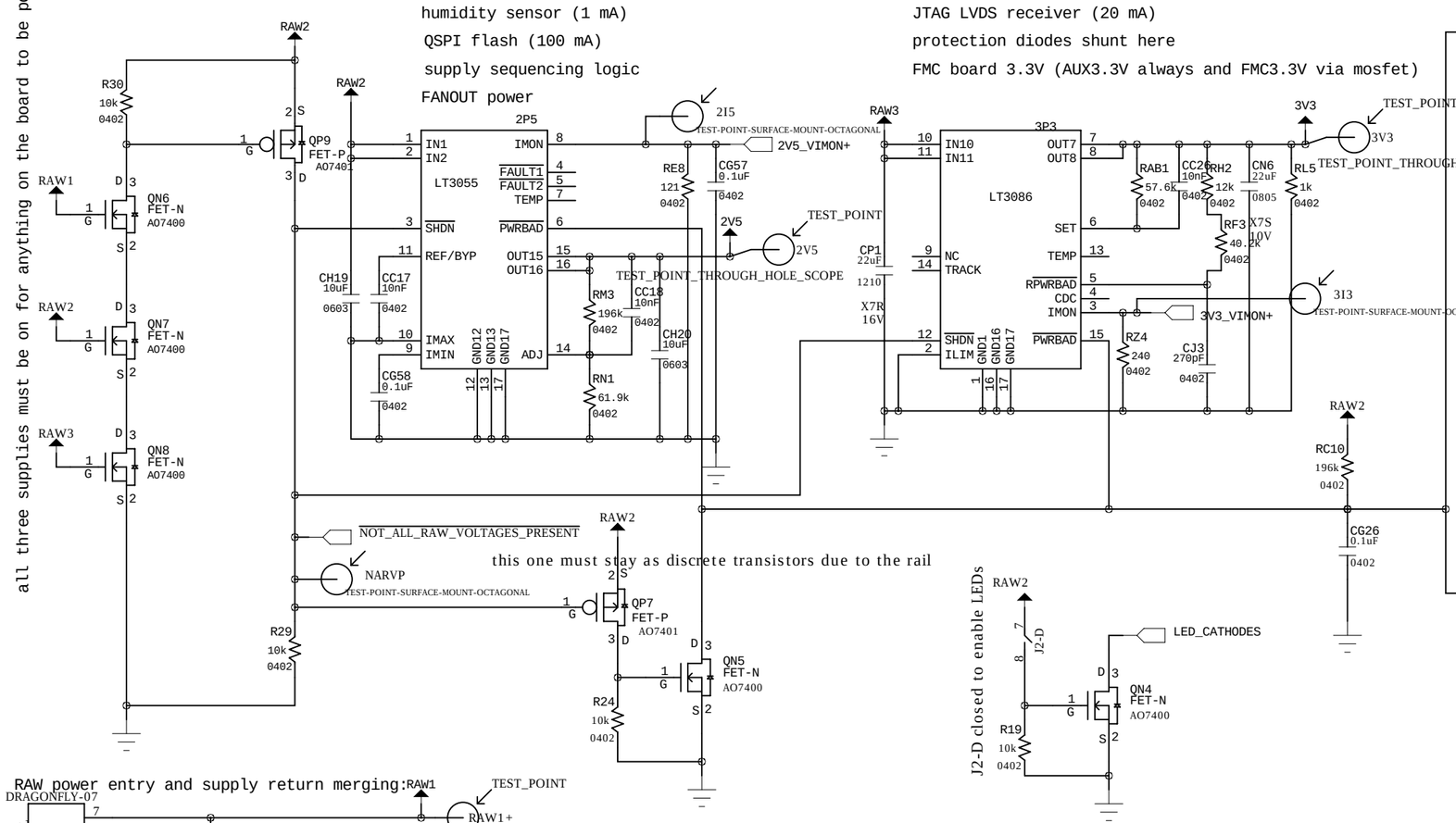
institution: University of Hawai'i at Manoa
High Energy Physics Group
Instrumentation Development Lab

title:	SCROD
revision:	B2
IDLAB design #:	IDL_15_007
circuit design:	MZA, KAN, GV, PO, JLB, KRO, BK, LM
PCB design:	MZA
sheet #:	1 of 11
sheet description:	NOTES
date last modified:	2016-01-11

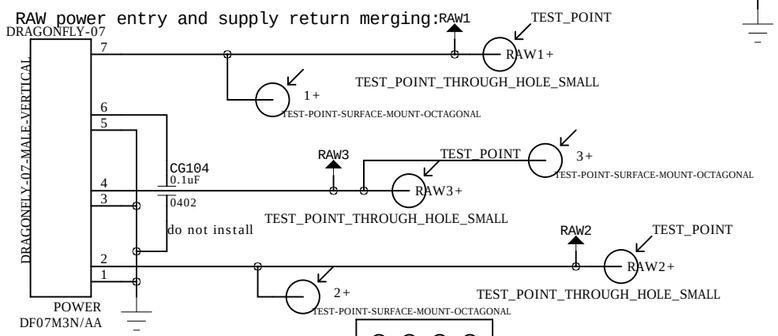
all three supplies must be on for anything on the board to be powered

this 2.5V regulator supplies:
oscillator (70 mA)
various pull-ups (1 mA)
humidity sensor (1 mA)
QSPI flash (100 mA)
supply sequencing logic
FANOUT power

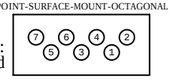
this 3.3V regulator supplies:
USB (12 mA)
QSPI flash (100 mA)
both fiber transceivers (470 mA)
JTAG LVDS receiver (20 mA)
protection diodes shunt here
FMC board 3.3V (AUX3.3V always and FMC3.3V via mosfet)



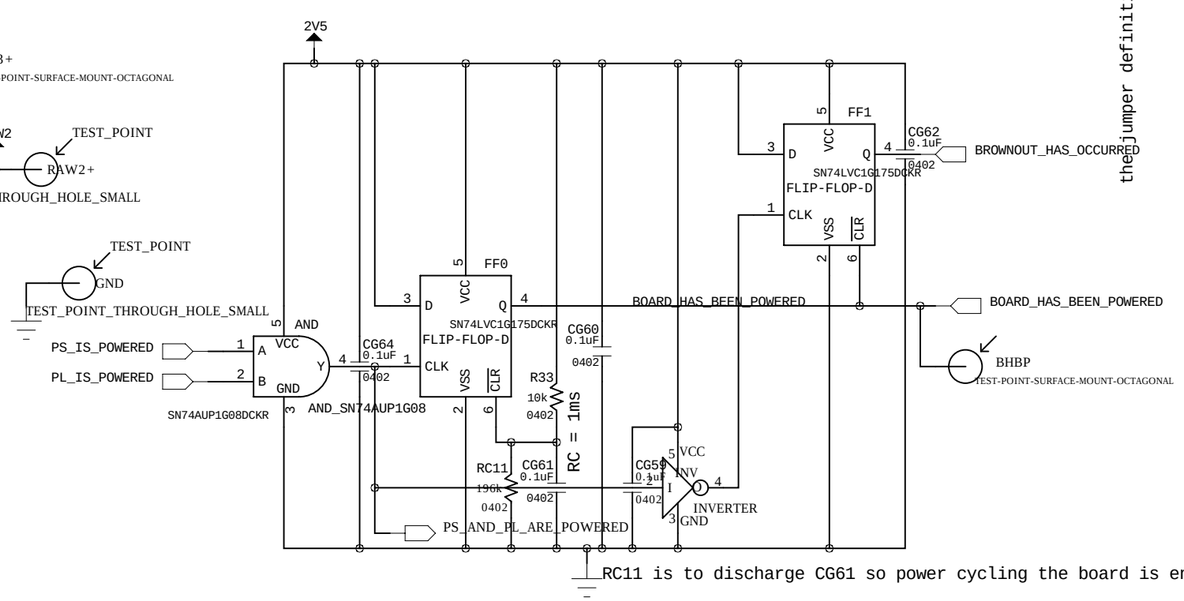
RAW power entry and supply return merging:



positronic dragonfly 7 pin connector:
as viewed from FPGA side of board



7 = RAW1+ 4 = RAW3+ 2 = RAW2+
5 = RAW1- 3 = RAW3- 1 = RAW2-



RC11 is to discharge CG61 so power cycling the board is enough to reset this flip-flop

PS_IS_POWERED	PL_IS_POWERED	PS_AND_PL_ARE_POWERED	$\overline{\text{INIT}}$
0	0	0	0
0	1	0	0
1	0	0	0
1	1	1	1

$\overline{\text{BOARD\_HAS\_BEEN\_POWERED}}$
1 for at least first 1 ms after 2V5 supply is stable
0 after the first time PS_AND_PL_ARE_POWERED is pulsed

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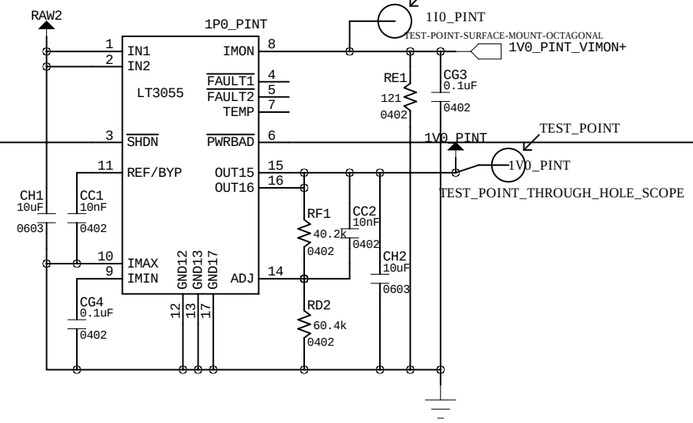
revision:	B2
IDLAB design #:	IDL_15_007
circuit design:	MZA, KAN, GV, PO, JLB, KRO, BK, LM
PCB design:	MZA
sheet #:	2 of 11
sheet description:	POWER_ENTRY_AND_SEQUENCING
date last modified:	2016-01-11

PS_SHOULD_POWER_UP

PINT = 1V; 122 mA quiescent + 70 mA @ power-on = 192 mA peak



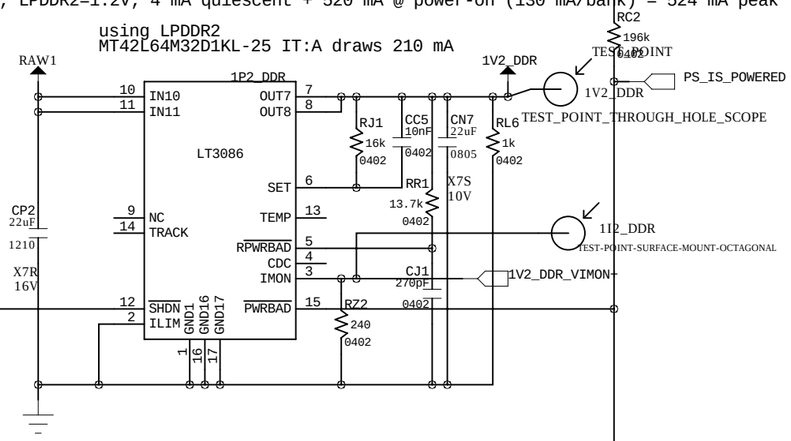
RC1
196k
0402

RC1 * CG5 = 20 ms

DBUF2-B
BUFFER-OPEN-DRAIN-SN74LVC2G07

DDR2=1.8V; DDR3=1.5V; LPDDR2=1.2V; 4 mA quiescent + 520 mA @ power-on (130 mA/bank) = 524 mA peak

using LPDDR2
MT42L64M32D1KL-25 IT:A draws 210 mA



DBUF2-C
BUFFER-OPEN-DRAIN-SN74LVC2G07

2V5

QP18
FET-P
AO7401
do not install

RL22
1k
0402
do not install

do not install
SML-P11MTT86
PS_INT_PLL_AUX

LED_CATHODES

RC2 * CG10 = 20 ms

2V5

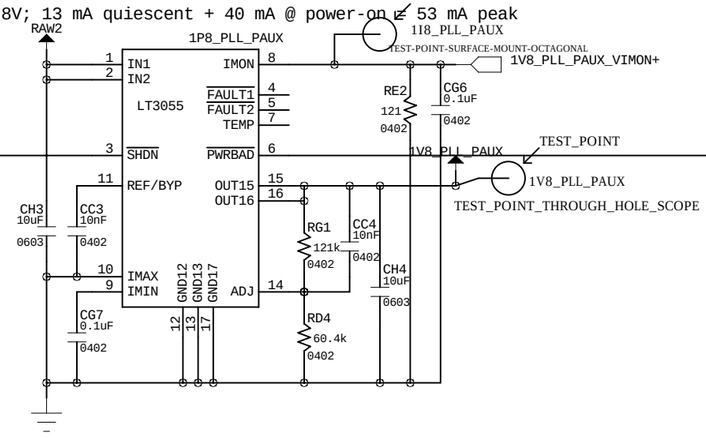
QP19
FET-P
AO7401
do not install

RL15
1k
0402
do not install

do not install
SML-P11MTT86
PS_DDR_VCCO

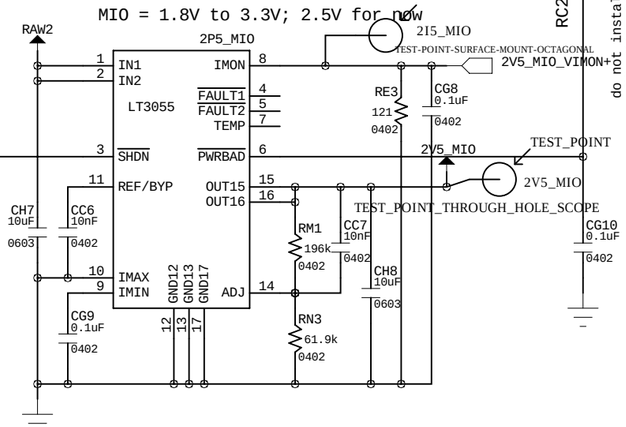
LED_CATHODES

PAUX = 1.8V; 13 mA quiescent + 40 mA @ power-on = 53 mA peak



CG5
0.1uF
0402

MIO = 1.8V to 3.3V; 2.5V for now



CG10
0.1uF
0402

2V5

DBUF2-A
BUFFER-OPEN-DRAIN-SN74LVC2G07

CG84
0.1uF
0402

total 8 stages of 20 ms RC filter for both PS and PL sequencing; LTspice simulation shows about 200 ms between power being applied and the PS_AND_PL_ARE_POWERED signal going high

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IDLAB design #:	IDL_15_007
circuit design:	MZA, KAN, GV, PO, JLB, KRO, BK, LM
PCB design:	MZA
sheet #:	3 of 11
sheet description:	PS_VOLTAGE_REGULATORS
date last modified:	2016-01-11

BRAM = 1V; 23 mA quiescent + 90 mA @ power-on = 113 mA peak

INT = 1V; 611 mA quiescent + 1400 mA @ power-on = 2011 mA peak

AUX = 1.8V; 131 mA quiescent + 60 mA @ power-on = 191 mA peak

AUXIO = 1.8V; 2 mA quiescent + 400 mA @ power-on = 402 mA peak

VCCO = 1.2V to 3.3V; 40 mA quiescent + 900 mA @ power-on = 940 mA peak
(for all HR and HP banks together)

can tie MCTVCCAUX to VCCAUX because QPLLs are unused (only true in non-zynq 7-series)
ug585 page 614 has details on selecting RAM (LPDDR2 seems best)

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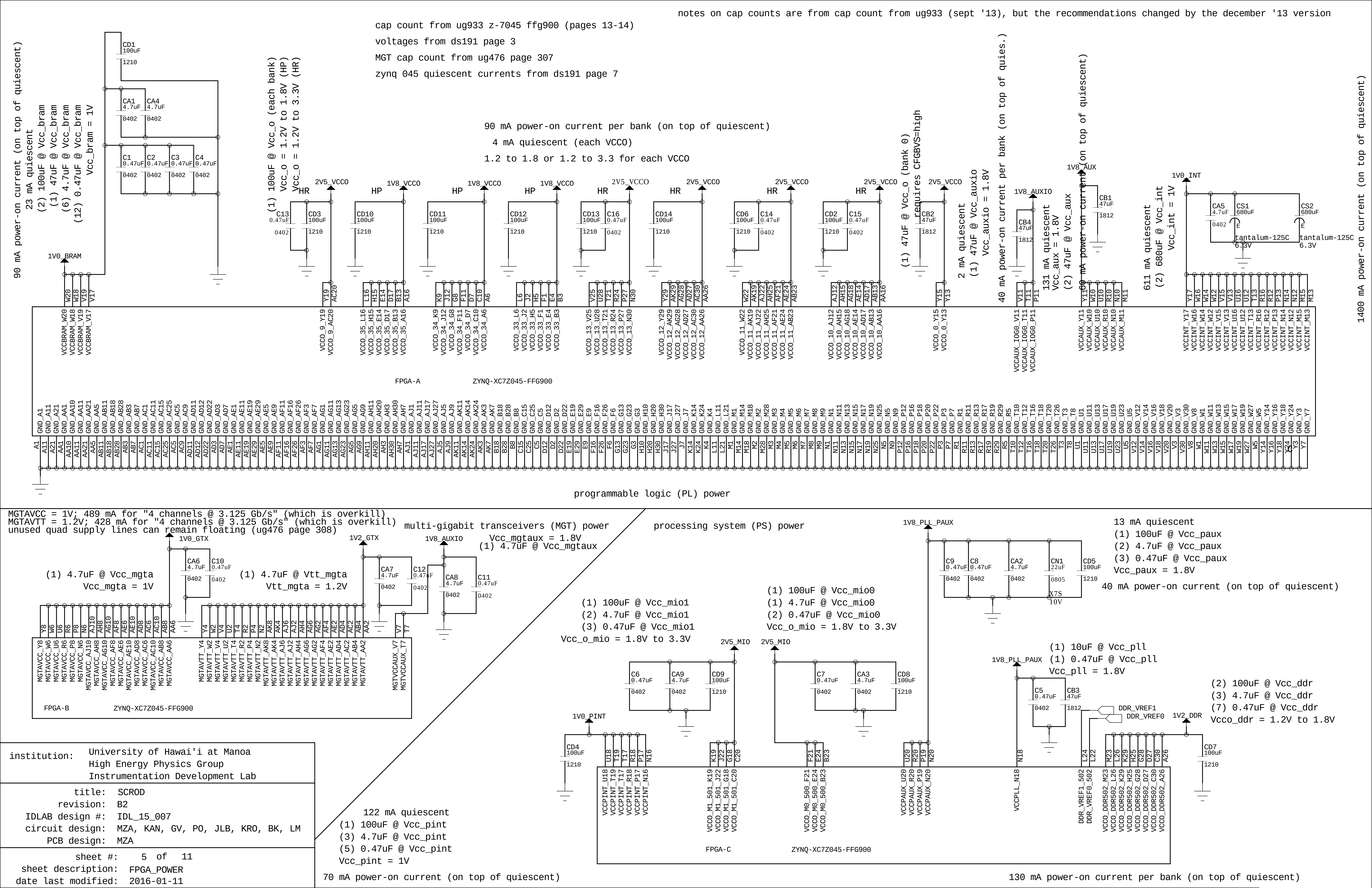
PCB design:	MZA
sheet #:	4 of 11
sheet description:	PL_VOLTAGE_REGULATORS
date last modified:	2016-01-11



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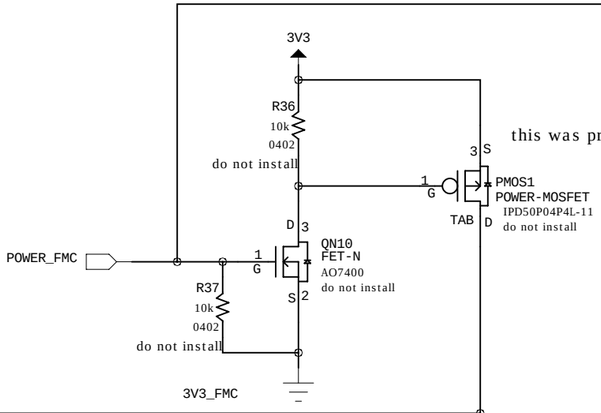
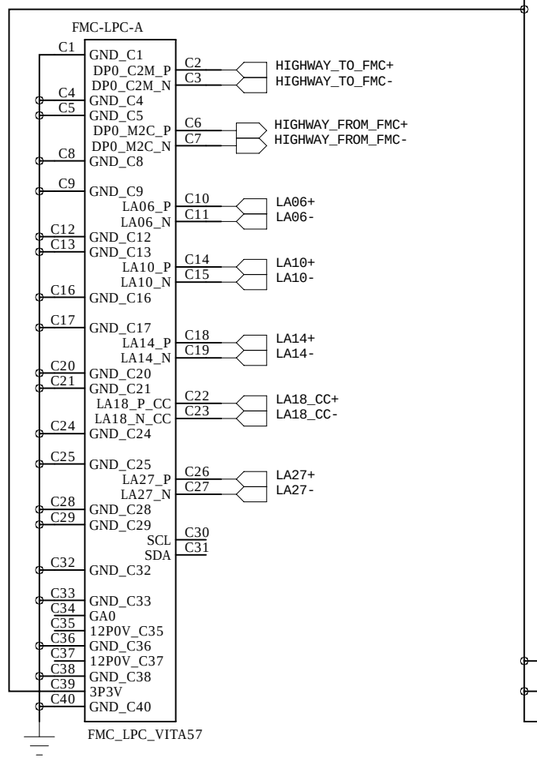
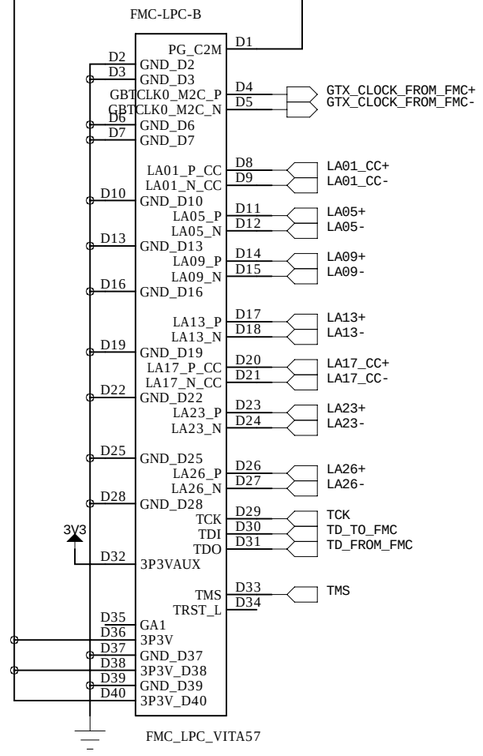
IDLAB design #:	IDL_15_007
circuit design:	MZA, KAN, GV, PO, JLB, KRO, BK, LM
PCB design:	MZA
sheet #:	5 of 11
sheet description:	FPGA_POWER
date last modified:	2016-01-11

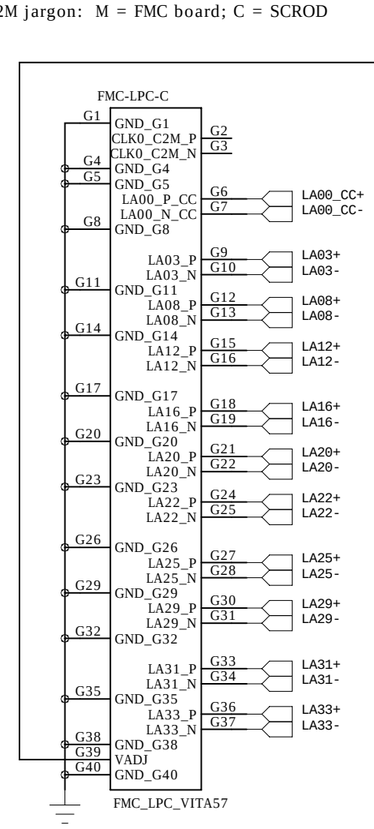


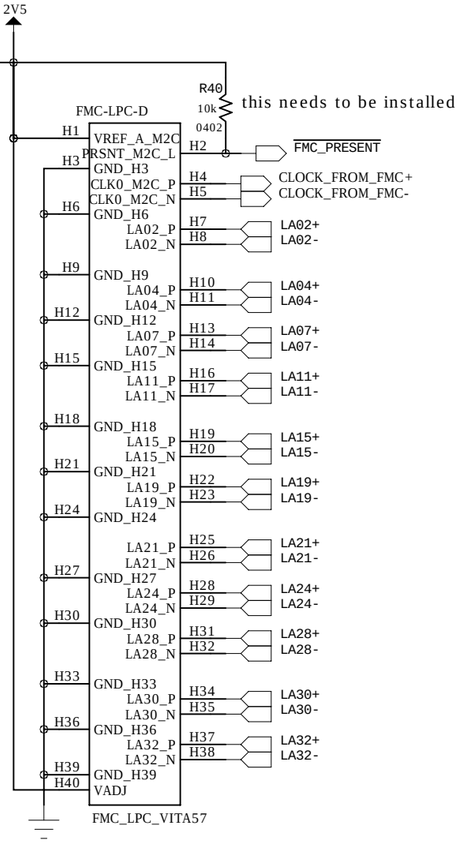
this was previously called out as an n-channel part number

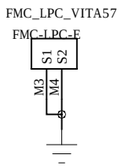
for M2C/C2M jargon: M = FMC board; C = SCROD

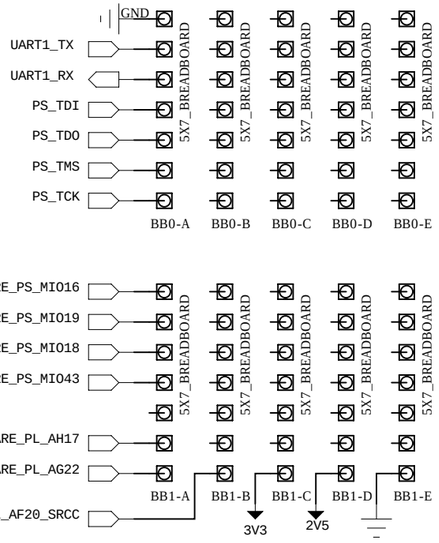












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IDLAB design #:	IDL_15_007
circuit design:	MZA, KAN, GV, PO, JLB, KRO, BK, LM
PCB design:	MZA
sheet #:	6 of 11
sheet description:	FMC_LPC_CONNECTOR_BREADBOARD
date last modified:	2016-01-11

X6
MOUNTING-HOLE-6-32-SKINNY
X7
MOUNTING-HOLE-6-32-SKINNY
X1
MOUNTING-HOLE
MOUNTING-HOLE-M2.5-MODIFIED
X8
MOUNTING-HOLE-6-32-SKINNY
GND

FX8C-100S-SV5

key=gnd for vertical position detection by carrier

2V5_VCCO
0402 R4 10k
0402 R12 10k
0402 R13 10k
0402 R14 10k

carrier presence detect for SCROD

CARRIER0_PRESENT
CARRIER1_PRESENT
CARRIER2_PRESENT
CARRIER3_PRESENT

could throw some resistors here so there's little chance of future power-to-ground shortnanigans next time...

X3
MOUNTING-HOLE-6-32-SKINNY
X4
MOUNTING-HOLE-6-32-SKINNY
X2
MOUNTING-HOLE
MOUNTING-HOLE-M2.5-MO
X5
MOUNTING-HOLE-6-32-SKINNY
GND

RAW3
CQ3 100uF D
CQ6 100uF D
CR3 100uF EBIG
niobium-oxide-105C 10V
niobium-oxide-105C 10V
tantalum-125C 20V

4V0
3V3
2V5

CAL3
CAL2
CAL1
CAL0

CAL signals to individual carrier boards

GTX-CLOCK-FROM-CARRIER+
GTX-CLOCK-FROM-CARRIER-

(comes from thermal_alarm)
RESET_CARRIERS
RESET_CLOCK_DIVIDER

(pulled up to 2V5_PSPL on carrier board)
THERMAL_ALARM
(open drain; pulled to RAW2)
NOT_ALL_RAW_VOLTAGES_PRESENT
BOARD_HAS_BEEN_POWERED
(open drain; pulled to 2.5V)

TCK
TD_TO_CARRIER
TD_FROM_CARRIER
TMS

T3

for power supply sequencing the other boards

T1

FX8C-100S-SV5

CLOCK_TO_ASICS_ON_CARRIER0+
CLOCK_TO_ASICS_ON_CARRIER0-
TRIG_TO_GDL_FROM_CARRIER0+
TRIG_TO_GDL_FROM_CARRIER0-
CLOCK_TO_ASICS_ON_CARRIER1+
CLOCK_TO_ASICS_ON_CARRIER1-
TRIG_TO_GDL_FROM_CARRIER1+
TRIG_TO_GDL_FROM_CARRIER1-
CLOCK_TO_ASICS_ON_CARRIER2+
CLOCK_TO_ASICS_ON_CARRIER2-
TRIG_TO_GDL_FROM_CARRIER2+
TRIG_TO_GDL_FROM_CARRIER2-
CLOCK_TO_ASICS_ON_CARRIER3+
CLOCK_TO_ASICS_ON_CARRIER3-
TRIG_TO_GDL_FROM_CARRIER3+
TRIG_TO_GDL_FROM_CARRIER3-

SCROD_TO_CARRIER0+
SCROD_TO_CARRIER0-
CARRIER0_TO_SCROD+
CARRIER0_TO_SCROD-
SCROD_TO_CARRIER1+
SCROD_TO_CARRIER1-
CARRIER1_TO_SCROD+
CARRIER1_TO_SCROD-
SCROD_TO_CARRIER2+
SCROD_TO_CARRIER2-
CARRIER2_TO_SCROD+
CARRIER2_TO_SCROD-
SCROD_TO_CARRIER3+
SCROD_TO_CARRIER3-
CARRIER3_TO_SCROD+
CARRIER3_TO_SCROD-

RAW1
CR1 100uF EBIG
CQ1 100uF D
CQ4 100uF D
tantalum-125C 20V
niobium-oxide-105C 10V
niobium-oxide-105C 10V

T2

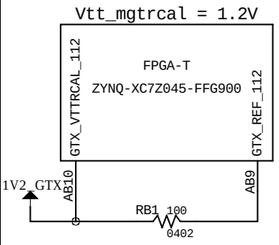
FX8C-100S-SV5

HIGHWAY_TO_CARRIER3+
HIGHWAY_TO_CARRIER3-
HIGHWAY_FROM_CARRIER3+
HIGHWAY_FROM_CARRIER3-
HIGHWAY_TO_CARRIER2+
HIGHWAY_TO_CARRIER2-
HIGHWAY_FROM_CARRIER2+
HIGHWAY_FROM_CARRIER2-
HIGHWAY_TO_CARRIER1+
HIGHWAY_TO_CARRIER1-
HIGHWAY_FROM_CARRIER1+
HIGHWAY_FROM_CARRIER1-
HIGHWAY_TO_CARRIER0+
HIGHWAY_TO_CARRIER0-
HIGHWAY_FROM_CARRIER0+
HIGHWAY_FROM_CARRIER0-

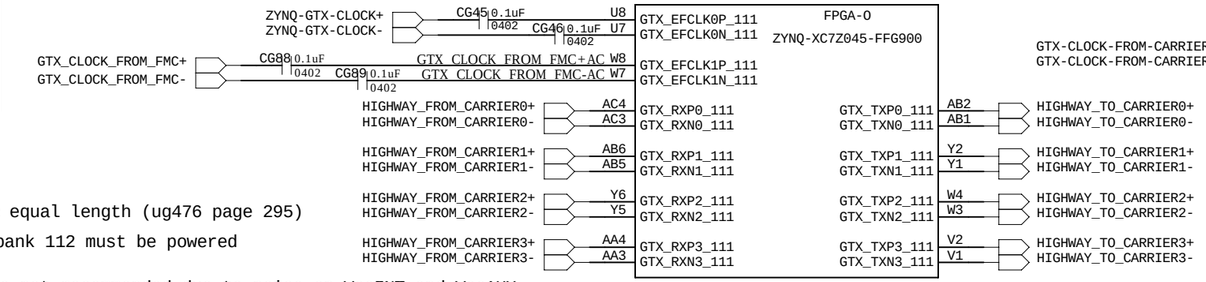
HIGHWAY_TO_CARRIER_SPARE0+
HIGHWAY_TO_CARRIER_SPARE0-
CLOCK_FROM_FTSW_FOR_CARRIER3+
CLOCK_FROM_FTSW_FOR_CARRIER3-
HIGHWAY_FROM_CARRIER_SPARE0+
HIGHWAY_FROM_CARRIER_SPARE0-
CLOCK_FROM_FTSW_FOR_CARRIER2+
CLOCK_FROM_FTSW_FOR_CARRIER2-
CLOCK_FROM_FTSW_FOR_CARRIER1+
CLOCK_FROM_FTSW_FOR_CARRIER1-
CLOCK_FROM_FTSW_FOR_CARRIER0+
CLOCK_FROM_FTSW_FOR_CARRIER0-

RAW2
CQ5 100uF D
CQ2 100uF D
CR2 100uF EBIG
niobium-oxide-105C 10V
niobium-oxide-105C 10V
tantalum-125C 20V

institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	SCROD
revision:	B2
IDLAB design #:	IDL_15_007
circuit design:	MZA, KAN, GV, PO, JLB, KRO, BK, LM
PCB design:	MZA
sheet #:	7 of 11
sheet description:	BOARD_TO_BOARD_CONNECTORS
date last modified:	2016-01-11

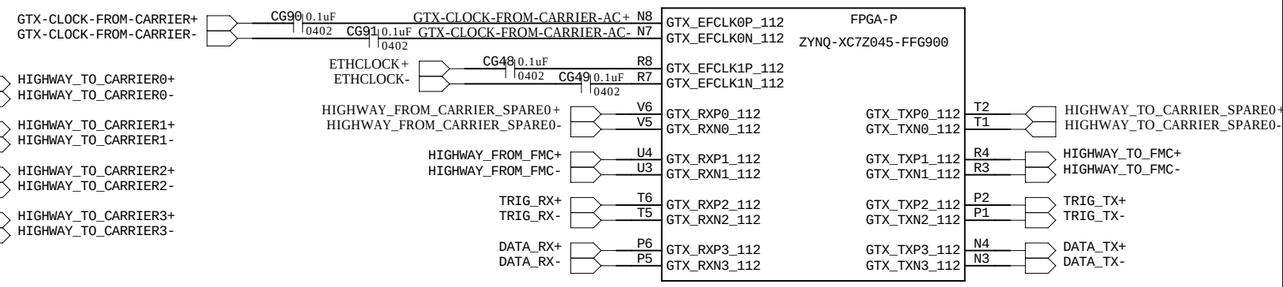


gigabit connections between SCROD and each carrier board



gigabit connections to backend HSLB and FMC daughtercard, and a spare channel to a carrier

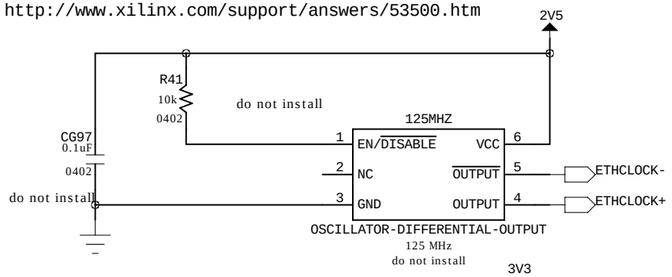
GTX clock must be AC coupled through 100nF caps (ug476 page 307)



these two traces must be equal length (ug476 page 295)

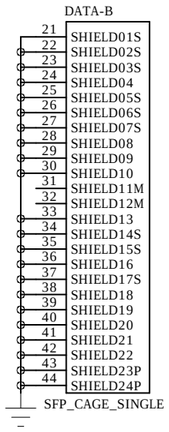
ug476 page 294 says quad/bank 112 must be powered

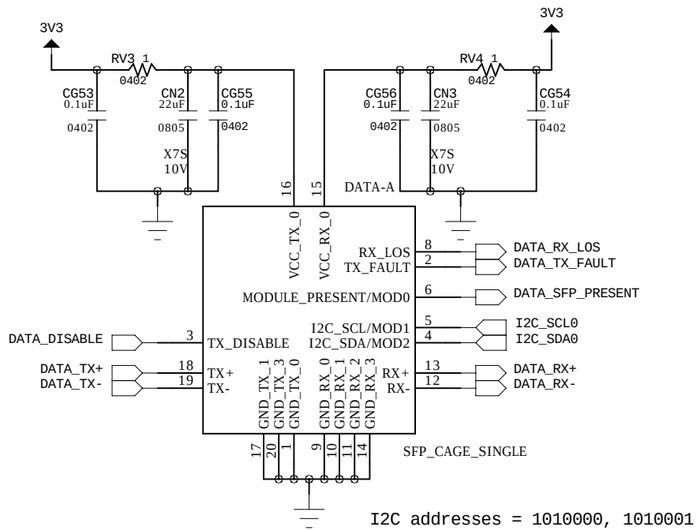
GTX clocks via fabric are not recommended due to noise on VccINT and VccAUX
http://www.xilinx.com/support/answers/53500.htm



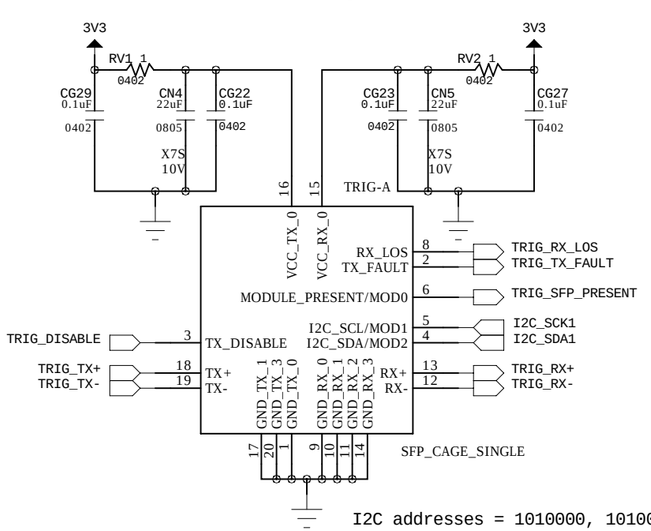
note: GTX clocks from 110 can be used on the 111; clocks from 112 can be used on the 111; but 110 clocks can't be used on the 112 and vice versa

each AFBR-57D7APZ uses 235mA (measured value is 120mA, but without FPGA connection)
trig_present and data_present need PULLUP enabled in FPGA
data_tx_fault and trig_tx_fault need PULLUP enabled in FPGA
ramp time of 3.3V seems to be ~3ms, so these 1 Ohm resistors see 150mV or 23mW peak

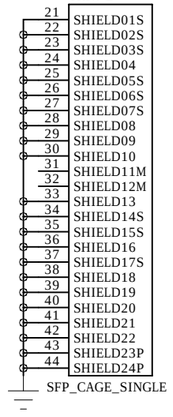




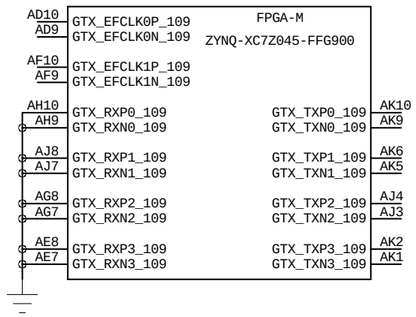
I2C addresses = 1010000, 1010001

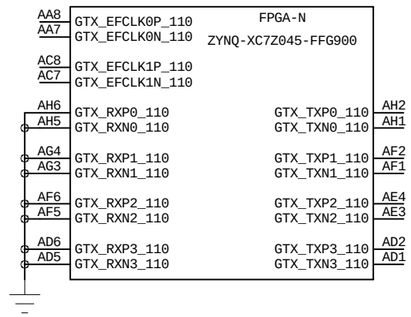


I2C addresses = 1010000, 1010001



ug476 page 304 says we should leave unused gtx clock inputs floating





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circuit design:	MZA, KAN, GV, PO, JLB, KRO, BK, LM
PCB design:	MZA
sheet #:	8 of 11
sheet description:	FIBER_OPTIC_TRANSCEIVERS
date last modified:	2016-01-11

CFGBVS determines JTAG voltage (ug470 page 22)
configuration (bank 0) voltage is 2.5V

all CGnn are 0.1uF 0402

M80-51220

clock in corner, then ground/shield, NC pins next, then timing stuff, then jtag

L=LVDS

H=Header

M=Multiplexer

F=FPGA

JTAG_SEL must be LVDS when 14 pin header not connected
ds593 page 16 suggests this hookup

sneaky place for the 17th analog input...

Xilinx now recommends 300 Ohms here

Vcc_adc = 1.8V @ 25 mA

ug480 page 13; short vrefp to gnd to use internal reference

2V terminated into 50 Ohms = 80 mW

5V terminated into two 10k = 5 mW each

5 V terminated into 50 Ohms = 500 mW

2G34 introduces 1.5 to 4.4 ns delay

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PCB design:	MZA
sheet #:	9 of 11
sheet description:	JTAG_MISCELLANEOUS
date last modified:	2016-01-11

VIO and VCC must come up at the same time for these parts
ug585 page 342 says only up to 128Mbit devices are supported, although a 256Mbit part would fit on the board...

data fiber transceiver also on this i2c chain

I2C address = 1001010

I2C address = 1010100

I2C address = 1000000

trig fiber transceiver also on this i2c chain

"multiple assert inhibit / thermal_alarm inhibit"

thermal_alarm	mai_tai	reset_carriers	result
1	1	1	normal operation
1	0	Z	normal operation
0	1	0	carriers held in reset
0	0	Z	normal operation (ignore thermal alarm)

ug933 page 62 says LPDDR2 does not require termination

ug585 page 256/257 : bank, ras, cas, we, reset signals not used in LPDDR2?

http://www.phys.hawaii.edu/~mza/PCB/SCROD/LPDDR2-propagation-delays.xls

10uF on VBUS is the limit of the USB spec

ug585 page 647 says pulsing SRST will clear the PL configuration

12mA@3.3V, 30mA@1.8V, 6mA@IOV

VDD1 = 1.8V; all else are 1.2V
VDD1 needs 20 mA
VDD2 needs 210 mA peak
VDDCA + VDDQ need 28 mA combined

ug585 page 273 and ug933 page 53 both say that the zynq can generate the vrefs for the LPDDR2 RAM resistive dividers are for when that doesn't work
ug585 pages 271 and 614 say LPDDR2 ram does not need a termination resistor

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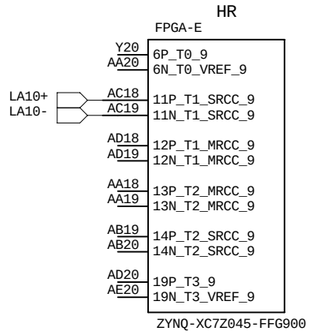
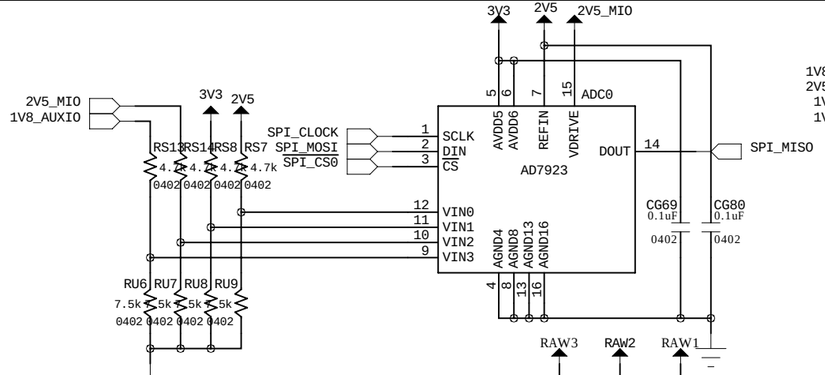
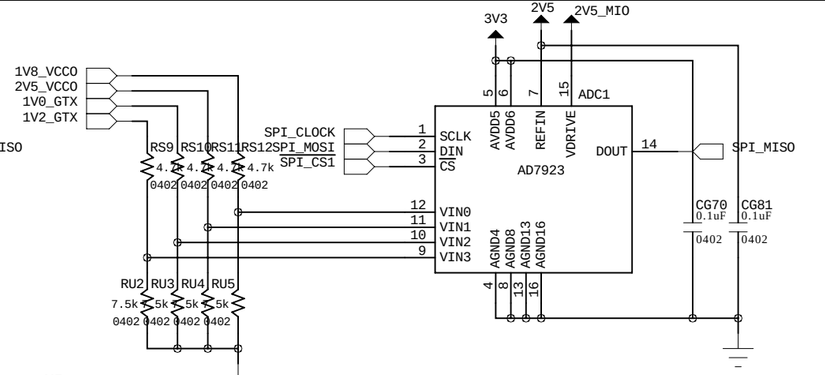
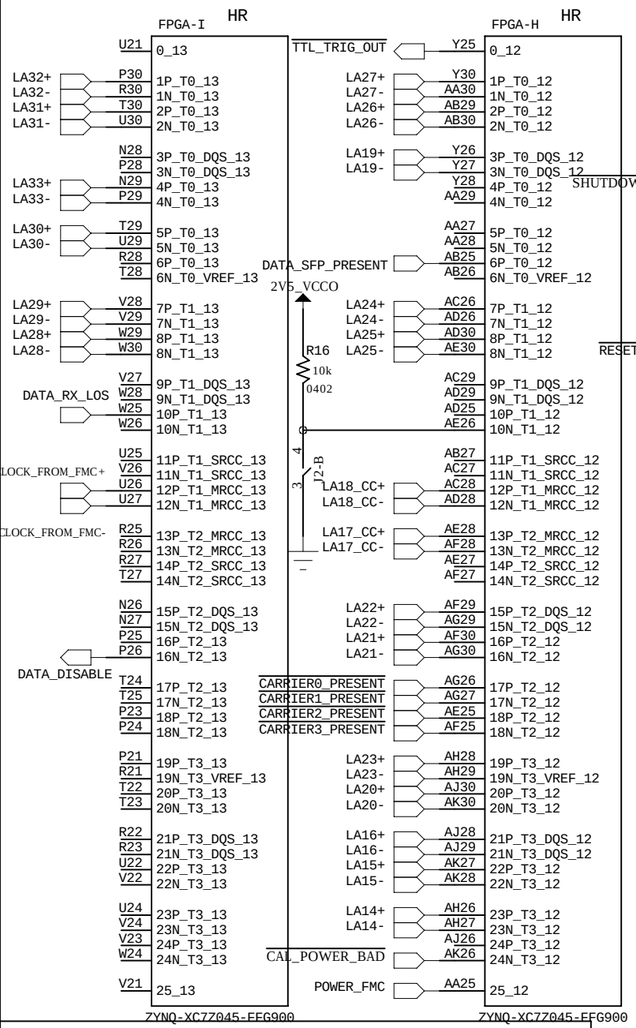
PCB design:	MZA
sheet #:	10 of 11
sheet description:	PS_CONNECTIONS_ARM_IIC_RAM_FLASH
date last modified:	2016-01-11

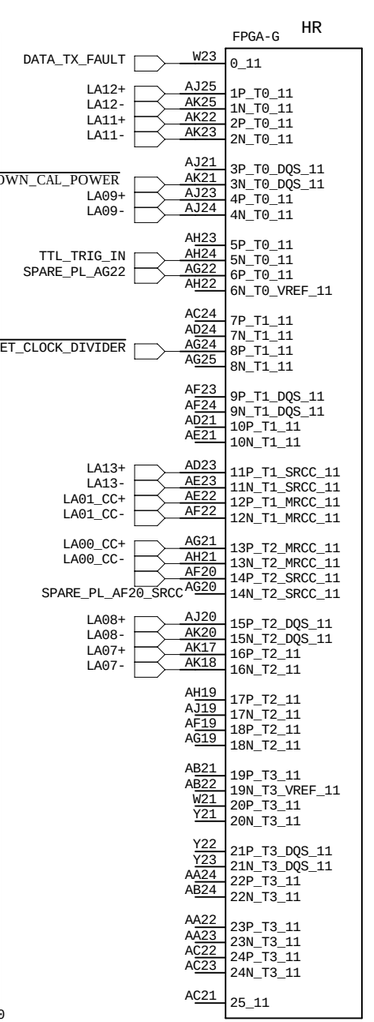
banks 33,34,35 are 1.8V; the rest are 2.5V

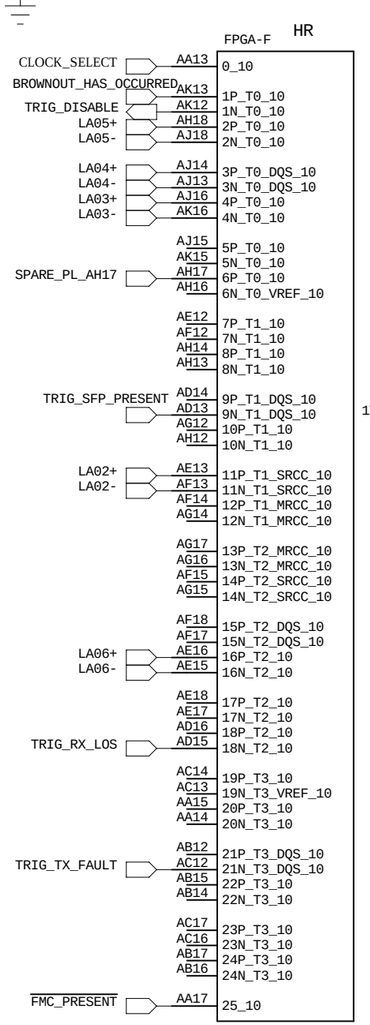


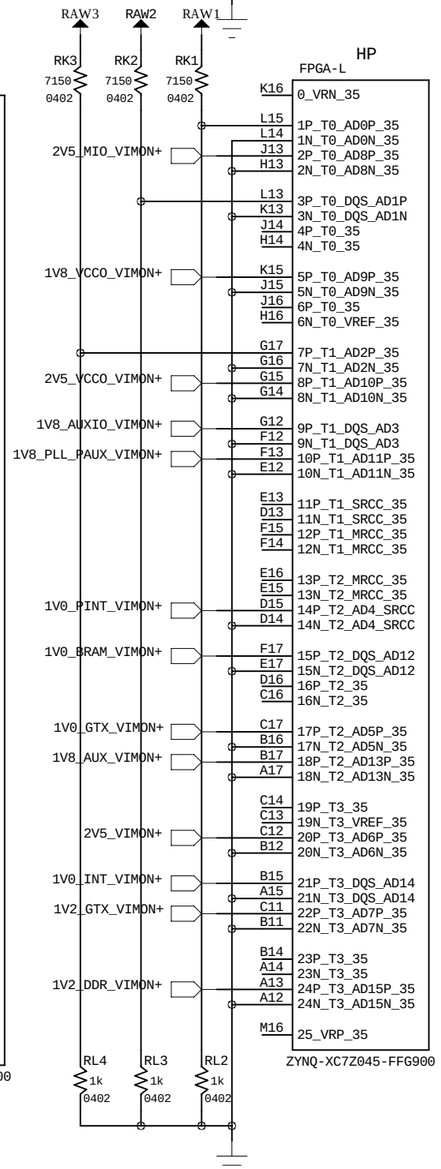


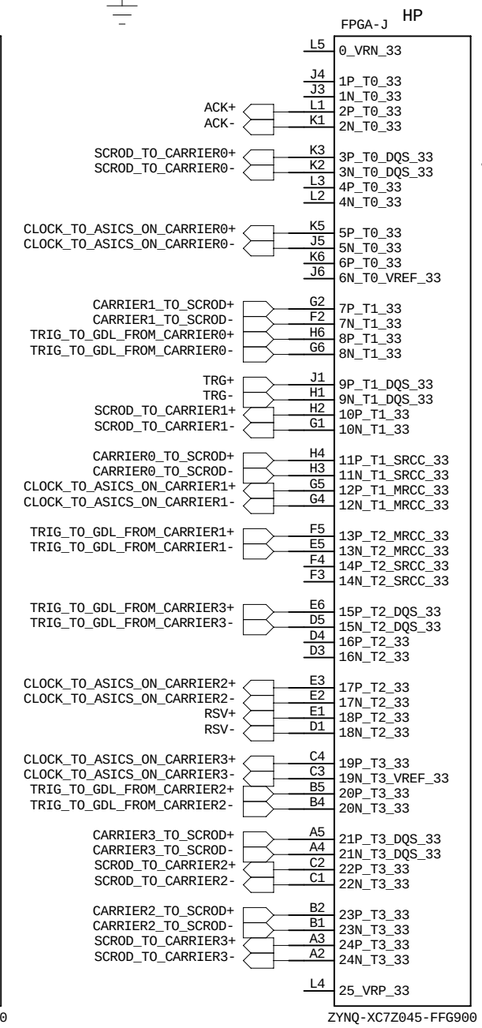


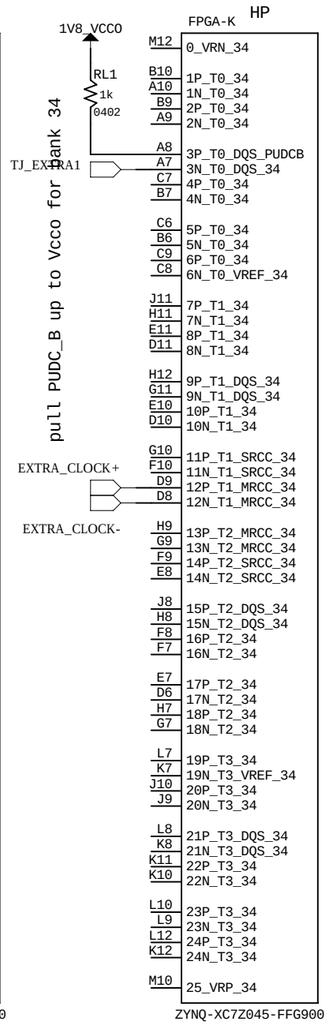












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PCB design:	MZA
sheet #:	11 of 11
sheet description:	PL_CONNECTIONS_FPGA_ANALOG_INPUT
date last modified:	2016-01-11

ug480 page 21 says Vccint, Vccaux, Vccbram, Vccpint, Vccpaux, Vccddr are monitored internally

analog inputs for current monitors:
LT3055s drive 1/500th of the current through 121 Ohm resistors
LT3086s drive 1/1000th of the current through 240 Ohm resistors
both of these go into 12 bit ADCs with a 1V full-range input
so both give approximately 1mA/ADC count

analog inputs for raw voltage monitors:
the three RAW inputs are divided with a 7.15k/1k voltage divider into a 1V / 12 bit A
so this gives approximately 2mV/ADC count

analog inputs for other voltage monitors:
the other voltage inputs go through 4.7k/7.5k voltage dividers
into 2.5V 12 bit ADCs
so this gives approximately 1mV/ADC count