things done for SCROD revB2:

- We will take the (wire-ORed) thermal_alarm signal and drive the reset_carriers signal from it, so if the boardstack goes overtemperature, all 4 carriers will get reset (which will immediately drive the ASIC and AMP regulators into shutdown)

- Add dual 100 Ohm resistors (one to power, other to gnd) near LPDDR2 memory for address lines? (and maybe control lines too?)

- Need to look into termination for the JTAG signals (ug470 page 60 says TCK must be terminated, but we have a distribution amplifier driving a copy of the raw signal)

- On second batch of assembled SCROD revB2's, RV5 is marked as "do not install"

- Changed R40 to install (or JTAG chain is not reliable)

- Changed protection diode to shunt to 4V0 instead of 3V3

- Connected the last TJ pin to a test point (TJ_EXTRA2)

- Connected another TJ pin to an FPGA pin (TJ_EXTRA1; on a HP bank)

- Added surface-mount test points for RAW1+,2+,3+ and two power-supply sequencing signals

- Exchanged 18 pin nicomatic/harwin part for the 20 pin

- Removed FET driving init after power-up, as PS_POR is doing what we want anyway

- Brought North end of board in by 1mm

- Added R39 pullup, marked as "do not install" for cases where there is a local oscillator present

- Removed cap from CLOCK_SELECT line; replaced 50 Ohm terminators with a 100 Ohm terminator for the DC-coupled oscillator

- Move DATA_DISABLE and DATA_RX_LOS to a HR bank (the bank they were on is now a 2.5V bank)

- Change reference designators on R, C so we have contiguous lists (RC1-12, etc); consolidate letters for parts with few instances

- Double-check pins on SFP connectors against the standard (matches list on wikipedia 2015-03-13, except for RateSelect pin which is NC in our decal)

- JTAG connector holes can be smaller

- Notes for end-user:
  - SCROD revB3:
    - not doing this:
      - change CAL fanout to use single mini-circuits ERA-2+ amplifier? (maybe?)

- Capacitors:
  - CS = 680 uF E tantalum 125C
  - CQ = 100 uF E niobium oxide 105C
  - CP = 22 uF 1210 16V X7R 10%
  - CN = 22 uF 0805 10V X7S 20%
  - CM = 100 pF 0402 50V NP0 5%
  - CJ = 270 pF 0402 50V NPO 0.1%
  - CD = 100 uF 1210 6.3V X5R 20%
  - CC = 10 nF 0402 16V X7R 10%
  - CA = 4.7 uF 0402 6.3V X5R 20%

- Resistors:
  - JA = 40 Ohm (1/4W)
  - JB = 40 Ohm (1/4W)
  - JC = 40 Ohm (1/4W)
  - JD = 40 Ohm (1/4W)

- LEDs enabled

- Jumper settings:
  - 12 (when jumper present)
  - 11 (when jumper present)

- 12A PS MOND7 = 0
- 12B PL AE26 = 0
- 12C PSBI mode
- 12D LDOs enabled
this 2.5V regulator supplies:
oscillator (70 mA)
various pull-ups (1 mA)
humidity sensor (1 mA)
SPI flash (100 mA)
supply sequencing logic
FADC0T power

this 3.3V regulator supplies:
USB (12 mA)
SPI flash (100 mA)
both fiber transceivers (470 mA)
JTAG LVDS receiver (20 mA)
protection diodes shunt here

FMC board 3.3V (AUX3.3V always and FMC3.3V via mosfet)

various pull-ups (1 mA)
JTAG LVDS receiver (20 mA)

this one must stay as discrete transistors due to the rail

- BROWNOUT HAS_OCCURRED
- BOARD_HAS_BEEN_POWERED
- BOARD_HAS_BEEN_POWERED
- DISABLE_PL
- DISABLE_PS
- PL_SHOULD_POWER_UP
- PS_SHOULD_POWER_UP
- PS_AND_PL_SHOULD_POWER_UP
- WAIT_FOR_PL
- WAIT_FOR_PS
- PS_AND_PL_ARE_POWERED
- PL_IS_POWERED
- PS_IS_POWERED
- DISABLE_PS_WAIT_FOR_PL_PS_SHOULD_POWER_UP
- DISABLE_PL_WAIT_FOR_PS_PS_SHOULD_POWER_UP
- PL_IS_POWERED_PS_SHOULD_POWER_UP
- PS_AND_PL_SHOULD_POWER_UP

- PS_NOT_DISABLED
- PL_NOT_DISABLED

200 closed to enable LEDs
10k pull-downs

- ps_and_pl_are_powered
- power_entry_and_sequencing
- testing_point_through_hole_score
- testing_point_s_c_c_surf
- testing_point_s_c_c_surf
- testing_point_s_c_c_surf
- testing_point_s_c_c_surf
- testing_point_s_c_c_surf
- testing_point_s_c_c_surf
- testing_point_s_c_c_surf
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- testing_point_s_c_c_surf
- testing_point_s_c_c_surf
- testing_point_s_c_c_surf
- testing_point_s_c_c_surface
PS_SHOULD_POWER_UP
MZA, KAN, GV, PO, JLB, KRO, BK, LM

IDL_15_007
SCROD

DBUF2-B
0603
0603
CH1
BUFFER-OPEN-DRAIN-SN74LVC2G07

RAW2
0.1uF
CG7
0402
0402
10nF
CC1
10
3
2
1

IMAX
REF/BYP
IN2
IN1

LT3055
12
GND13
PWRBAD
PWRBAD
FAULT2
OUT16
OUT15
TEMP
IMON
16
8
15
4

RD4
RD2
0402
0402
RF1
121k
40.2k
0402
CC4
10nF
0402
0603
0603
10uF
CH2

TEST-POINT-SURFACE-MOUNT-OCTAGONAL
1V8_PLL_PAUX
1I8_PLL_PAUX
1I0_PINT
1V0_PINT_VIMON+

DBUF2-A
BUFFER-OPEN-DRAIN-SN74LVC2G07
0402
0402
0.1uF
CG3

DBUF2-C
BUFFER-OPEN-DRAIN-SN74LVC2G07
1210
4

DDR2=1.8V; DDR3=1.5V; LPDDR2=1.2V; 4 mA quiescent + 520 mA @ power-on (130 mA/bank) = 524 mA peak

using LT3055

MIO = 1.8V to 3.3V; 2.5V for now

REF/BYP
SHDN
ILIM
SHDN
TRACK
NC
GND1
GND13
GND17
GND17

DDR2=1.8V; DDR3=1.5V; LPDDR2=1.2V; 4 mA quiescent + 520 mA @ power-on (130 mA/bank) = 524 mA peak

Ps = 1V; 122 mA quiescent + 70 mA peak = 192 mA peak

PsAux = 1.8V; 13 mA quiescent + 40 mA peak = 53 mA peak

Ps_PIN1
Ps_PIN2
Ps_PIN3
Ps_PIN4
Ps_PIN5
Ps_PIN6
Ps_PIN7
Ps_PIN8
Ps_PIN9
Ps_PIN10
Ps_PIN11
Ps_PIN12
Ps_PIN13
Ps_PIN14
Ps_PIN15
Ps_PIN16
Ps_PIN17
Ps_PIN18
Ps_PIN19
Ps_PIN20

Ps_AND_Pl_ARE_POWERED

total 8 stages of 20 ms RC filter for both Ps and Pl sequencing; LTspice simulation shows about 200 ms between power being applied and the Ps_AND_Pl_ARE_POWERED signal going high

institution: University of Hawai'i at Manoa
High Energy Physics Group
Instrumentation Development Lab

title: SCROD
revision: B2
IDLAB design #: IDL_15_007
circuit design: MZA, KAN, GV, PO, JLB, KRO, BK, LM
PCB design: MZA

sheet #: 3 of 11
sheet description: PS_VOLTAGE_REGULATORS
date last modified: 2016-01-11
100uF
10V
niobium-oxide-105C
10V
100uF
D
EBIG
CR1
CARRIER1_PRESENT
TRIG_TO_GDL_FROM_CARRIER1+
TRIG_TO_GDL_FROM_CARRIER1-
CARRIER1_TO_SCROD-
CARRIER1_TO_SCROD+
SCROD_TO_CARRIER1+
SCROD_TO_CARRIER1-
CLOCK_TO_ASICS_ON_CARRIER1+
CLOCK_TO_ASICS_ON_CARRIER1-
CAL signals to individual carrier boards

key=gnd for vertical position detection by carrier
could throw some resistors here so there's little chance of future power-to-ground shorntangas next time...

for power supply sequencing the other boards

MOUNTING-HOLE-6-32-SKINNY
MOUNTING-HOLE-6-32-SKINNY
MOUNTING-HOLE-M2.5-MODIFIED
MOUNTING-HOLE-6-32-SKINNY
MOUNTING-HOLE-M2.5-MODIFIED
MOUNTING-HOLE-6-32-SKINNY
MOUNTING-HOLE-6-32-SKINNY
MOUNTING-HOLE-M2.5-MODIFIED
MOUNTING-HOLE-6-32-SKINNY

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Instrumentation Development Lab

title: SCROD
revision: B2
IDLAB design #: IDL_15_007
Circuit design: MGA
PCB design: MGA

sheet #: 7 of 11
sheet description: BOARD TO BOARD CONNECTORS
date last modified: 2016-01-11
gigabit connections between SCROD and each carrier board

GTX clocks via fabric are not recommended due to noise on VccINT and VccAUX
http://www.xilinx.com/support/answers/53500.htm

note: GTX clocks from 110 can be used on the 111; clocks from 112 can be used on the 111; but 110 clocks can't be used on the 112 and vice versa
banks 33,34,35 are 1.8V; the rest are 2.5V