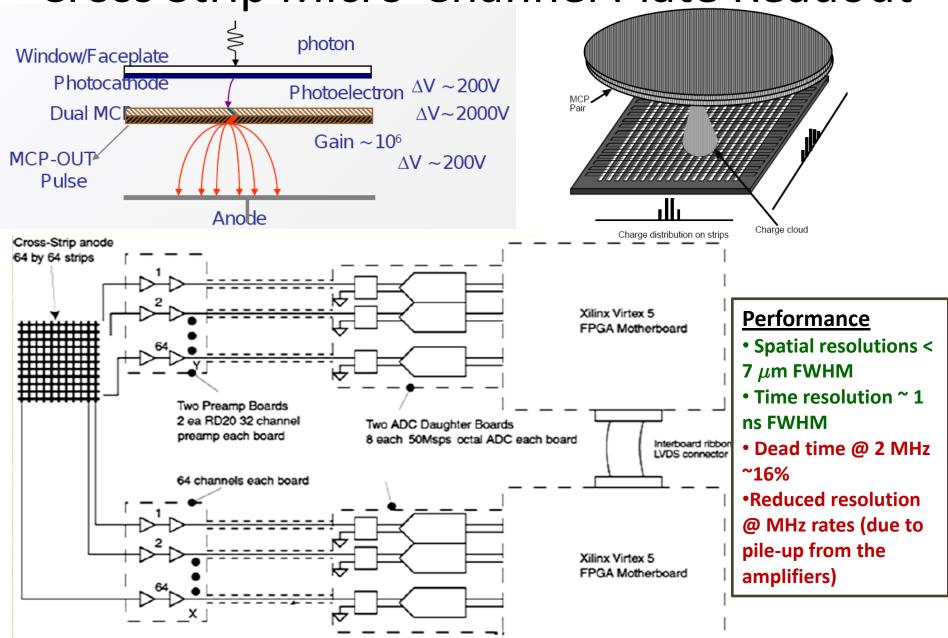
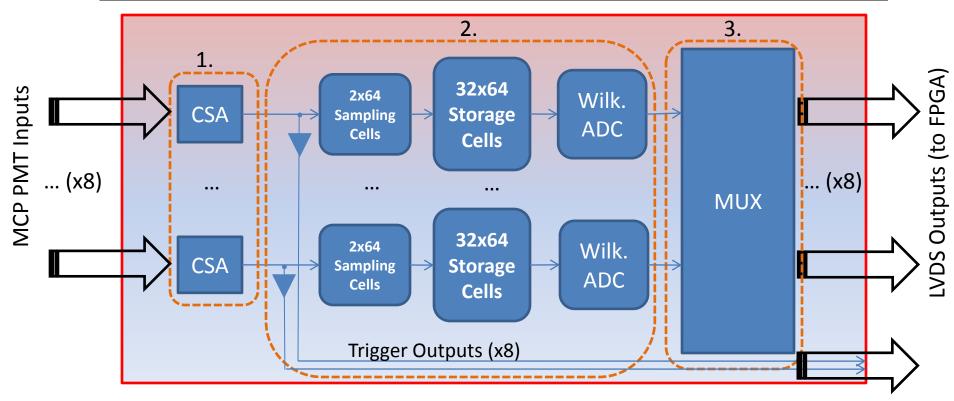
Cross Strip Micro-Channel Plate Readout



Gigasample Recorder of Analog waveforms from a Photodetector (GRAPH) ASIC



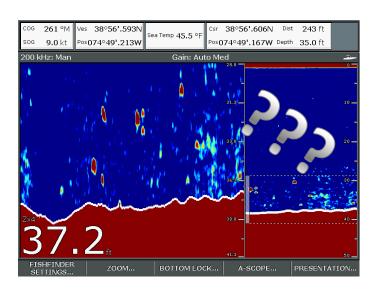
The full GRAPH block diagram is represented above, and has 3 primary challenges:

- 1. Charge sensitive amplifier (CSA) performance
 - Reduce pile-up with a faster amplifier.
 - Maintain low noise.
- 2. Noise and dynamic range of the sampling/digitization
 - Increase sampling rate from 50 MHz to ~GHz.
 - Large dynamic range to allow detection of signal on many strips.
- 3. Fast throughput to the FPGA
 - Onboard triggering & MUX for data reduction during transfer/readout

An aside on naming...

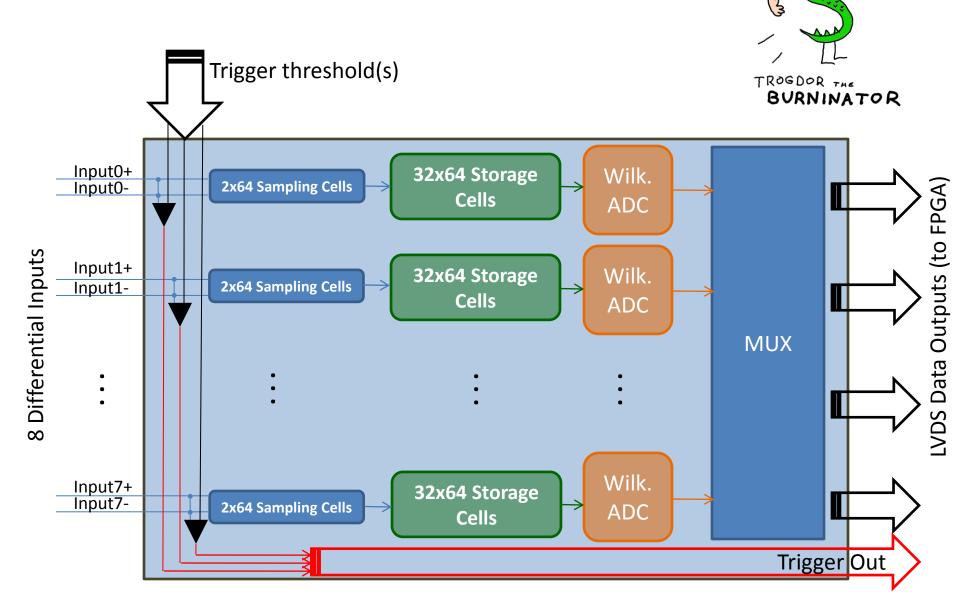
- Original name: Sampler Optimized for Noise and Range (SONAR)
 - I guess this is okay... but the ASIC really has nothing to do with sonar, which could be confusing.





- New acronym that doesn't mislead.
 - (Though it does betray that I'm a nerd.)

TRigger-Onboard Gigahertz Digitizer Optimized for Range (TROGDOR)



TROGDOR Specifications

Parameter	Value	Comments
Input channels	8	Differential
Sampling cells per channel	128	2 rows of 64 cells
Storage cells per channel	2048	32 rows of 64 cells
Sampling rate	~1 Gsa/s	
Dynamic range	~10 bits	Effective(?)
Buffer depth	~2 μs	@ 1 GSa/s
Throughput	~4 MHz	w/~0 dead time
Trigger outputs to FPGA	8(?)	LVDS? Individual trigger thresholds? Prototype 1 or 2 channels only?
Data outputs to FPGA	4(?)	LVDS

Important questions...

- Independent Wilkinson ADCs for each channel?
- Triggering
 - How many trigger lines? One to prototype, or all channels?
 - Thresholds set externally or onboard?
- Output multiplexing 4 channels out?

Simulations Needed

- Input coupling & analog bandwidth
 - Input expected from CSAs?
- Triggering
- Sampling speed
- Sampling transfer to storage array
- Wilkinson performance
 - Linearity
 - Digitization time
- Output multiplexing