Electronic Readout System for Belle II Imaging Time of Propagation Detector

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Belle II experiment at SuperKEKB electron-positron collider (KEK, Tsukuba, Japan):

- asymmetric collisions of 7 GeV electron beam with 4 GeV positron beam (program’s total integrated luminosity = 50 ab⁻¹)

- studies of CP-violating physics processes from decays of Υ(4S) resonances

- need for improved barrel particle identification to detect rare and previously unobserved phenomena and to mitigate beam backgrounds

- in the p_T range from 1 GeV/c to 4 GeV/c pions have to be separated from kaons with the efficiency of 85-90%, while the misidentification efficiency has to be less than 5%

- new 8192-channel Cherenkov radiation imaging Time of Propagation Detector (iTOP)
Imaging Time of Propagation Detector

16 modules placed between Central Drift Chamber and Electromagnetic Calorimeter

in each module:

- 2.5 m long quartz bar glued from two 125 x 44 x 2 cm² pieces
- a spherical mirror is glued to one end and a prism is glued to another end of the bar
Cherenkov Radiation in Quartz

Cherenkov photon from kaon

Cherenkov photon from pion

measurement of Cherenkov photon x-y position at the prism surface (MCP-PMT pixel coordinate) and in-quartz propagation time

Hamamatsu microchannel plate photomultiplier tube (MCP-PMT) R10754-07-M16(N)

16-channels (4 x 4 pixel matrix)

32 MCP-PMTs are attached to each prism
Ice Radio Sampler

Ice Radio Sampler version X (IRSX) ASIC
adaptation from designs for neutrino experiments in Antarctica

0.25 µm TMSC CMOS process

8 channels

switched capacitor array with 32,768 storage cells for each channel sampling buffer

operational sampling speed is 2.714 gigasamples per second
Sample and Hold Cell

Write Strobe

Trigger

Vin

T1

T2

Csample

V_{\text{pedestal}}

to ADC

basic unit or Switched Capacitor Array

trigger or write strobe closes an analog switch and an input signal gets stored in 14 fF capacitor

charge remains held in the capacitor until it is overwritten or until discharge occurs through leakage
Wilkinson Analog-to-Digital Conversion

A common voltage ramp connected to a positive input of a comparator

11-bit Gray code counter increments while the ramp voltage increases

When the voltage ramp level exceeds the stored sample voltage, the comparator latches the Gray code value

12th bit is for the phase

Stored voltage → time interval → ADC value
Subdetector Readout Module

128-channel standalone front-end electronic readout unit

assembly of four ASIC carrier Boards and one Standard Control Read-Out Data (SCROD) board

ASIC carrier board:
four 8-channel IRSX ASICs and one Xilinx Zynq Z-7030 System on a Chip

SCROD board:
one Xilinx Zynq Z-7045 System on a Chip
SCROD

data link
programming and clock
trigger link
desktop
RAM
connectors to ASIC carrier
low voltage power
Zynq Z-7045
ASIC Carrier Board

- amplifiers
- pogo pin assemblies
- Zynq Z-7030
- IRSX connectors to ASIC carrier or SCROD
Front Boards

- Sockets for MCP-PMT anode and HV contacts (one board per four MCP-PMTs)
- Contact pads for ASIC carrier pogo pins
- Contact pads for HV divider board
High Voltage Board

8 channels (one channel per one MCP-PMT)

each channel: 400 MOhm resistive divider coupled with high voltage transistors

aluminum enclosure

attached to Subdetector Readout Module and to an aluminum water cooling reservoir

pogo pins are pressed against the HV contact pads on two front boards

MCP-PMTs:

operational voltage: from 2100 V to 3100 V
charge gain: from $2 \times 10^5$ to $3 \times 10^5$
Single-Photon Laser Signal Data Taking

data fiber link

programming and clock

high voltage board

water cooling reservoir

laser fiber

MCP-PMT
iTOP Readout Scheme

one iTOP module:

- 32 MCP-PMTs
- 4 Subdetector Readout Modules (SRMs)
- 16 ASIC carrier boards
- 64 IRSX ASICs
- 512 channels
Device: Xilinx Zynq Z-7045

PL: Programmable Logic
Kintex-7 FPGA
350,000 cells
218,600 Look-Up Tables

PS: Processing System
Dual-core ARM Cortex-9
1 GHz

T/T: Trigger and Timing

GTX: Gigabit Transceiver
Device: Xilinx Zynq Z-7030

PL: Programmable Logic
Kintex-7 FPGA
125,000 cells
78,600 Lookup Tables

PS: Processing System
Dual-core ARM Cortex-9
800 MHz

T/T: Trigger and Timing
GTX: Gigabit Transceiver
ASIC Carrier Timing Performance

Single Channel Timing Performance

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<th>Timing</th>
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<tr>
<td>Entries</td>
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<tr>
<td>Mean</td>
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<tr>
<td>RMS</td>
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<tr>
<td>$\chi^2 / \text{ndf}$</td>
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</tr>
<tr>
<td>Constant</td>
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</tr>
<tr>
<td>Mean</td>
<td>$-0.0001576 ± 0.0007125$</td>
</tr>
<tr>
<td>Sigma</td>
<td>$0.02131 ± 0.00050$</td>
</tr>
</tbody>
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measurement of 20 ns time delay between leading edges of a reconstructed 1.5 V pulse of 7 ns width and its delayed copy

overall time resolution is 20 - 30 ps
Timing Performance with MCP-PMTs

Measurement of a time between leading edges of a reconstructed pulse from MCP-PMT signal and a reconstructed calibration reference pulse

Single photon laser signal

Laser trigger is independent from the calibration pulse

Overall time resolution at the laser test bench is from 60 ps to 80 ps

(MCP-PMT transit time spread = 30 ps; laser bench TDC time resolution = 25 ps)
Back-End DAQ System

Common Pipelined Platform for Electronic Readout (COPPER) version III

9U VME format

one High Speed Link Board collects data from one SRM

one COPPER-III board serves one iTOP module

16 COPPER-III boards serve the iTOP detector
Integration at the iTOP

Assembled Subdetector Readout Modules: 78

Installed at iTOP (8192 channels): 64
Installed at a spare iTOP module: 4
Uninstalled spare SRMs: 10

In-situ data taking from calibration laser and cosmic muon ray events without magnetic field demonstrated performance comparable to or surpassing the in-lab performance.

DAQ tests with 1.5 T magnetic field have started and will be continued through several campaigns.

Calibration software that allows reconstruction of laser, cosmic ray muon, and electron-positron collision data with resolution of less than 50 ps have been developed.