TOF Upgrade??

Gary S. Varner

January 20, 2006
FY2005 Activities

• CAP basic functionality published:

• High-performance (timing, waveform) FINESSE

• SVD Rad FET monitor readout development

• CAP3 “full-sized” detector
  • Fabricated, under detailed characterization
  • Mechanics for developing a full-sized pixel vertex detector based upon these devices
Background for today

• Due to increased hit rates in the TOF counter at higher luminosity (higher background conditions), inefficiency of TOF increasing

• Many sub-detectors are considering upgrades to pipelined readout to combat these effects

• We have been exploring possible upgrades to the readout electronics as part of the PID upgrade for Super-Belle

• Shorter-term upgrade?
High Luminosity

At $L = 10^{35} \text{ cm}^{-2}/\text{s}$:
- Pipelined readout:
  128k channels equiv., 40MHz x 2bytes
  10 Tera-bytes per second! (10,000 CDs per second)

  Global Decision logic trigger: 10kHz
  - FIFO: 128k channels equiv., 16 bytes
    20 Giga-bytes per second! (200 GbE links)

  COPPER, online Farm

  200 Mega-bytes per second! (max. data rate to tape)
Common Electronics

- COPPER (CCommon Pipelined Platform for Electronics Readout)
- Card ~ crate – aid in data reduction
- On board data reduction
FINESSE Developments

- Direct time-walk correction

- Belle TOF Counter
- PMT pulse comparison
- 2GSa/s oscilloscope

- CuEval FINESSE
- LABRADOR FINESSE
- LAB FINESSE
- HPTDC FINESSE

- Full-speed, arbitrary Front-End electronics emulation
Current TOF Readout

Belle Detector

- SC solenoid 1.5T
- CsI(Tl) 16X0
- TOF counter 8GeV e⁻
- Si vtx. det. 3 lyr. DSSD
- μ / K_s detection 14/15 lyr. RPC+Fe
- Aerogel Cherenkov cnt. n=1.015~1.030
- 3.5GeV e⁺

Pre-amp

- TOF 256
- TSC 64

TOFFEE

- Mean Time
- T output
- Q-T

Front-End

- Trigger (x4)

Master

- TOF Trigger

To Global Decision Logic and SVD L0 logic

LRS 1877 Mulit-hit TDCs

FastBus Data Acquisition

PID Upgrade Development Status – Jan ‘06
Proposed Upgraded TOF Readout

PID Upgrade Development Status – Jan ‘06
Proposed Partitioning

Single COPPER Card (8 total needed)

- Precision Timing
  - HPTDC (16 channels)

- PMT copy
  - LABRADOR (16 channels)

- Precision Timing
  - HPTDC (16 channels)

- PMT copy
  - LABRADOR (16 channels)

2x “double wide” TOF_FINESE Per COPPER
32 TOF channels/ COPPER
Double Wide Module (to accommodate input connectors/common signals)

1. Prototype with LAB3 (WFS) this semester
2. Pipeline logic extracts single “Q” value from waveform (next slide)
3. Possibility to improve performance
Precision Time Measurement

- Many ideas: e.g. direct digitization at high speed?
PID Upgrade Development Status – Jan ‘06

PID Upgrade Readout

40-80k Photodetector channels

PROMPT Die floorplan: 4 (H)APD channels in a 2.5mm x 2.5mm die

SPICE Simulation of PROMPT Response

The plot shows a linear relationship between output code and TSA timing with the equation:

\[ y = 2.1926x - 282.16 \]

\[ R^2 = 1 \]
Summary

• **TOF Upgrade?**
  – Plan to develop techniques, only 2x new boards needed
  – One uncertainty is getting more HPTDC chips
  – **Decision based upon prototype performance**

• **Short-term goals**
  – Demonstrate WFS technique (LAB_FINESS) TOF performance without TDC
  – Build TOF_FINESS prototype by summer
  – Discussions with DAQ types at Belle TRG-DAQ ’06 (??)