Belle Pixel Detector Upgrade

Gary S. Varner, for the Belle Pixel Group*
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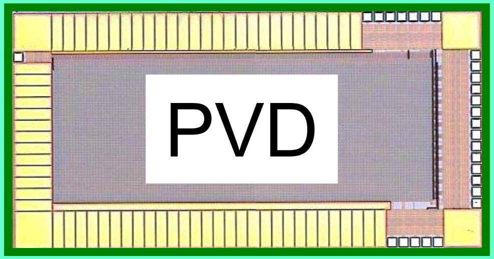
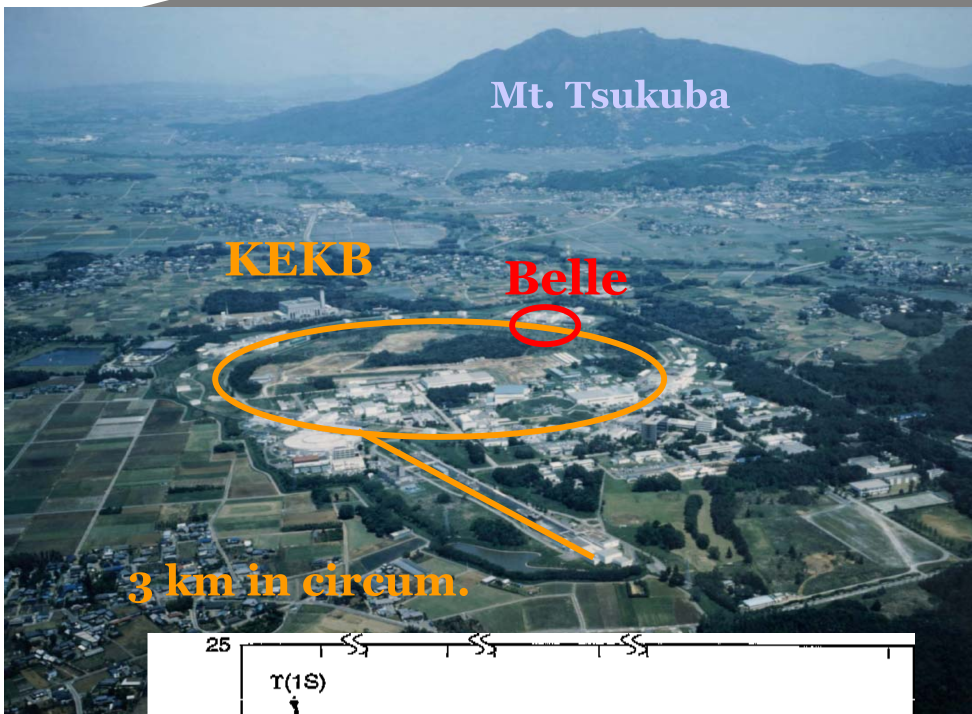
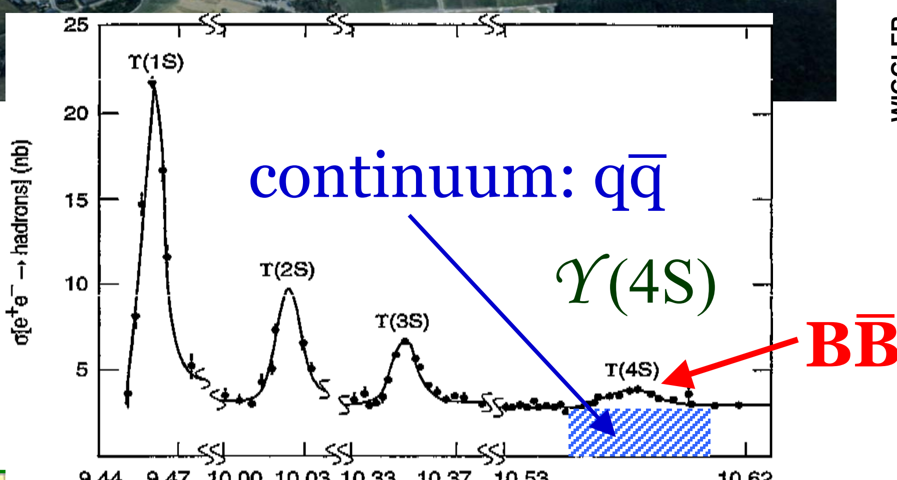
*G. Varner[1], H. Aihara[5], M. Barbero[1], A. Bozek[4], T. Browder[1], F. Fang[1], M. Hazumi[3], J. Kennedy[1], N. Kent[1], J. Mueller[7], S. Olsen[1], H. Palka[4], M. Rosen[1], L. Ruckman[1], S. Stanič[2,6], K. Trabelsi[1], T. Tsuboyama[3], K. Uchida[1], and Q. Yang[1]

[1]University of Hawaii, [2] University of Tsukuba,
[3] High Energy Accelerator Research Organization (KEK),
[4] H. Niewondiczanski Institute of Nuclear Physics,
[5] University of Tokyo, [6] Nova Gorica Polytechnic,
[7] University of Pittsburg



KEK-B asymmetric collider



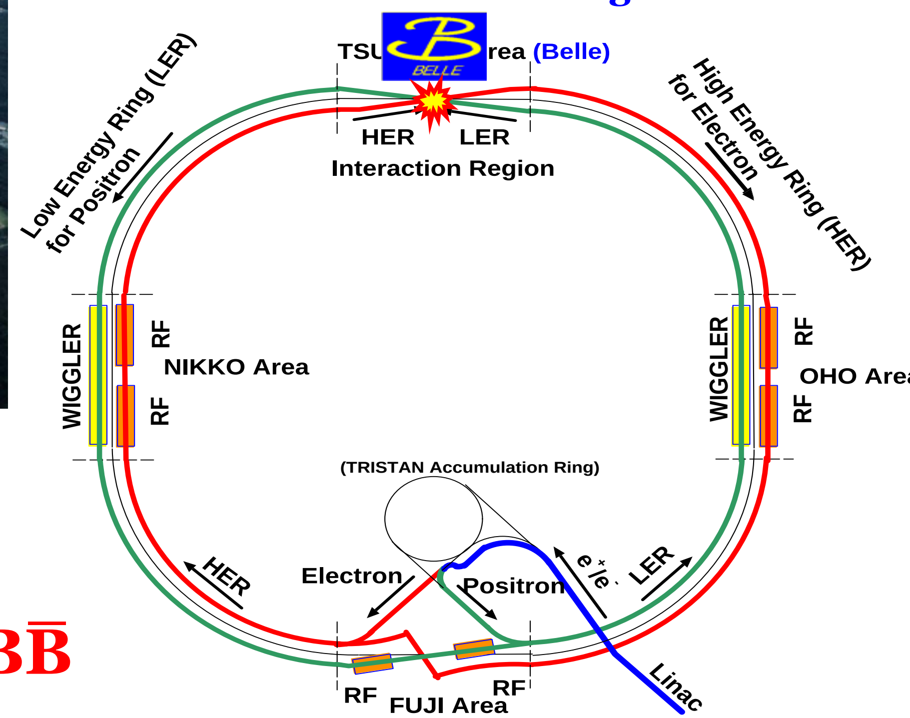


KEKB / Belle started operation in 1999

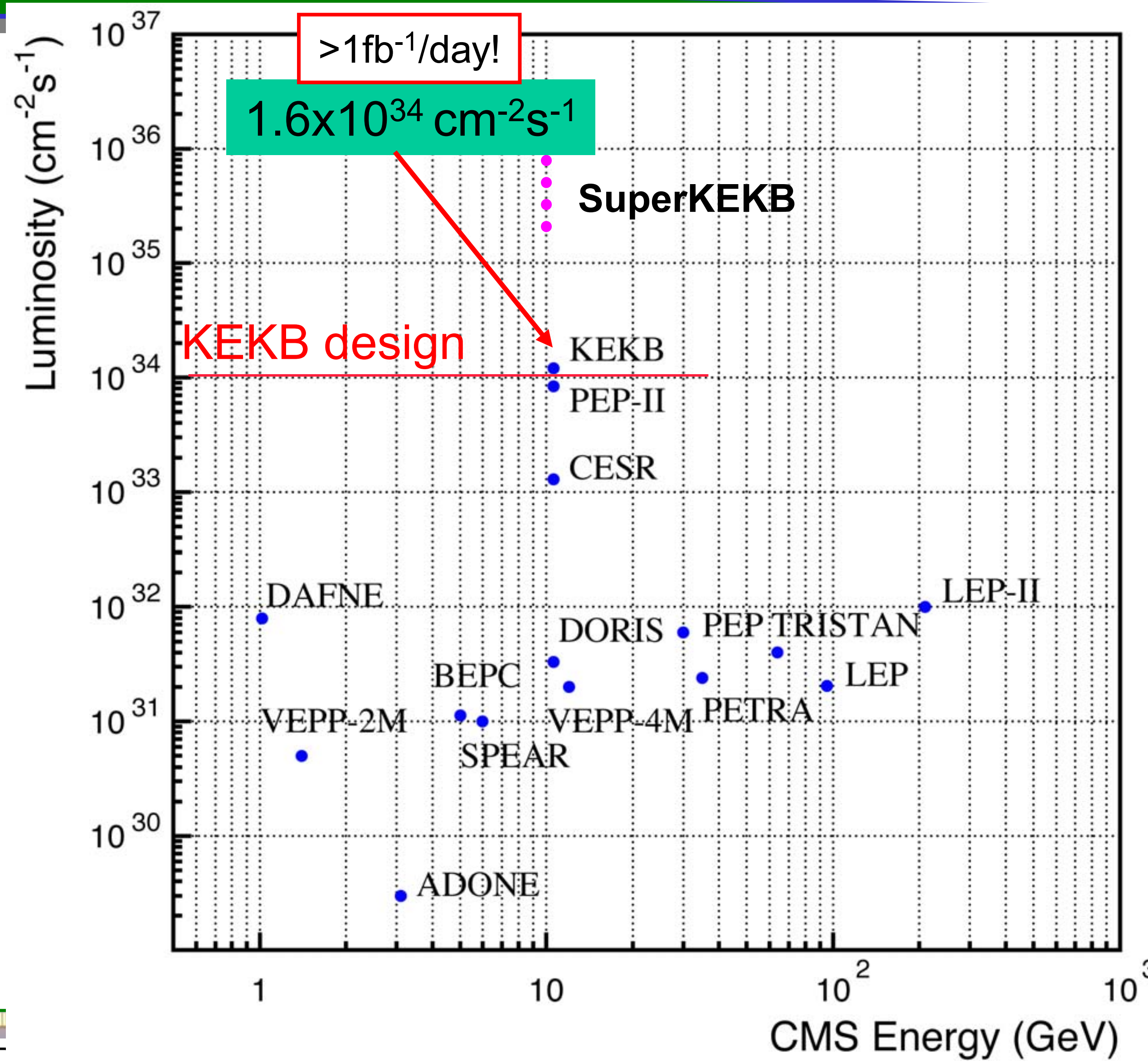
8 GeV e^- x 3.5 GeV e^+

→ $B\bar{B}$ boost !

± 11mrad crossing



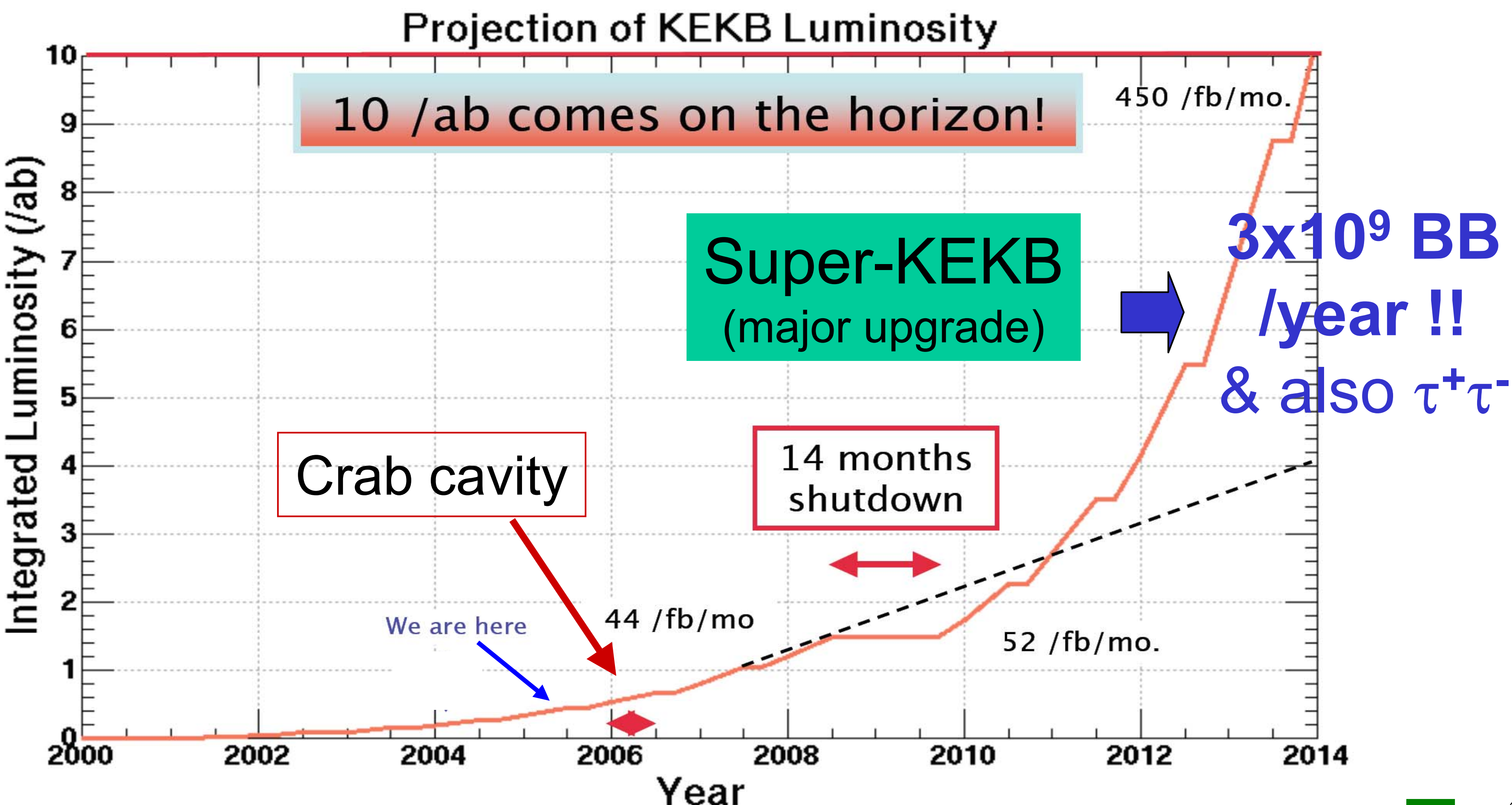
World’s Highest Luminosity Collider



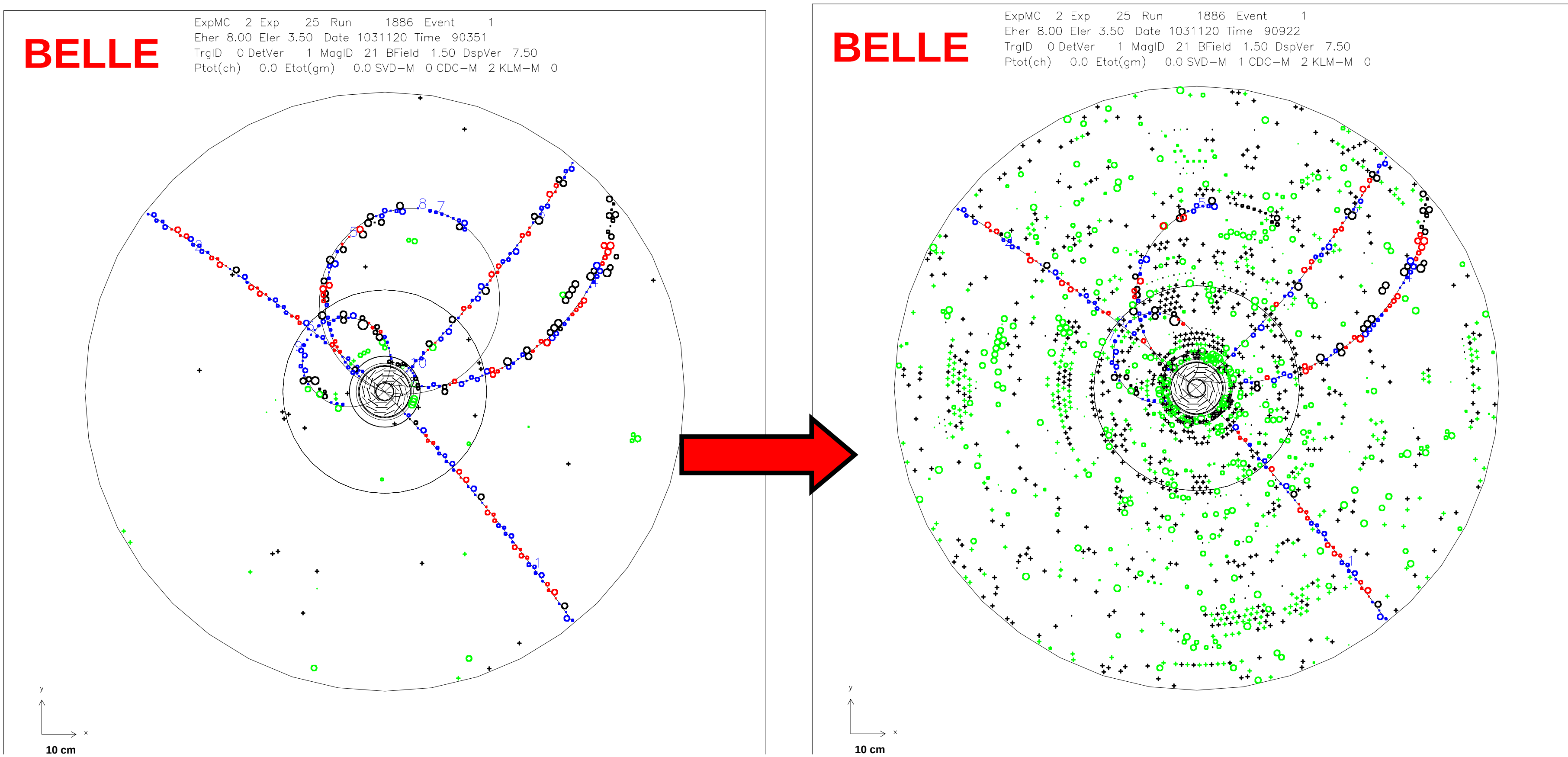
KEKB Upgrade Scenario

L_{peak} ($cm^{-2}s^{-1}$) 1.6×10^{34} → 5×10^{34} → 5×10^{35}

L_{int} 467 fb^{-1} → 1 ab^{-1} → 10 ab^{-1}



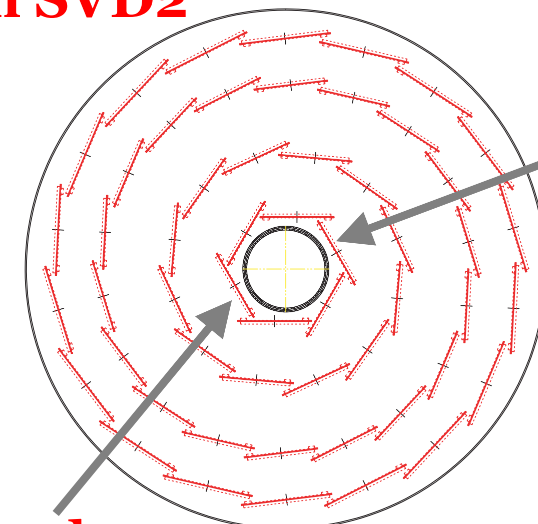
Detector Impact

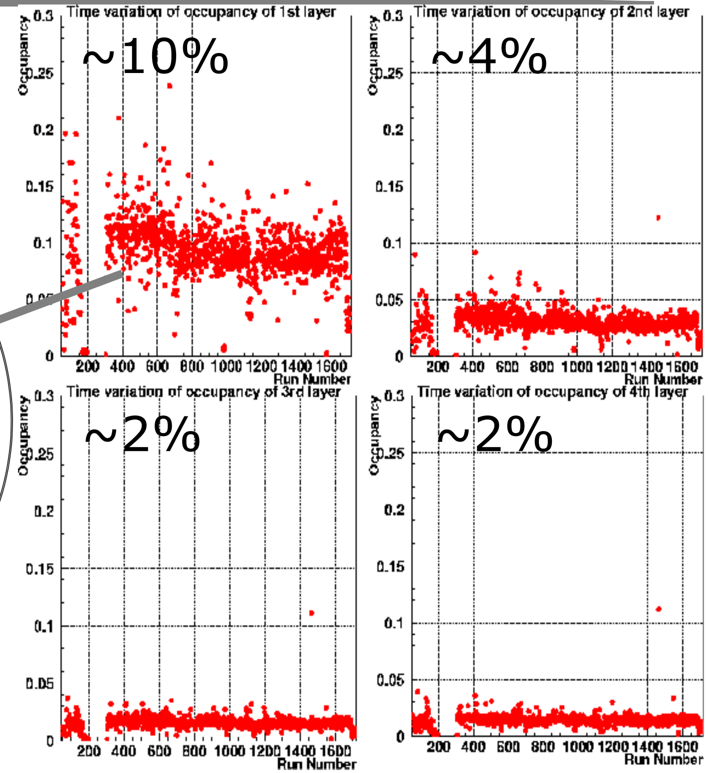


- Occupancy → x20-x50 background increase
- Many analyses aren't statistically limited → better vertexing

Occupancy in SVD2

152M $B\bar{B}$ pairs with SVD1
+ ~300M $B\bar{B}$ pairs with SVD2





Present : layer 1 of SVD

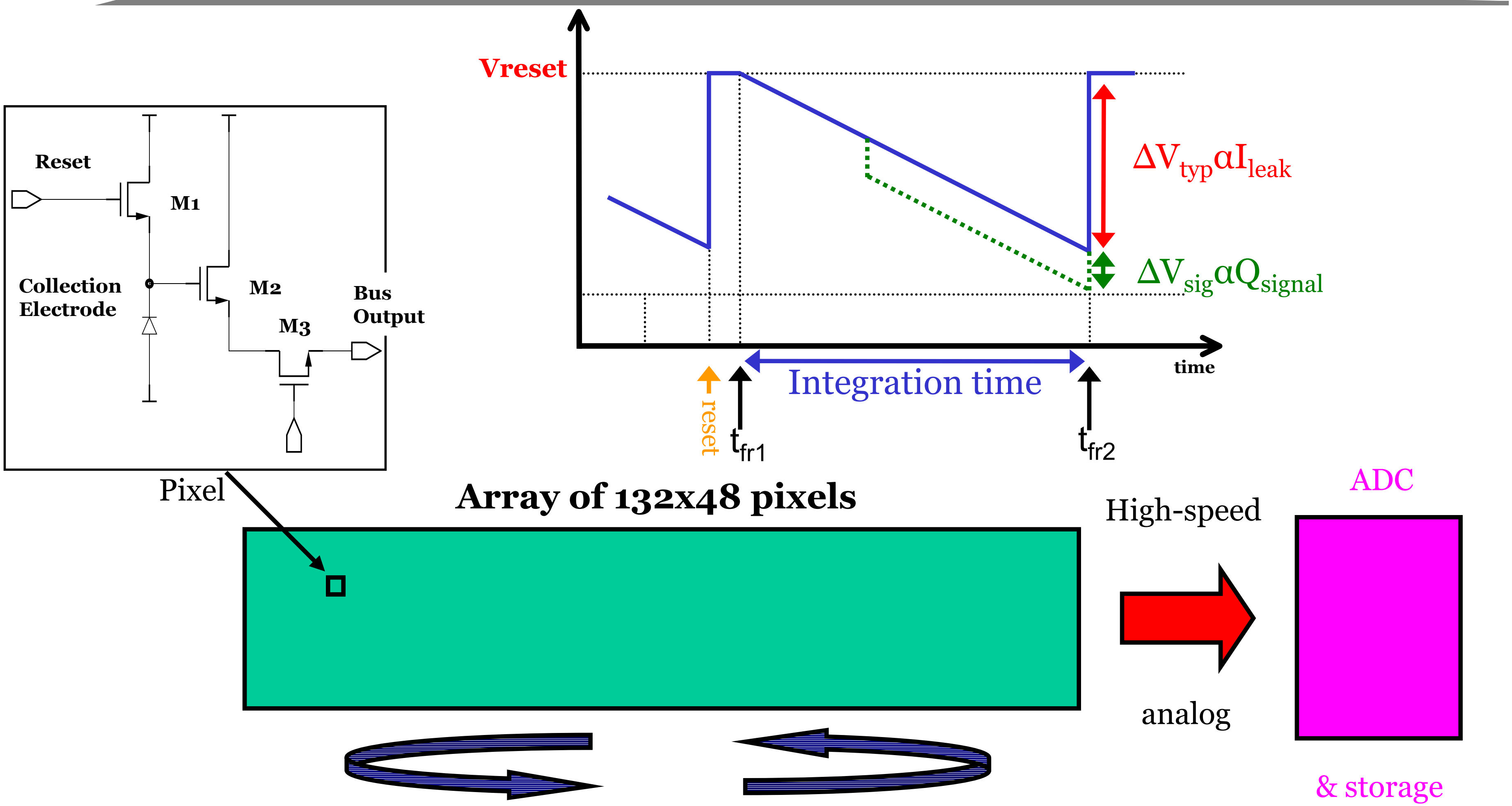
~10% occupancy / 200 Krad.yr^{-1}

Upgrade: **L~1.6x10^{34} → L~5x10^{35} cm^{-2}.s^{-1}**

Background increase typ. x20 (x50) → Occupancy / dose

Conventional solutions (Si strips) do not work → Striplet (SVD2.5)

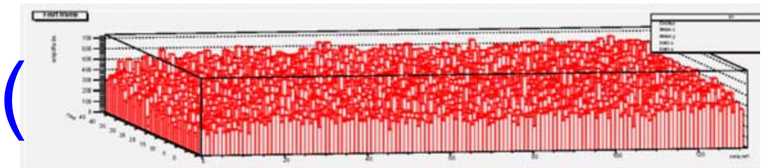
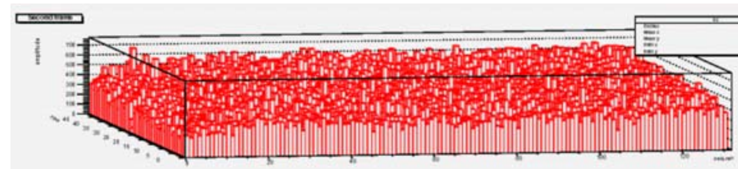
Continuous Acquisition Pixel (CAP)



Pixel Array: Column select – ganged row read

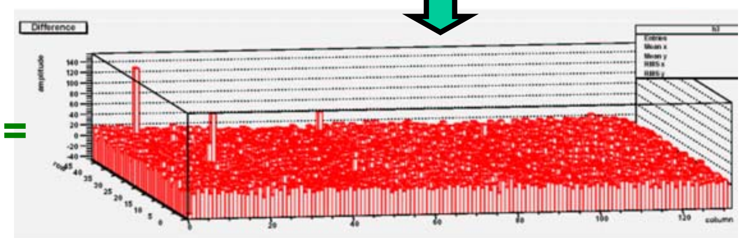
Low power – only significant draw at readout edge

Correlated Double Sampling (CDS)

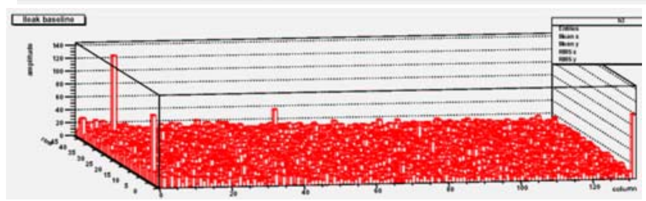
( - )

8ms integration shown

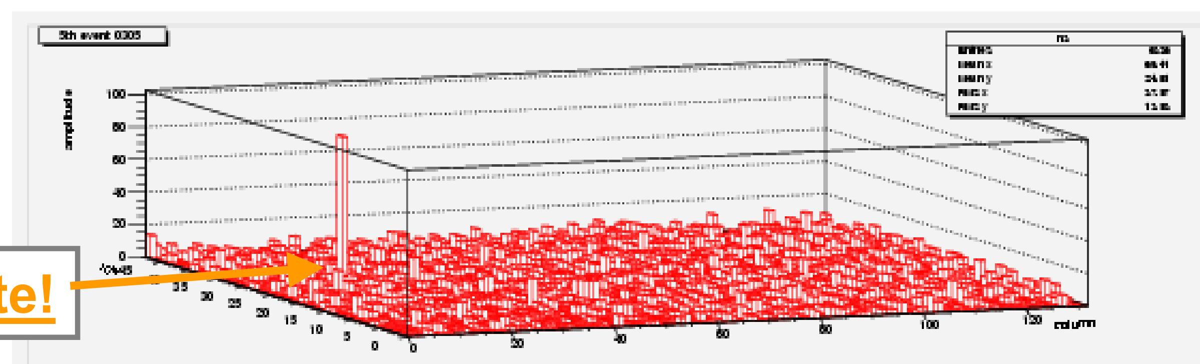
Frame 1 - Frame 2 =



- Leakage current Correction



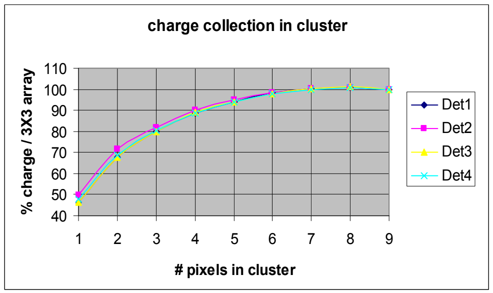
~fA leakage current (typ)
~18fA for hottest pixel shown

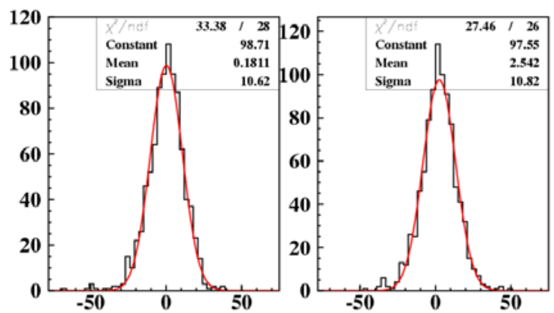


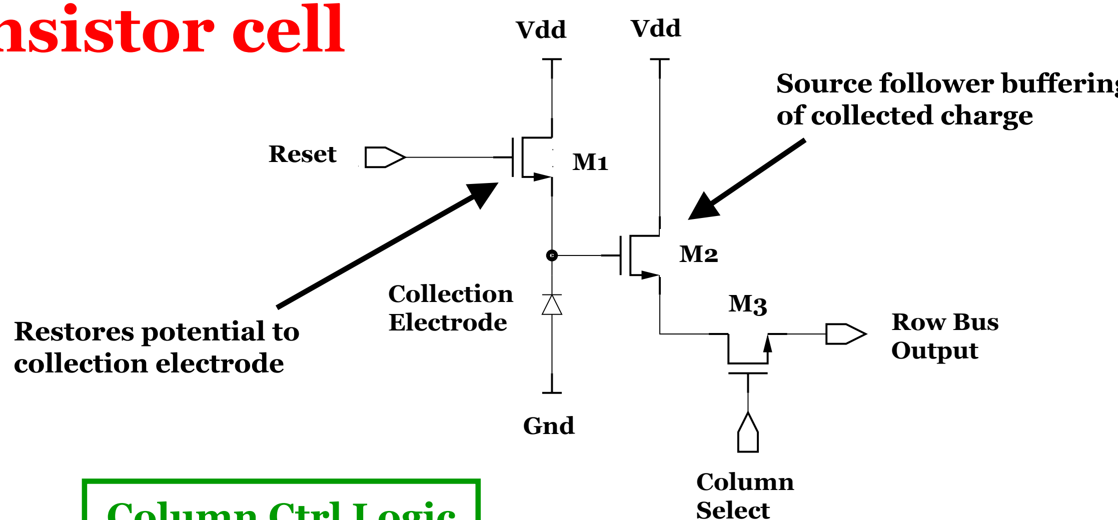
Hit candidate!

Cont. Acq. Pixels (CAP) 1 Prototype

CAP1: simple 3-transistor cell



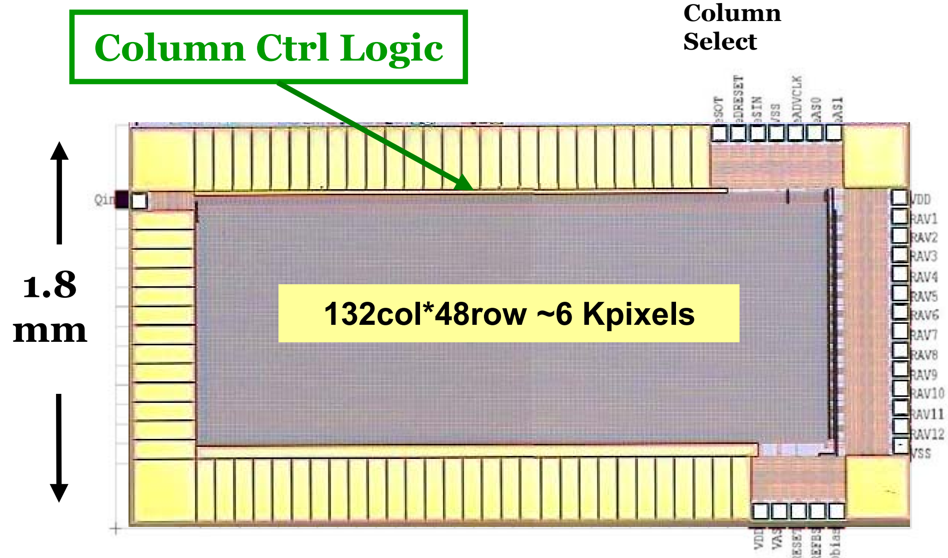




Pixel size:

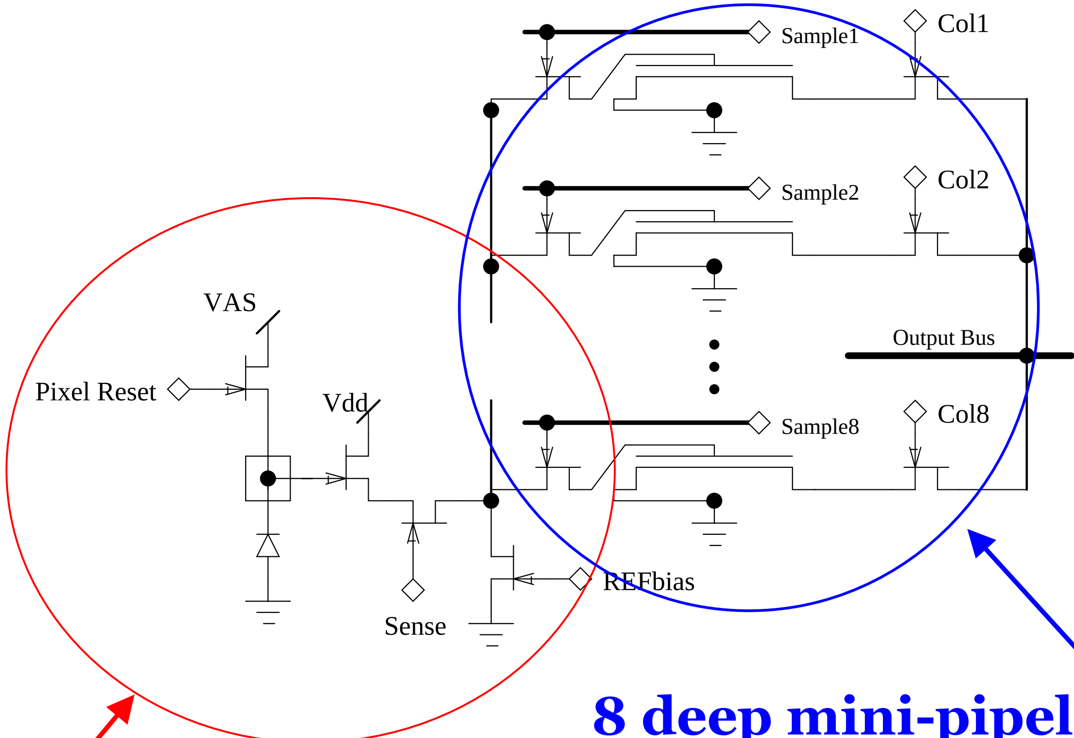
22.5 μm x 22.5 μm

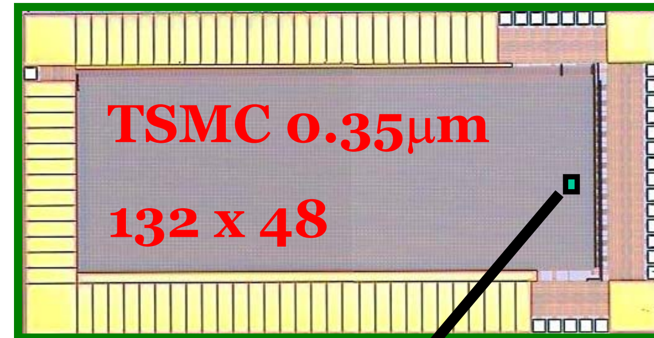
CAPs sample tested: all detectors (>15) function.

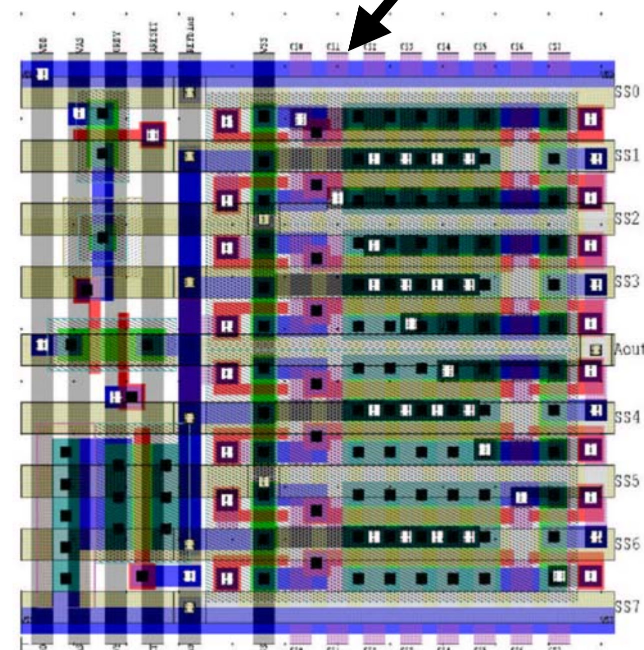


NIM A541:166-171 (2005)

CAP2 – Pipelined operation







Pixel size 22.5 μm x 22.5 μm

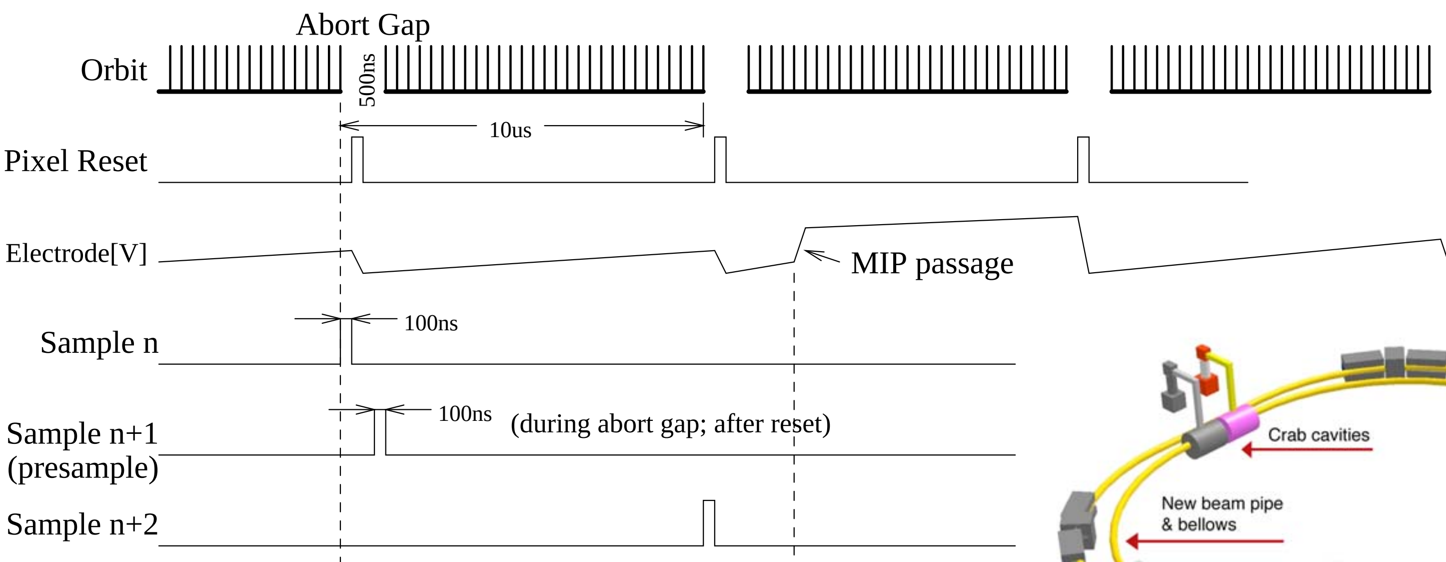
8 deep mini-pipeline in each cell

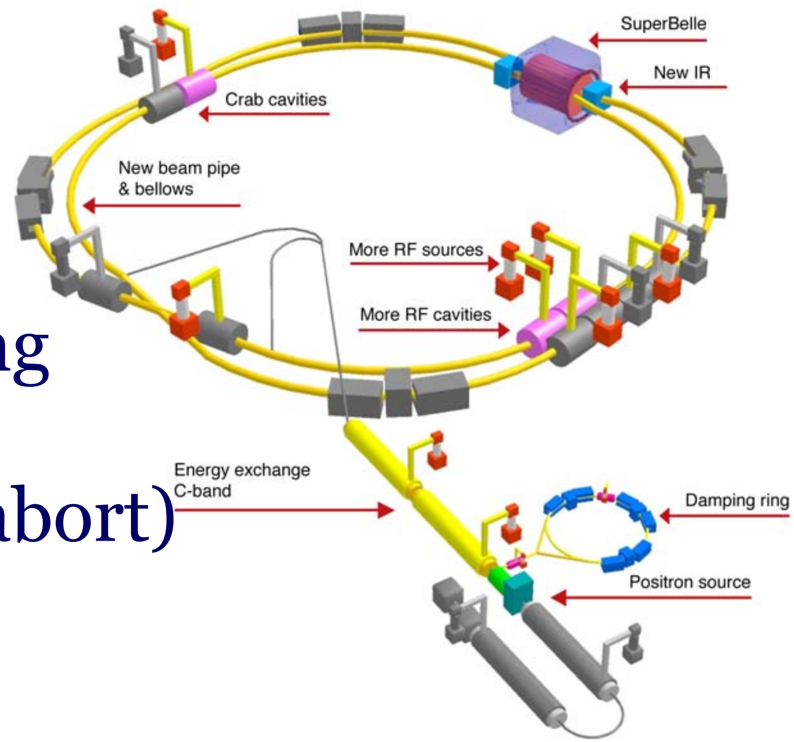
3-transistor cell

132x48=6336 channels 50688 samples

10μs frame acquisition speed achieved!

Tune for machine operation





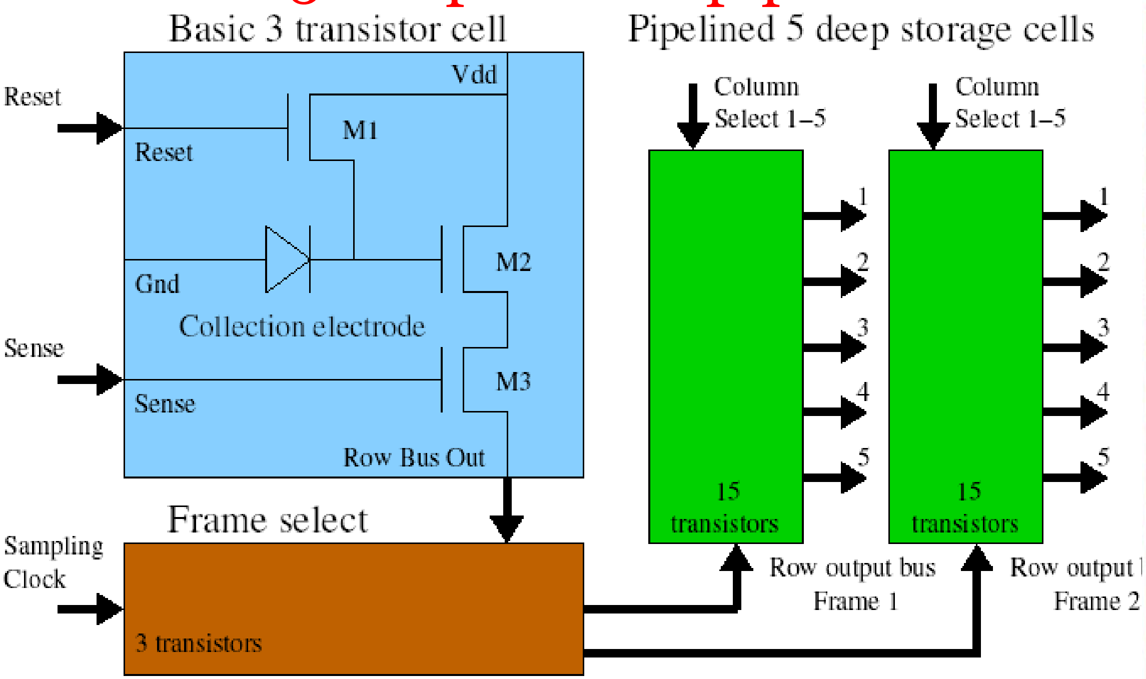
- → Up to ~4k bunches in each ring
- → Approx 2ns spacing (0.5-1us abort)
- → 4A/10A in e+/e- beam

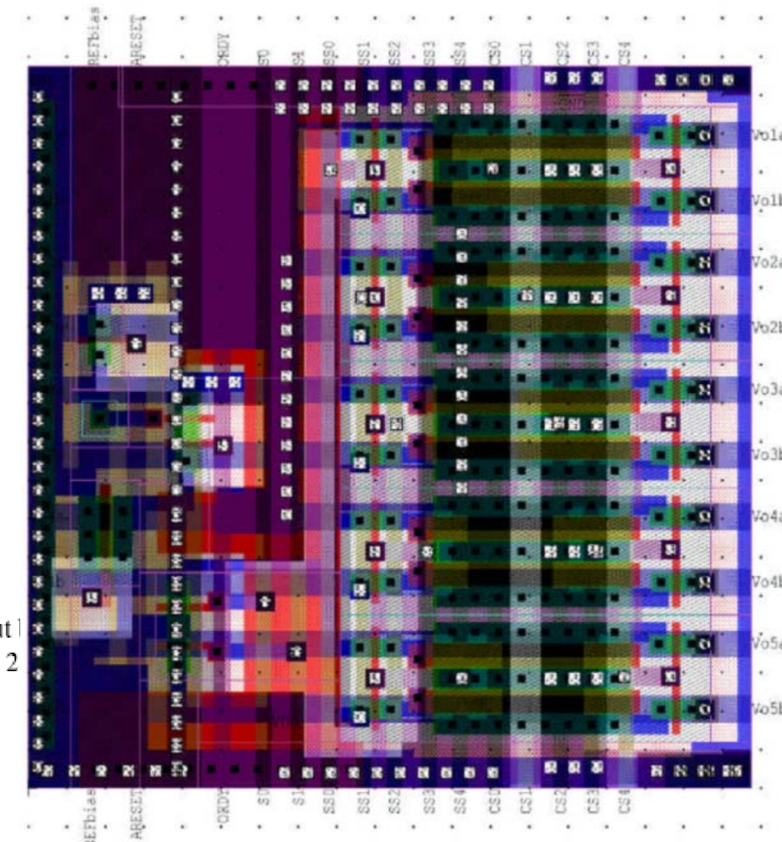
CAP3

120Kpixel sensor (128x928 pix)

TSMC 0.25μm Process

5-deep double pipeline





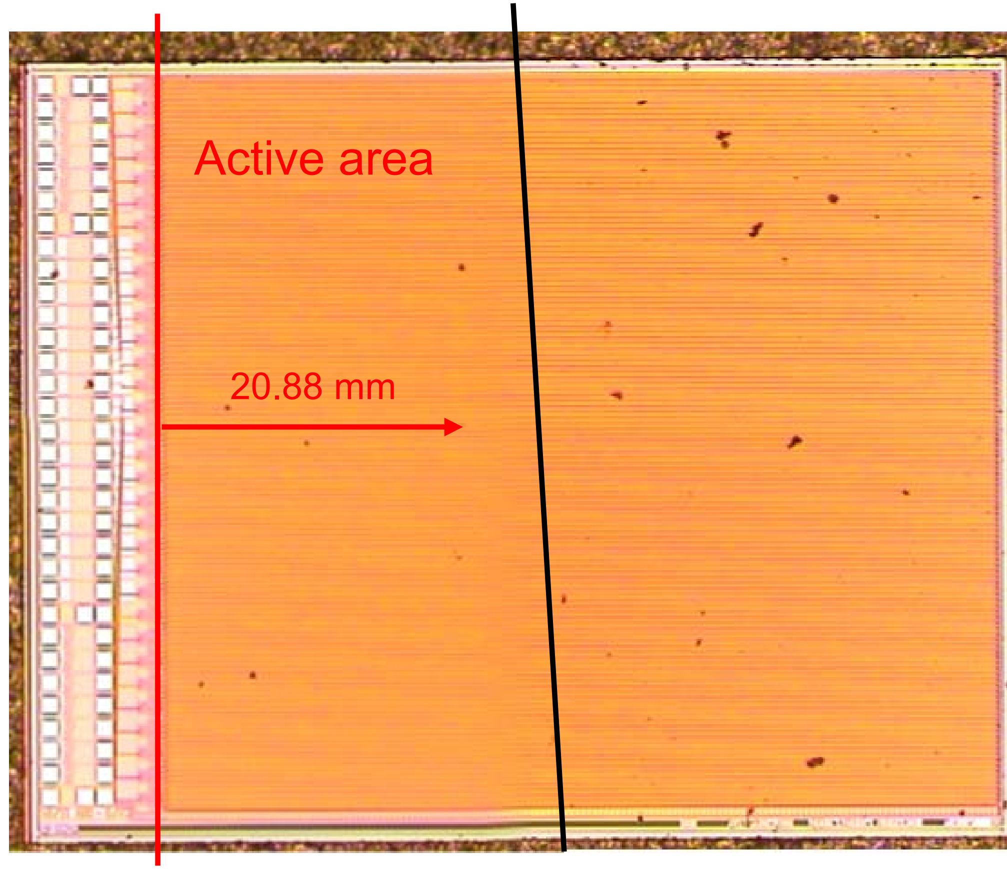
36 transistors/pixel

5 sets CDS pairs

5 metal layers

CAP3 – full-sized!

21 mm



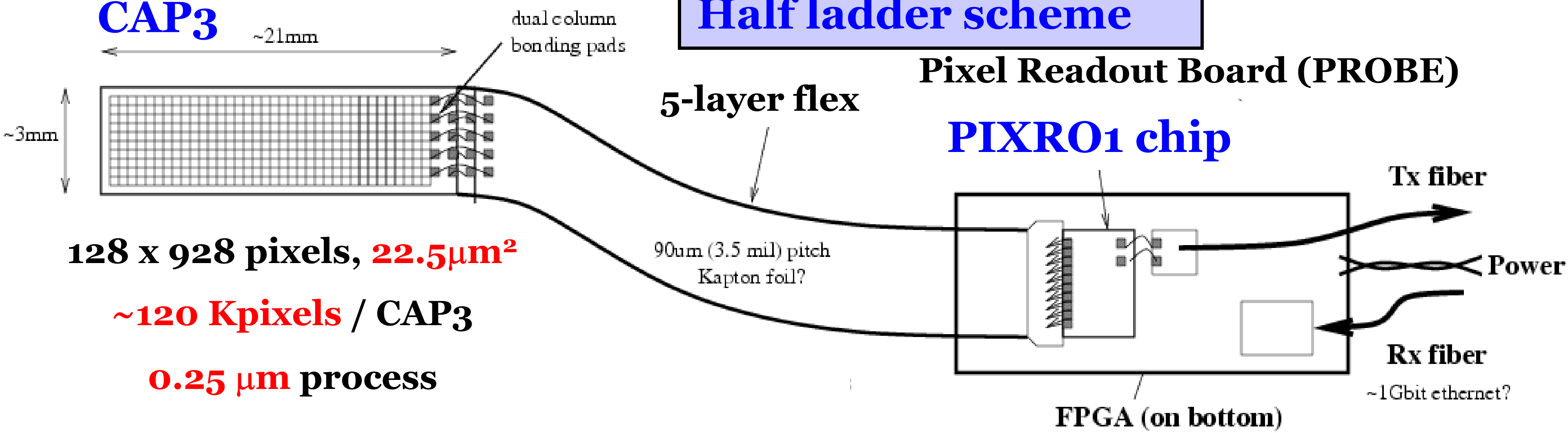
928 x 128 pixels = 118,784

~4.3M transistors

>93% active without active edge processing

CAP3: Full-size Detector

Half ladder scheme

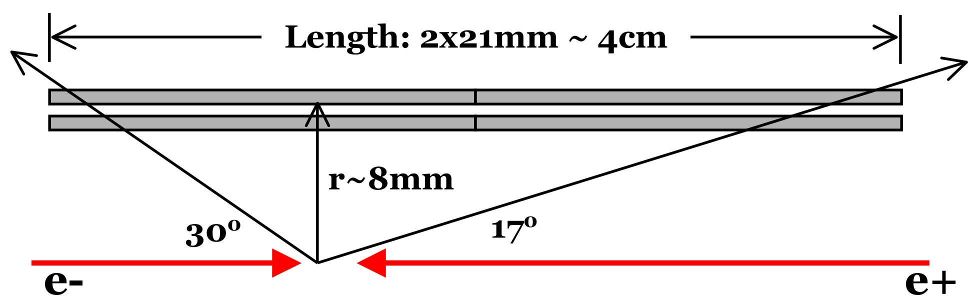


128 x 928 pixels, 22.5μm²

~120 Kpixels / CAP3

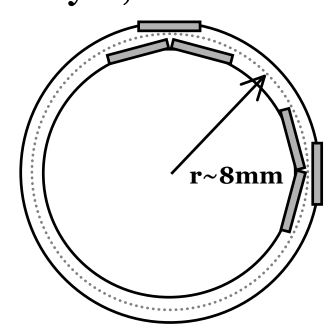
0.25 μm process

Side view



End view

Double layer, offset structure



# of Detector / layer ~ 32

CAP R&D Roadmap

Requirements

1. Low occupancy
2. Fast Readout Speed
3. Radiation Hardness
4. Thin Sensor
5. Full-sized detector

Prototypes

R&D steps

Technology Choice — XTEST2, LHC hybrid pixels

↓ MAPS

CAP1 – basic functionality — Jun. 2004 @ KEK

↓

CAP2 – pipelined readout — T943 Dec. 2004 @ FNAL

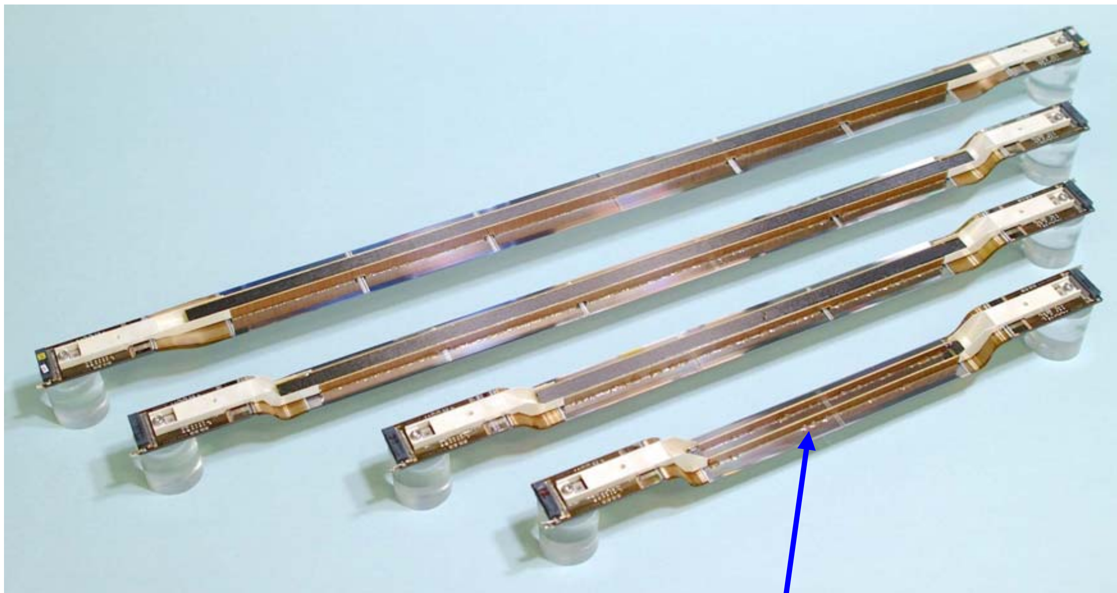
↓

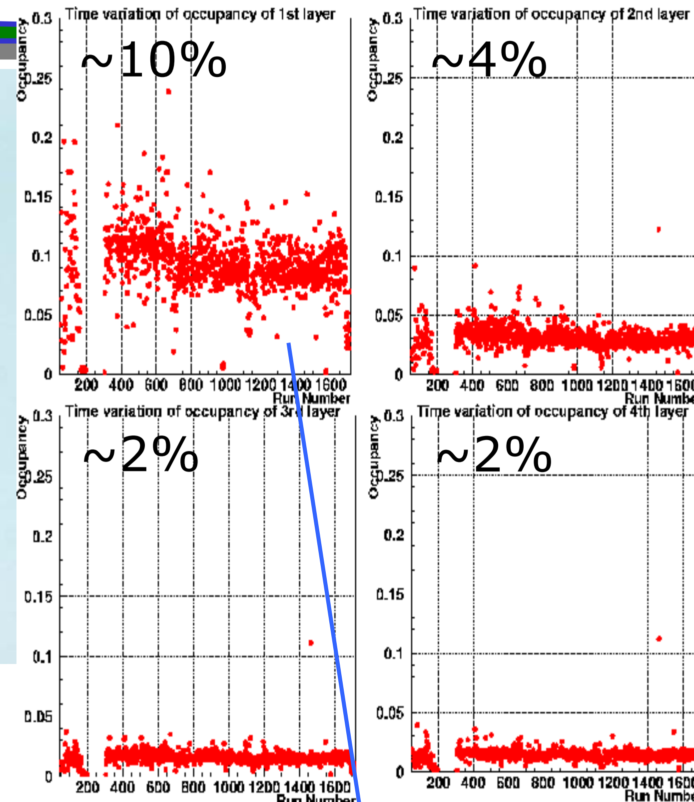
CAP3 – full-size/speed — T569 ~ Dec. 2005 @ KEK

↓ Preliminary Design Report

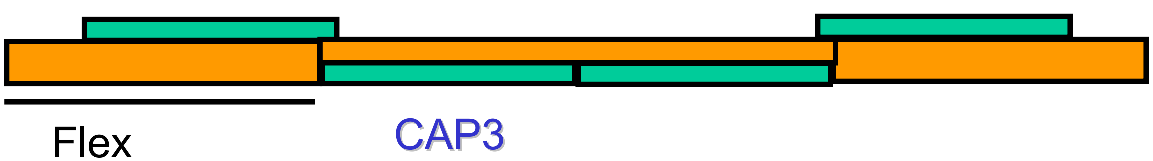
PVD1.0
- ➔ Near Term (SVD2 Layer 1 drop-in)
- ➔ IR upgrade

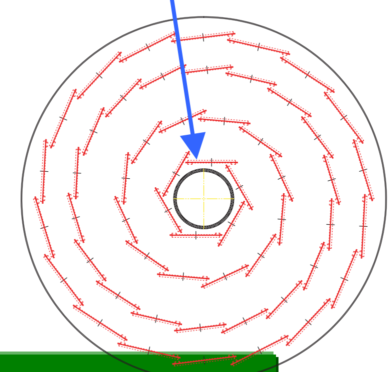
Short-term Upgrade



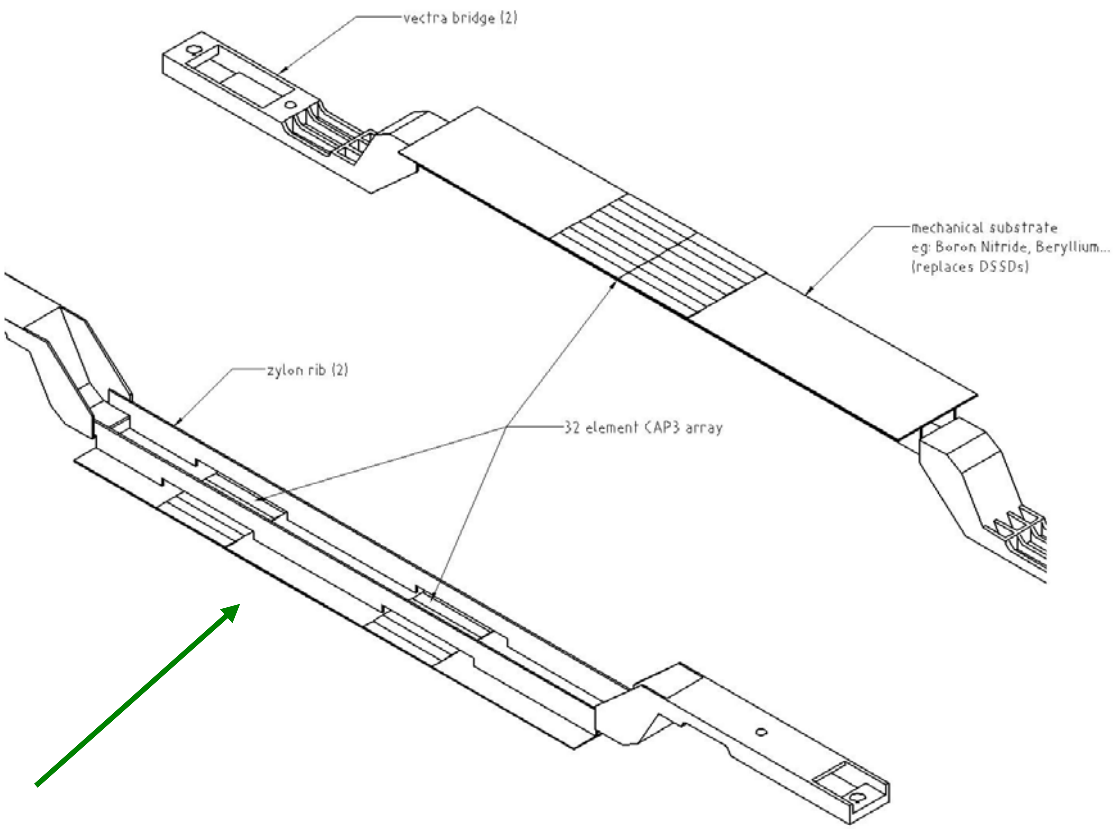


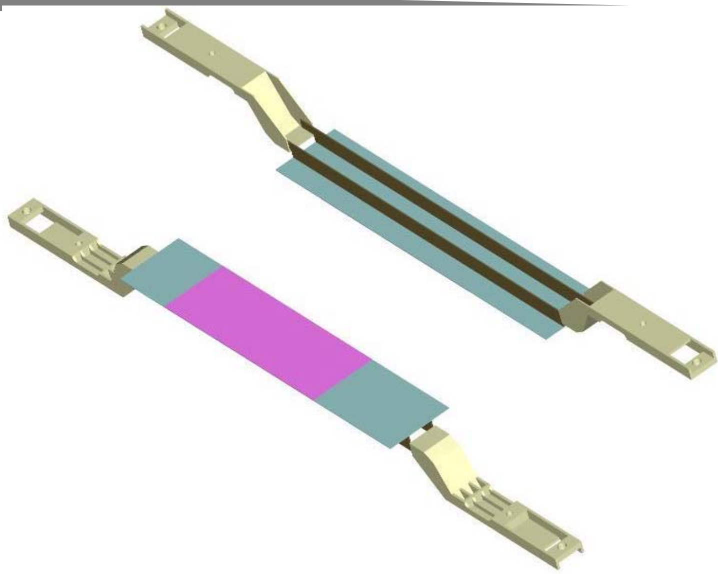
Replace Layer 1 with CAP3 pixels
Mechanically identical (drop in)





Short-term Upgrade (2)

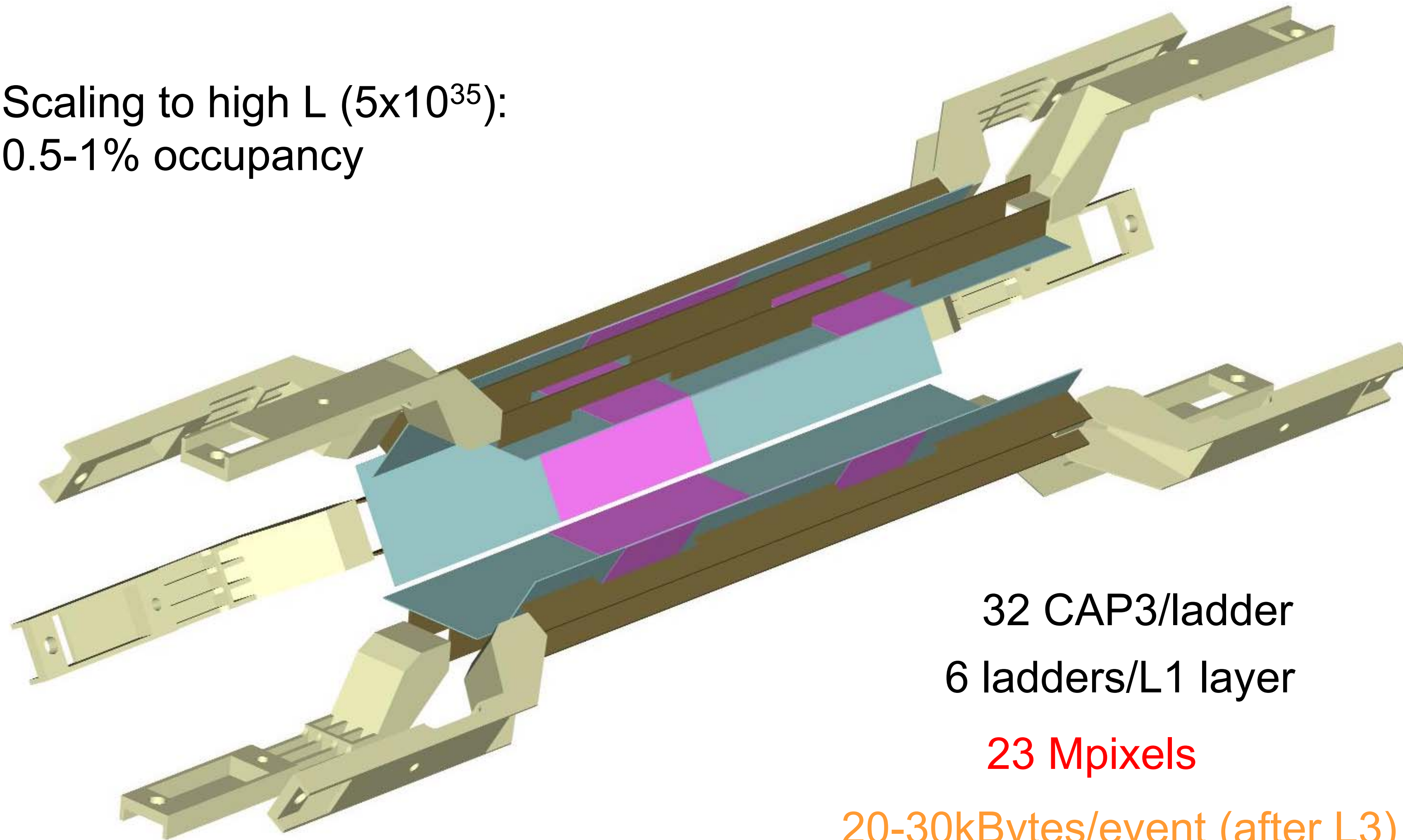




4 x 8 CAP3 basically spans Belle acceptance

Short-term Upgrade (3)

Scaling to high L ($5x10^{35}$):
0.5-1% occupancy



32 CAP3/ladder

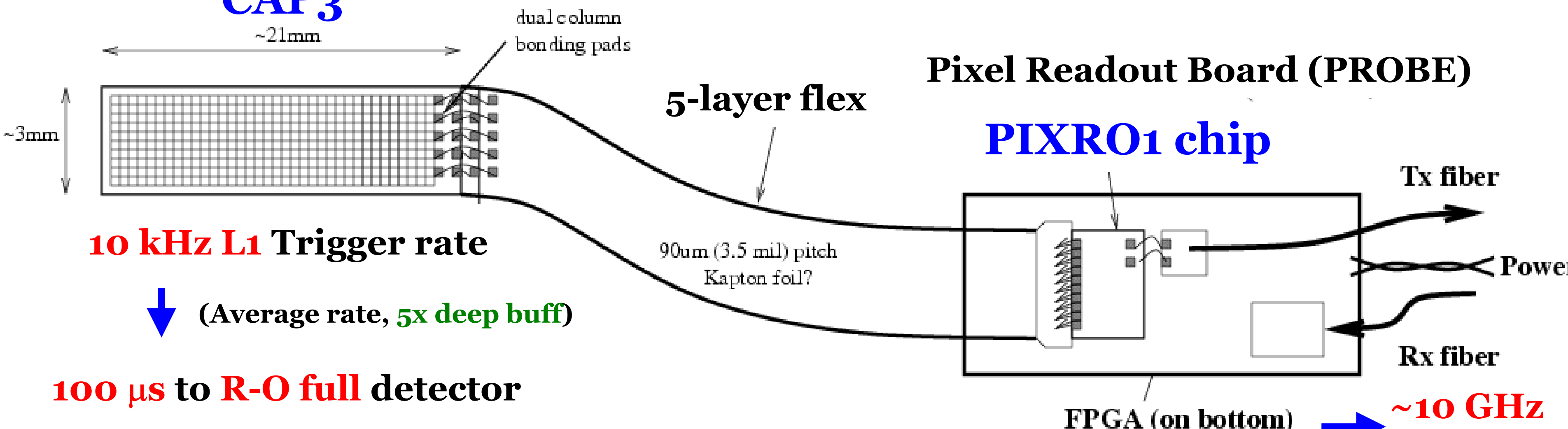
6 ladders/L1 layer

23 Mpixels

20-30kBytes/event (after L3)

Detector concept: data flow

CAP3: 10μs frame rate (experienced with CAP2)
Super-Belle: 10kHz L1 Trigger rate



10 kHz L1 Trigger rate

↓ (Average rate, 5x deep buff)

100 μs to R-O full detector

↓ (~1k column x 2samples)

100 ns / column

↓ (128 rows x2, 32 8:1 MUX)

20 ns bus settl., 10 ns/sample

→ **16 pairs of signals** (100 MHz signals) →

Differential receiver

↑ **16 CDS** (high speed analog 16:1 MUX)

1.6 GSa/s analog (6 bits)

↑

(embedded sample) → **~10 GHz analog**

Critical R&D Scorecard

1. Readout Speed

   100kHz frame rate, 10kHz L2 accept

   10μs frame OK (CAP2), CAP3 to test 100μs frame readout

2. Radiation Hardness

   >= 20MRad

   Leakage current OK (CAP2), q collection efficiency TBD

3. Thin Detector

   <= 50μm, double layer <= 200μm

   50μm mechanical dummies, CAP3 to be thinned

4. Full-sized detector

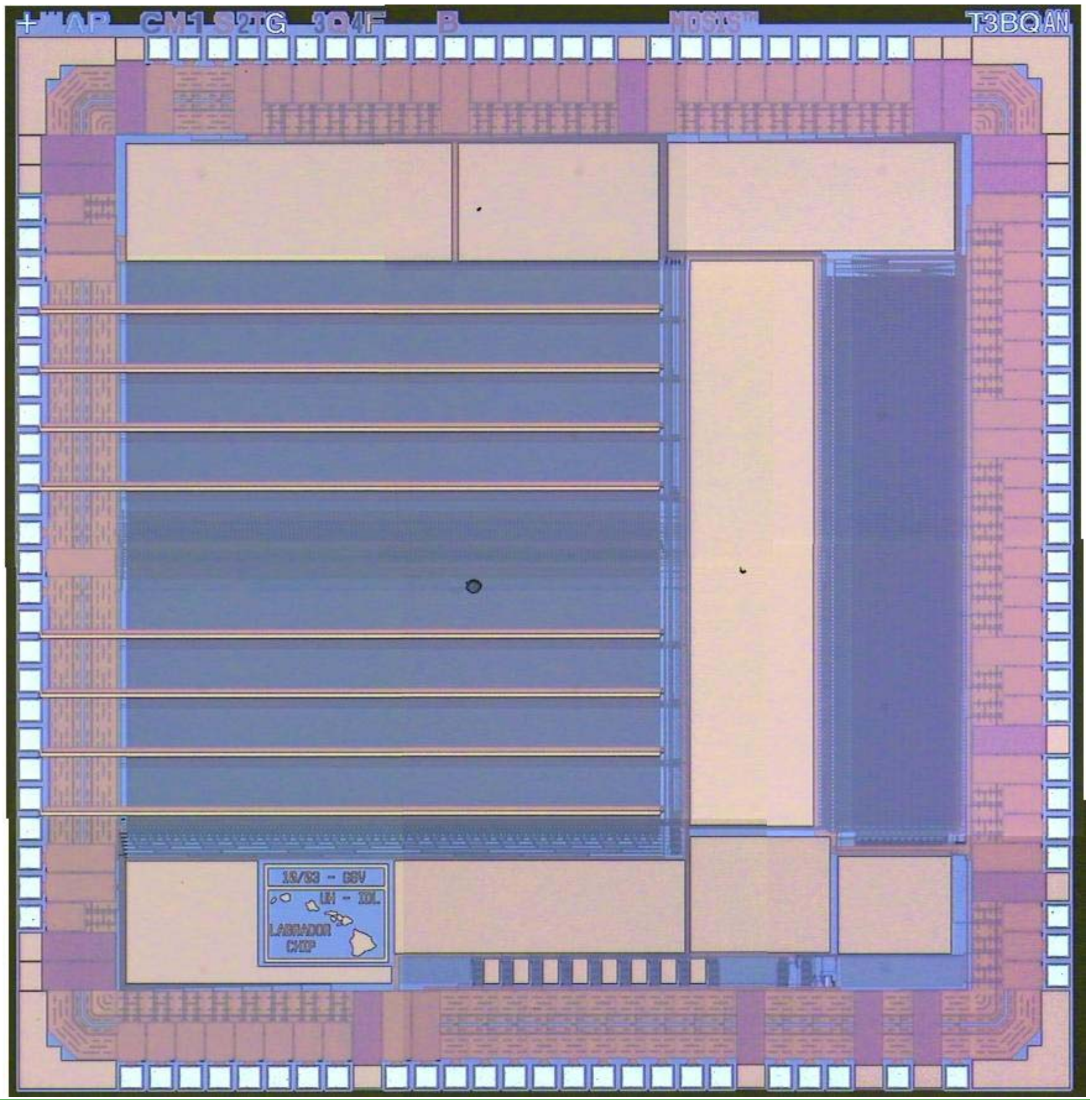
   Span acceptance (reticle limit)

   CAP3 fabricated – performance being evaluated

Summary

- Great Progress toward Pixel Vertex Detector
- Looking ahead:
  - Further testing/KEK beam test in December :
    - "ultimate" resolution, triggered/pipelined readout, SNR/hit efficiency of irradiated detectors with CAP3
  - SVD2 Layer 1 "drop in" design started
    - Exploring optical high-speed links
    - Si-Ge integration (merge CAP+PIXRO)
  - First MAPS in an actual experiment?

Back-up slides

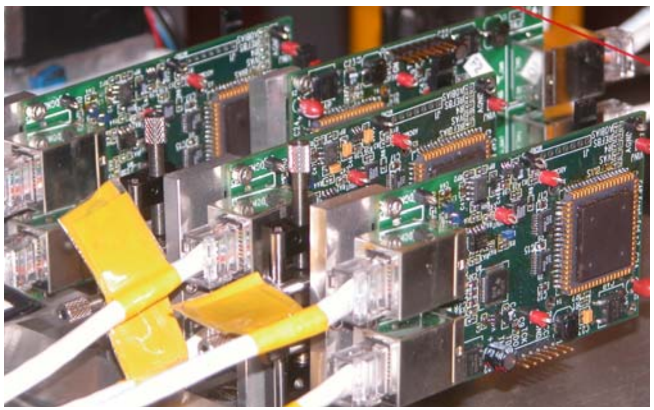


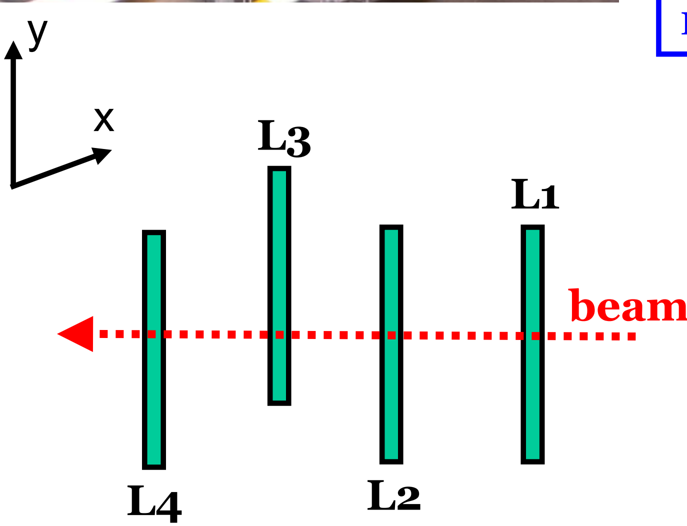
CAP Comparison

	Technology	# channels (# cells)	spatial resolution	Noise	Rad hardness I_{leak}	Rad hardness Q_{col}	Problem
CAP1	TSMC 0.35μm	6336 (6336)	<11μm (~3μm)	16e-	> 2MRad	unmeas.	too slow
CAP2	TSMC 0.35μm	6336 (50688)	unmeas. (3-4μm)	30-50e-	>=20MRad	unmeas.	poor power
CAP3	TSMC 0.25μm	118,784 (1.18M)	**TBD** (3-4μm)	**TBD**	**TBD**	**TBD**	**TBD**

Mechanical alignment

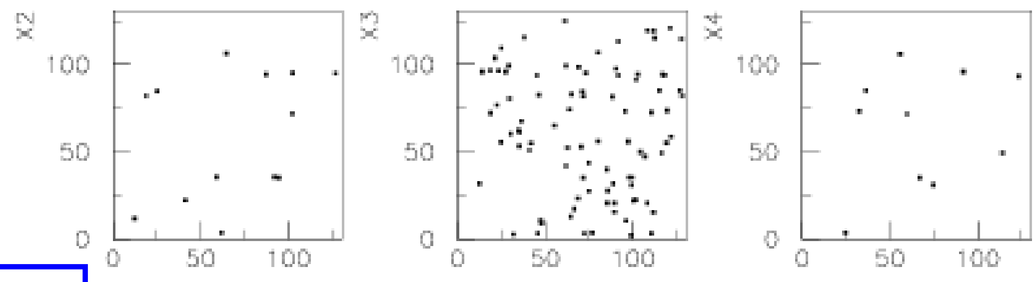
~1mm x 3mm “rice grain”





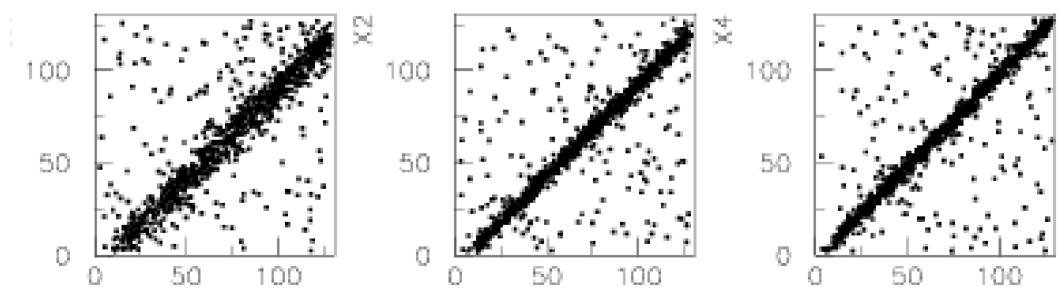
Initial Det. /Det. correlations

Det.3 vs. Det.1 **Det.3 vs. Det.2** **Det.3 vs. Det.4**

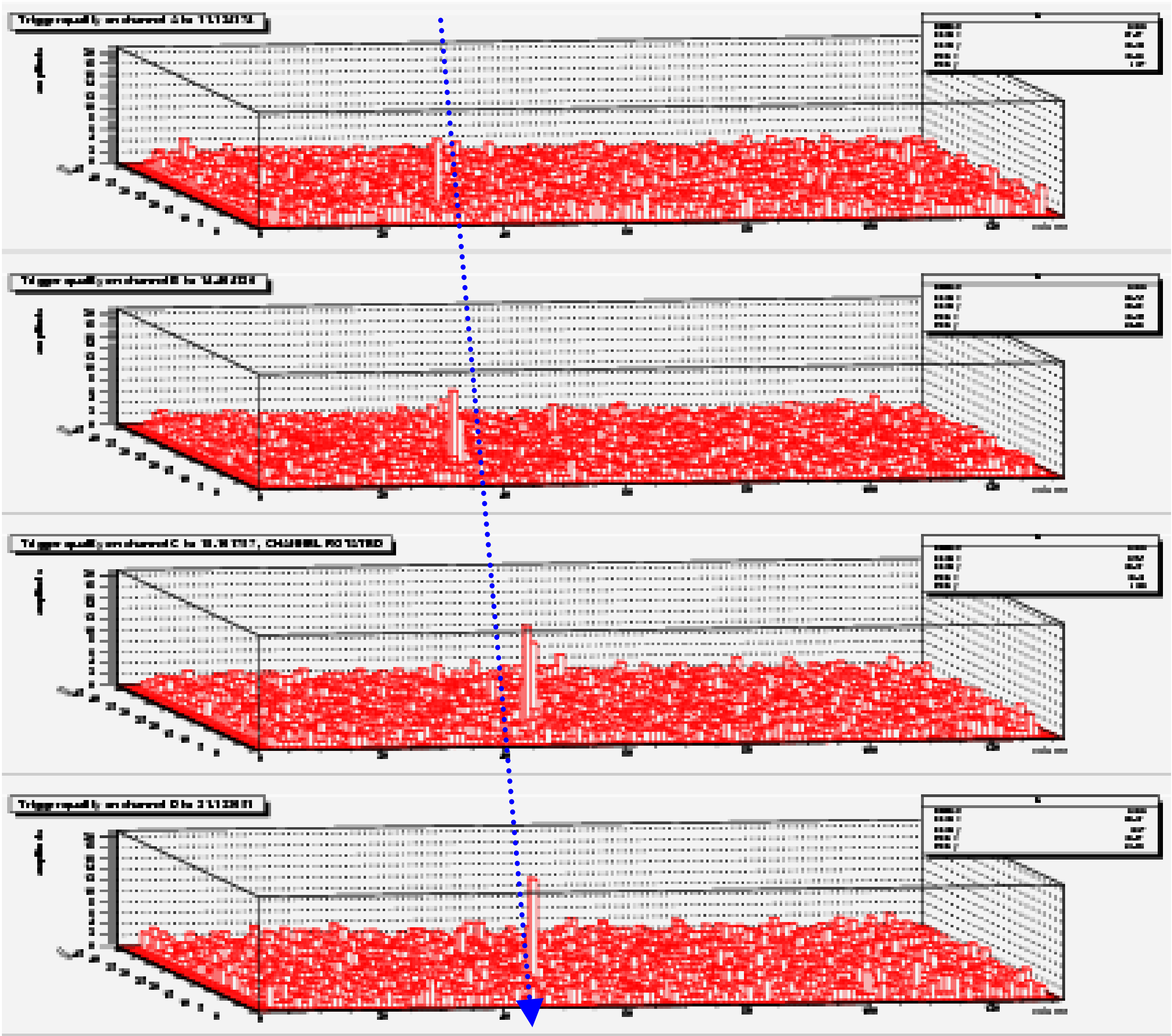


In X

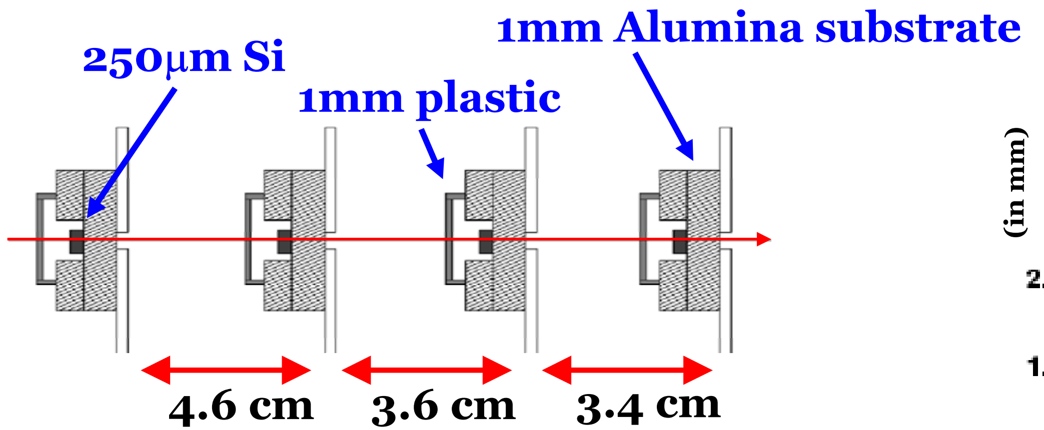
Improved correlations

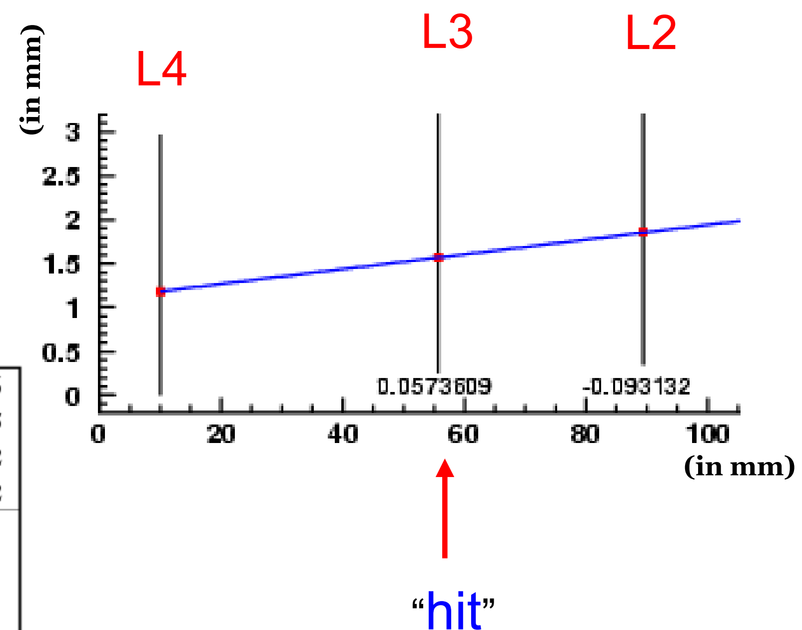


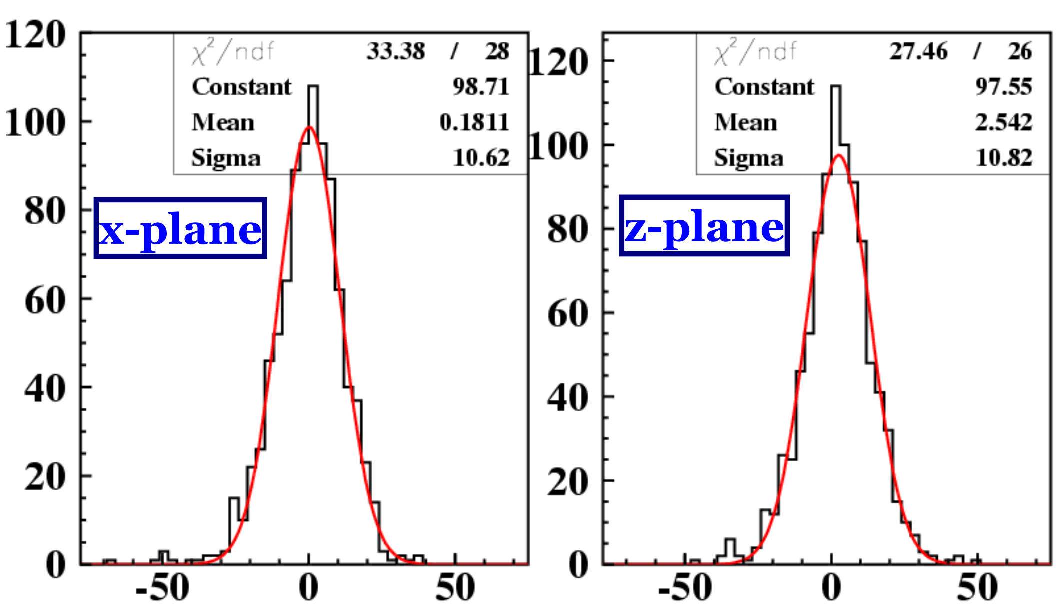
Hits! alignment proof



Hit resolution measurement







Residuals for 4GeV/c pions:

- <11μm (in both planes)

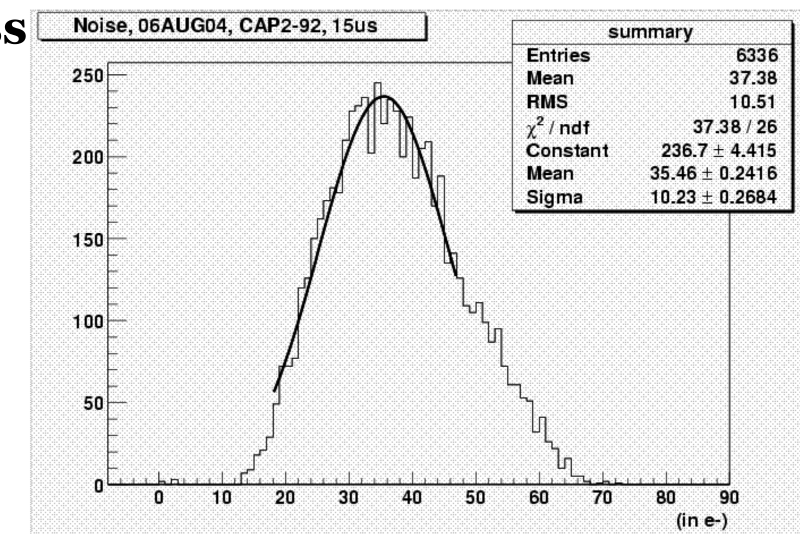
Increased readout speed: CAP2

15μs operation of CAP2:

Current status:

- **Noise higher than what is observed with CAP1/F2/B2 (~30 to 50e- vs. 16e-). Related to digital activity → better shielding**
- **Mini-pipeline output level dispersion rather large → Larger storage cells**
- **CAP2 testing demonstrated weakness Bus voltage drops during readout → Improved power routing**

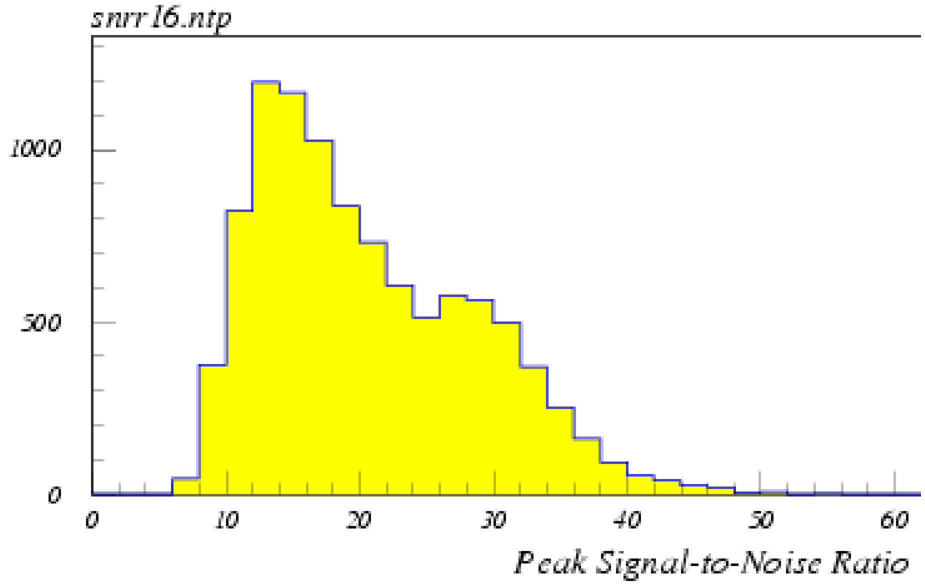
Items improved in CAP3

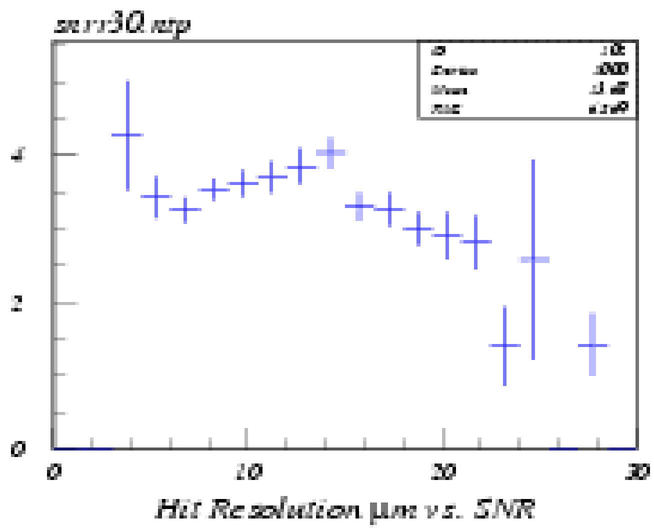


Hit resolution vs. SNR MC

<u>Toy MC:</u>

1) Generate random impact parameter
2) Landau fluctuation of signal
3) Charge diffusion (thermal)
4) Add noise (16e-/30e- system)
5) CoG of hit calculation



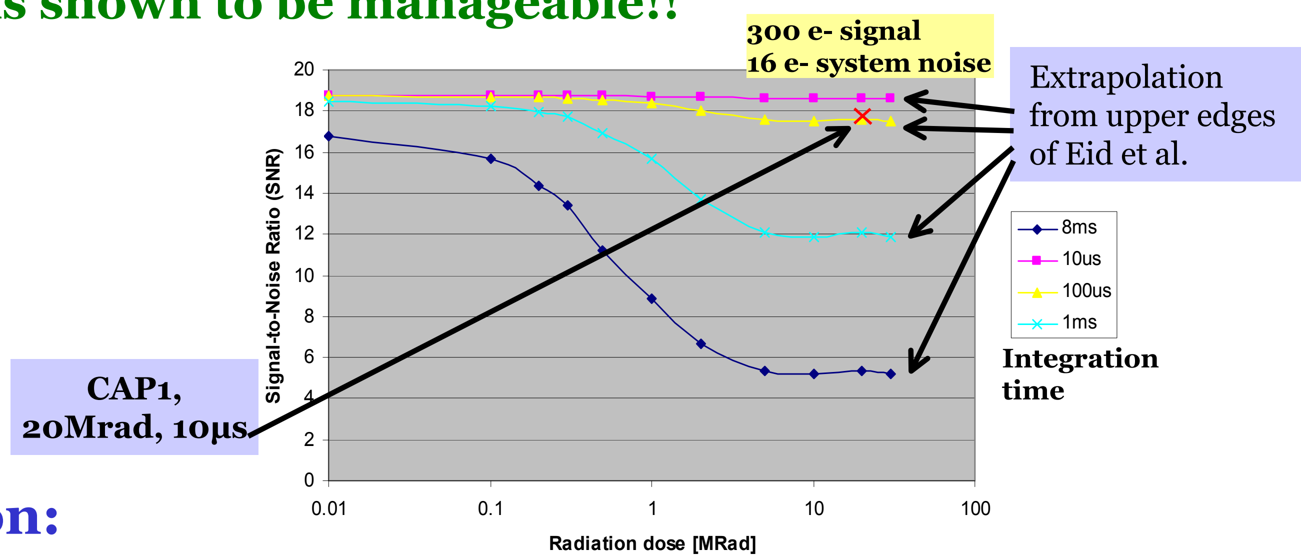


<u>Good hit resolution even at low SNR</u>

Note binary limit:
22.5µm/sqrt(12) ~6.5µm

Status of irradiation studies

- **Leakage current:**
  - **At 200 krad, leakage current increase a factor ~10. At 20Mrad, leakage current increase a factor ~10000 (fast dose)**
  - **Annealing of detector reduces Ileak 1-2 orders of magnitude**
  - **In simul, the contribution of the leakage current to the SNR degradation is shown to be manageable!!**



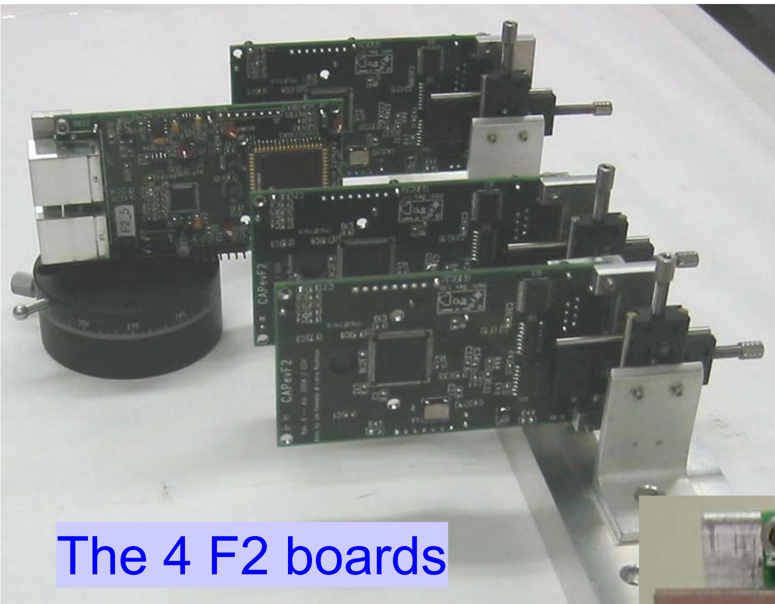
- **Signal collection:**
  - **Bulk damage → trapping centers → signal loss.**
  - **To be studied in a beam test.**

Occupancy Scaling

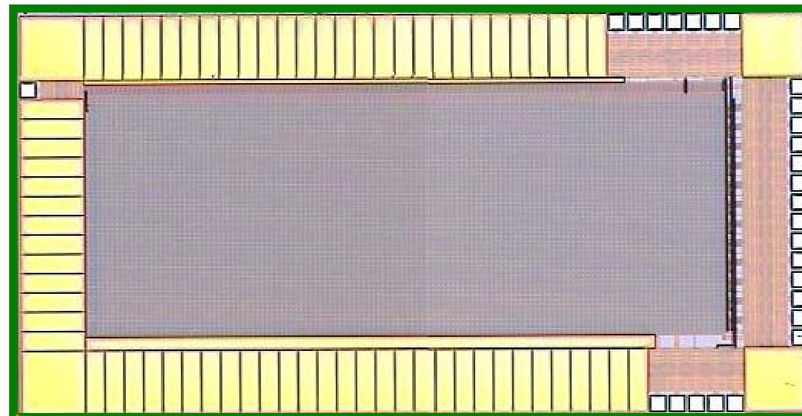
- Work from following assumptions:
  - Super-B canonical x20 background increase
    - Assume 10% Layer 1 occupancy as "current"
    - Strip area (L1) = 85mm x 50μm = 4.25M μm^2
  - Pixel spatial reduction:
    - Pixel area = 22.5μm x 22.5μm = 506 μm^2
    - Reduction factor ~8400
    - Low E γ, reduced cross-section (~3% active thickness)
  - Pixel temporal loss:
    - 0.8μs SVD vs. 10μs PVD (could be improved)
    - Increase factor ~ 12.5
  - Grand total:
    - 10% * 20 * 8400^{-1} * 12.5
    - Can expect ~ 0.3% occupancy (no ghosting)

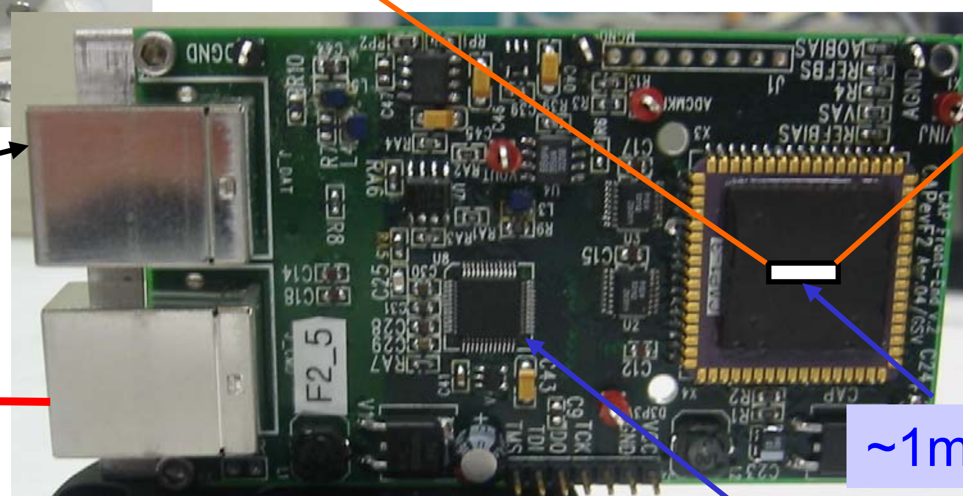
CAP on Front-End Board

Pixel chip: 132x48=6336 channels



The 4 F2 boards





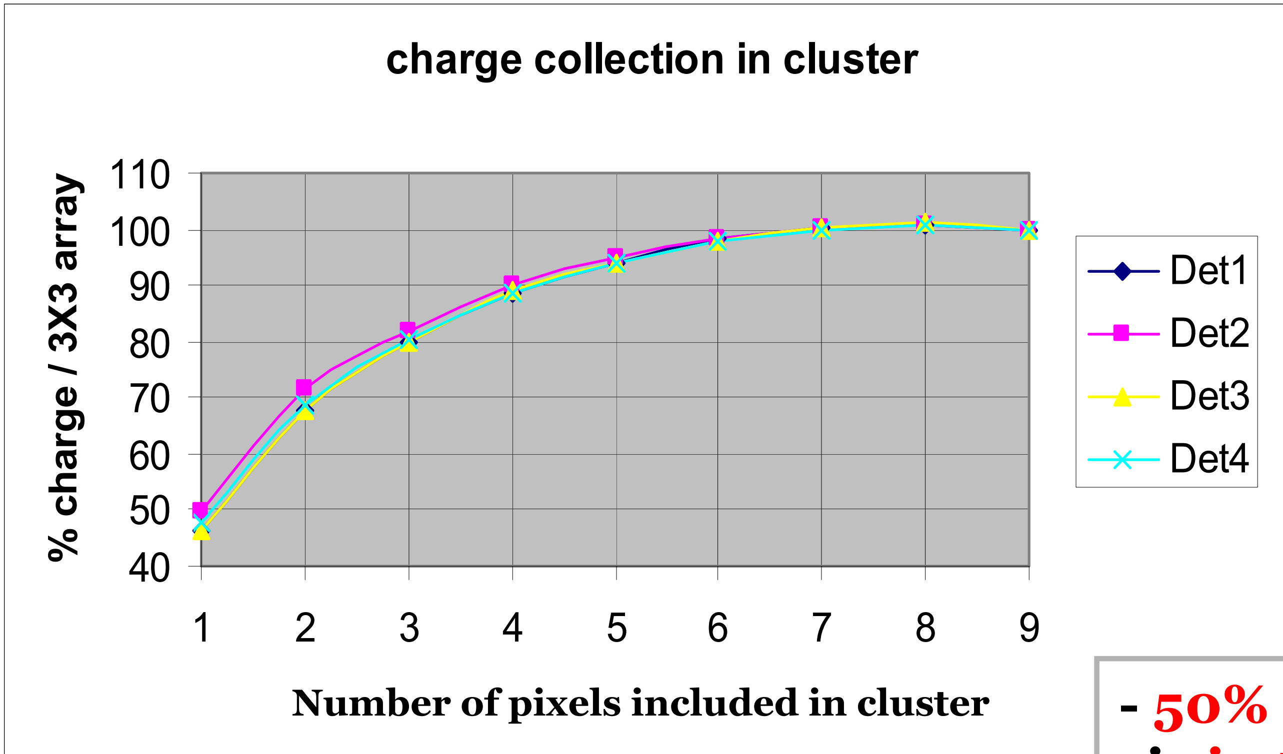
All LVDS digital I/O

300-600Mbaud link

~1mm x 3mm

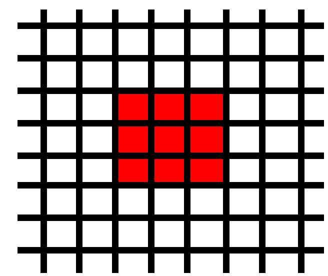
On board ADC

Charge Spread in CAPS



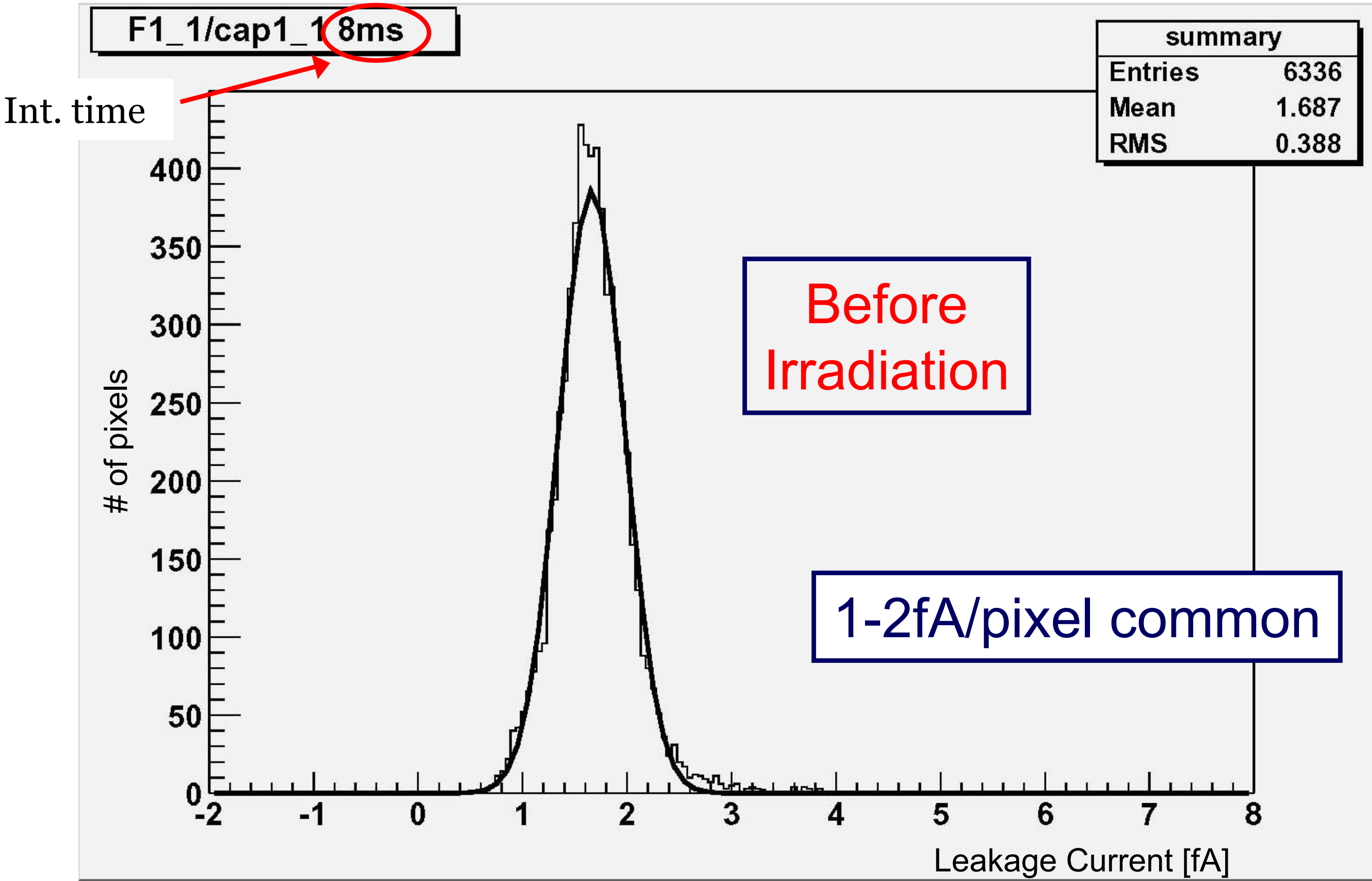
(MPV of landau fit)

Hyp: charge entirely collected in 3X3 pixel array.



- **50% of the charge is in the peak pixel.**
- **90% in the 4 largest.**

Leakage Current



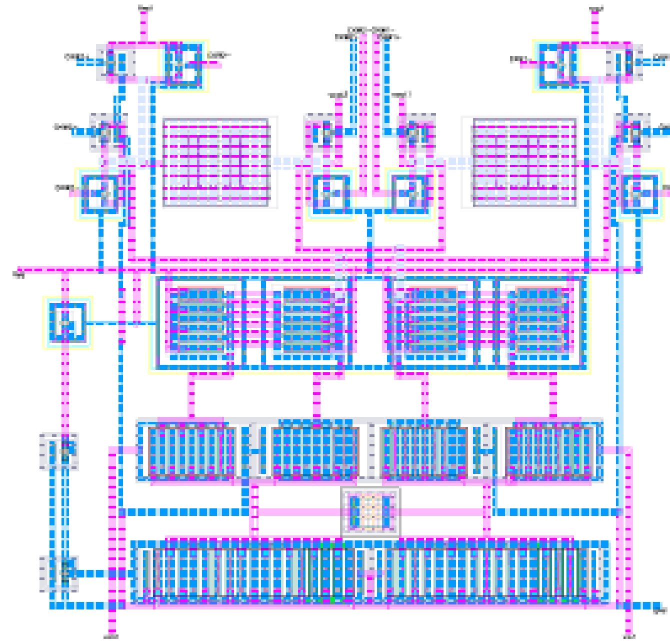
PIXRO1(1): Output Amplif.

<u>In development at present time</u>: **PRELIMINARY**

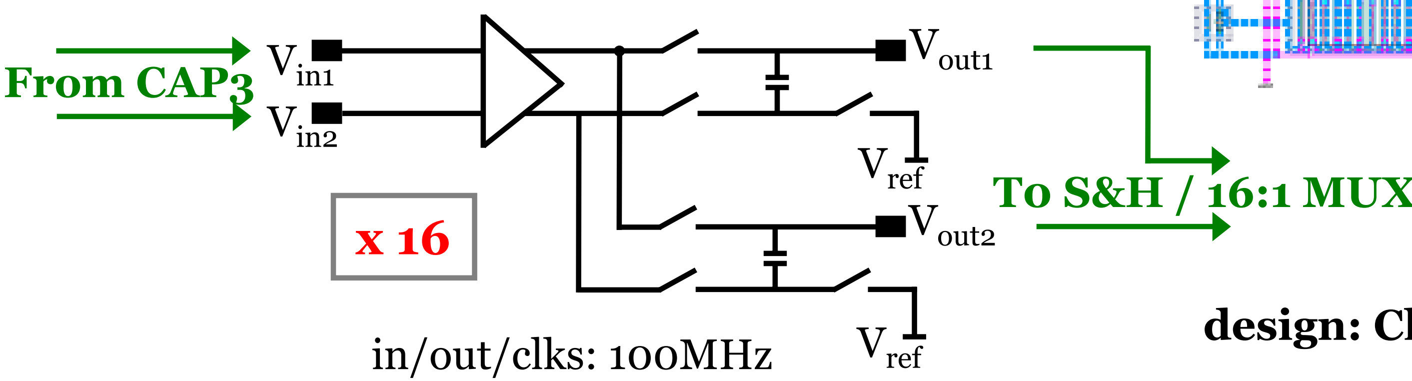
1 CAP ⟷ 1 PIXRO1

SiGe 0.5µm process from IBM

First version of PIXRO chip:
(relative) simplicity



Amplifier: Diff→Single Ended (fr2-fr1)



design: Chenyan Song (UH)

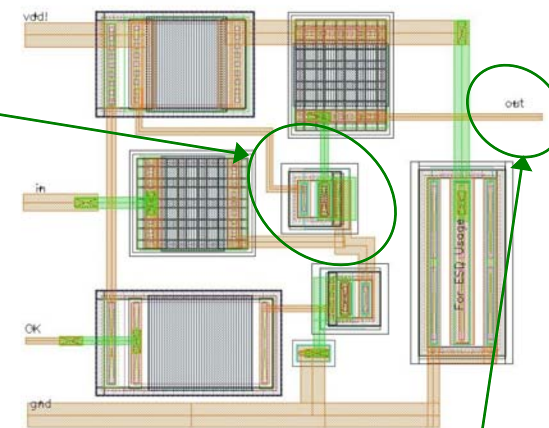
PIXRO1(2): S&H and 16:1 MUX

In development at present time: **PRELIMINARY**

SiGe 0.5µm process from IBM

NPN switches & SF for high speed

NPN SiGe SF



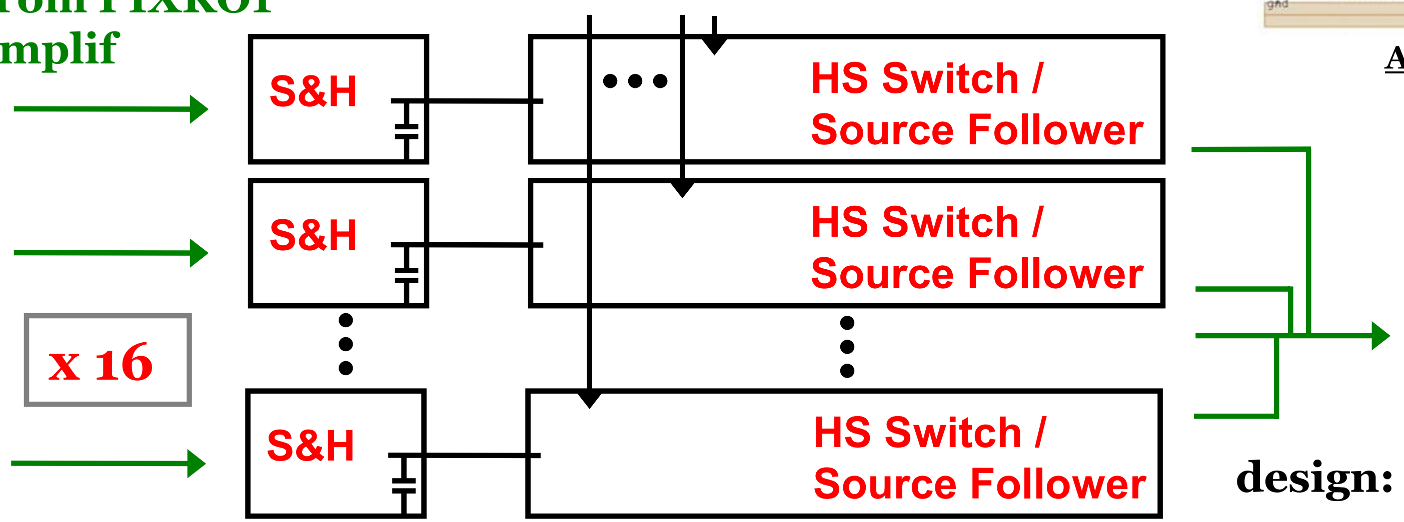
clk

A HS Switch/SF

Simul, single switch: 0.15ns settling (1V swing)

From PIXRO1 Amplif

clks: ripple chain

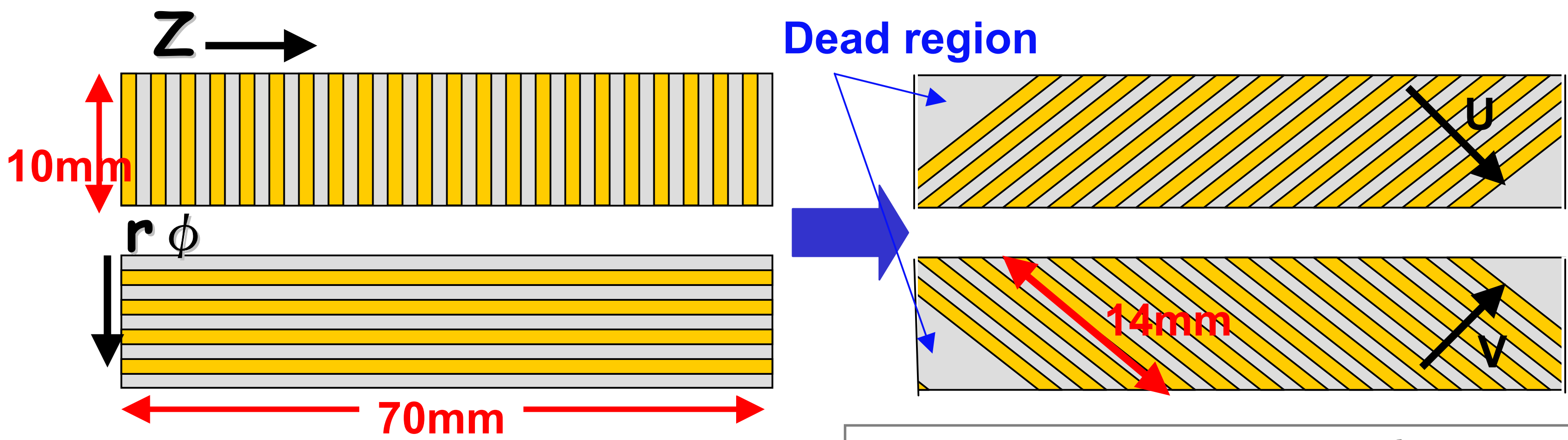


single output / 1.6GSa/s

design: Qianyi Yang (UH)

Short strip DSSD (Striplet)

- New type of DSSD: Striplets   T.Tsuboyama-san & M.Hazumi-san, KEK
  - Strip length is shortened.
  - Arrange strips in 45 degrees wire-bonding eased.
  - Small triangle dead region exists (about 7 % in layer1).
  - Occupancy is reduced to ~5% @L= $10^{35}/cm^2/s$
  - Higher luminosity case needs pixel type sensor



From T.Kawasaki-san, Niigita-U, 6th HL WS, 2004/11