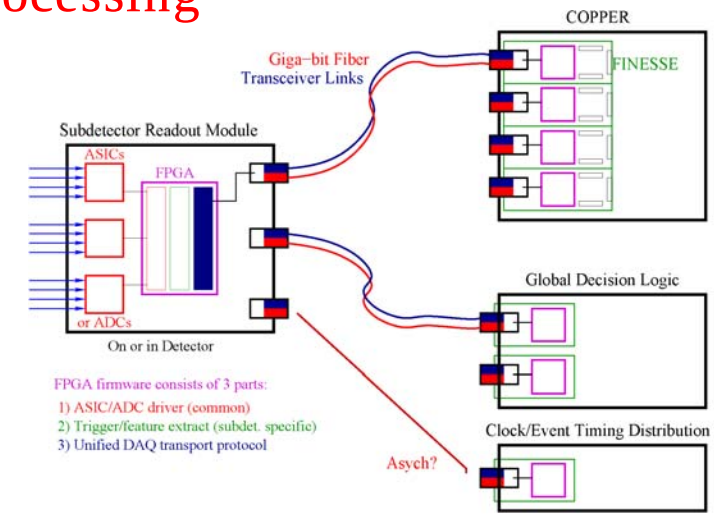
X-ray FEL Detector mechanics

- Overview
- Planned 1st run configuration
  - Flux estimates
  - Detector configuration
  - Data rates
- Future development efforts
  - Detectors
  - Electronics/processing



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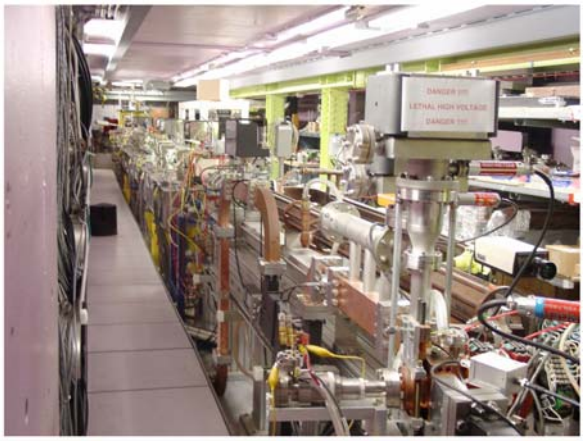
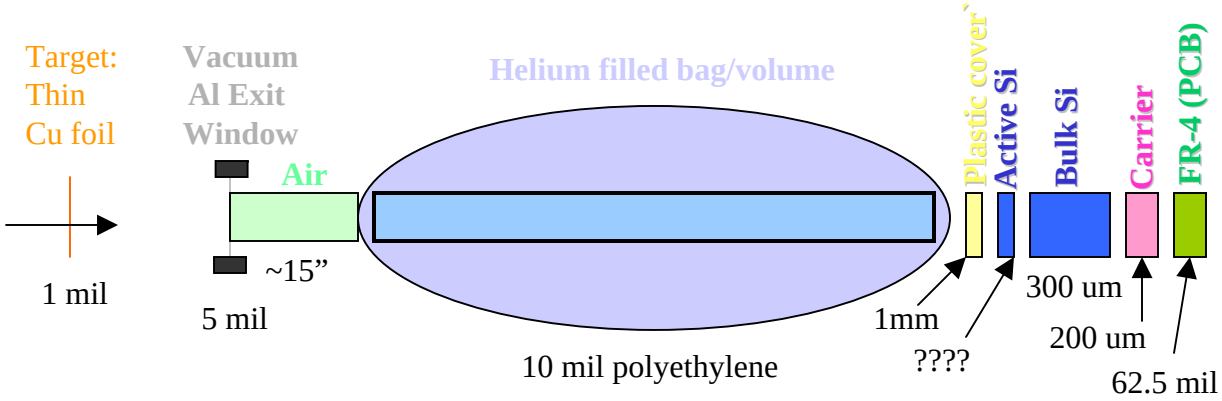
Gary Varner

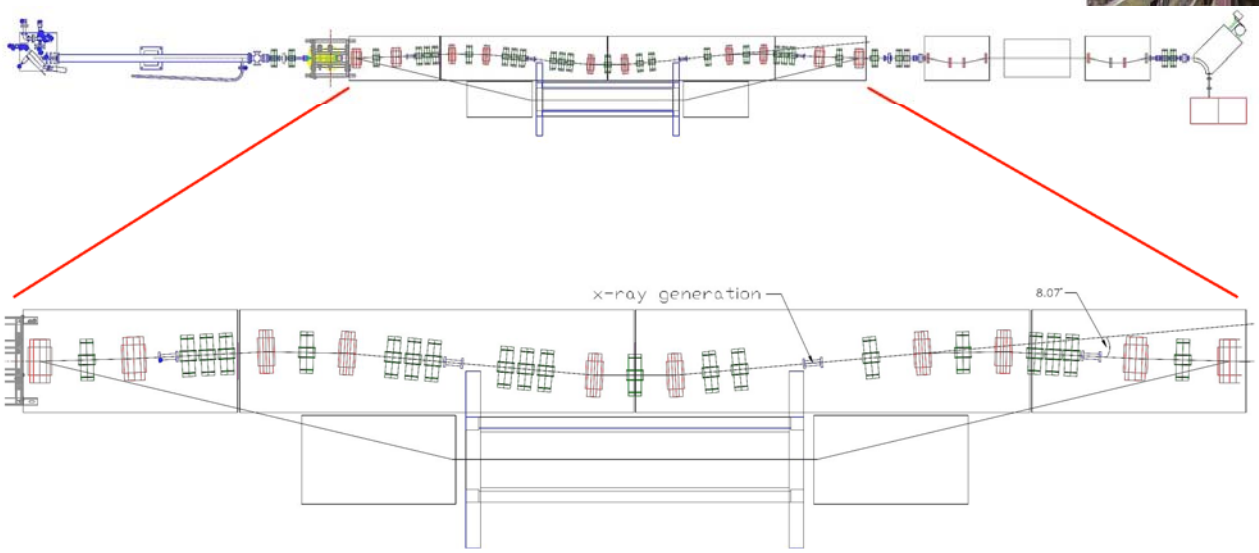
5-FEB-2010

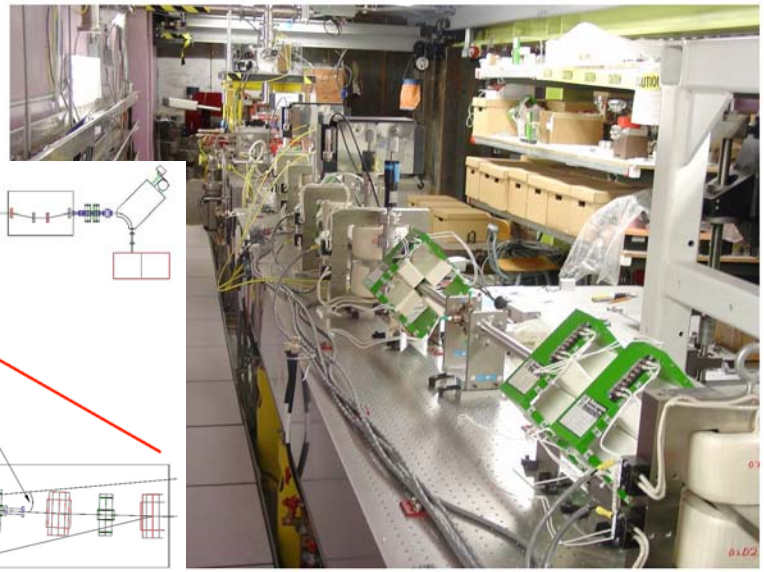
Bremsstrahlung Beamline Estimates

Dec.-2009





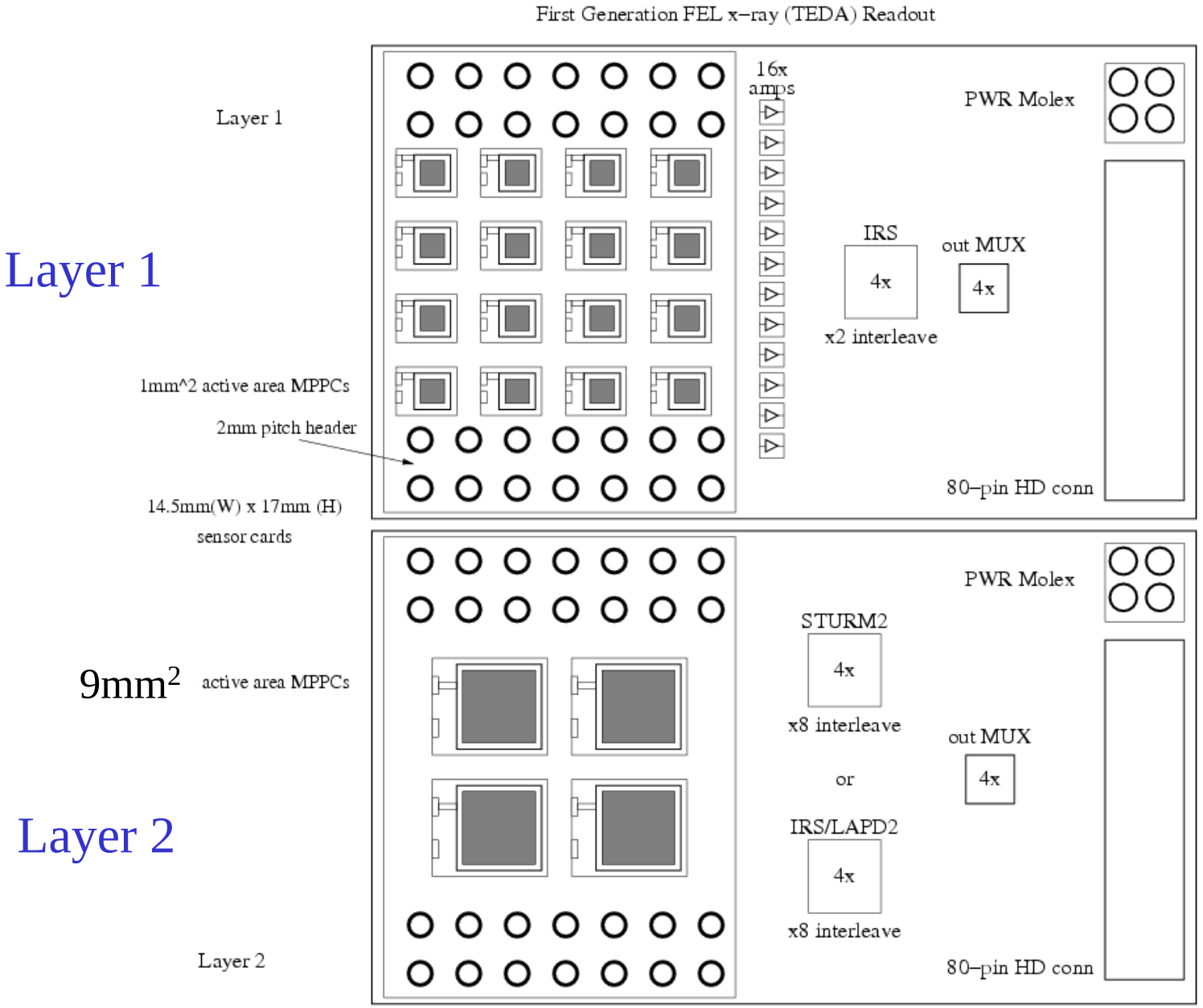




Brem beamline Summary

- Initial run with 2 detector planes
  - 1mm2 array for “bare” layer
  - 3mm2 array with BaF2 radiator
- More than adequate flux (2nd layer)
- Developed x-ray transport simulation
  - Input to a signal Monte Carlo
  - Fix readout/ASIC design specifications

First Detector Arrays



Layer 1

Layer 2

Readout for FEL x-ray beamline

cPCI crate (control room)

ASICs

Detectors

X-rays

Front-end Module

Master Module

New card

CPU

Giga-bit Fiber links

Master module

First Prototype throughput

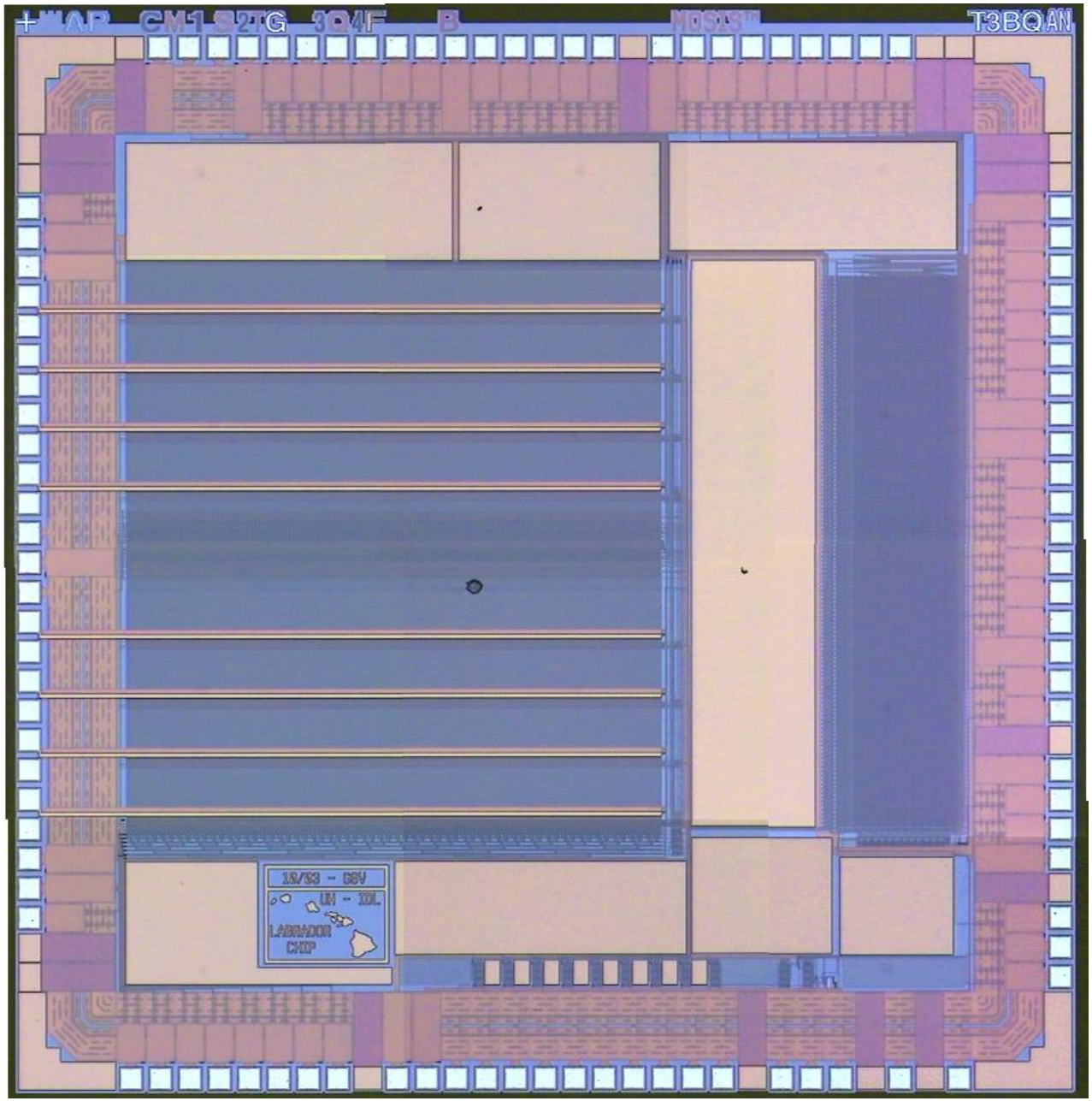
- For configuration shown earlier
  - 1 layer = 4 ASICs (8Ch.)
  - 1 “shot” = 4 chip * 8Ch * 32k = 1Msmp/layer
  - (1 shot = 8us recording @ 4GSa/s)
- 16Mbit/s/shot
- 320Mbit/s @ 20Hz operation
  - 2x Layers/fiber ~ 0.64 Gb/s (20% capacity)
  - May do 1 fiber/layer for convenience (fibers are inexpensive)
- 40MBytes/s raw data (need to feature extract)

Readout System Summary

Great Progress

- Now have a clear plan for late Feb. first run (on schedule)
- ASIC development path is multi-prong, design effort will intensify this semester
- Data transfer architecture has plenty of margin and is scaleable upward
- Detector development – prototype from CERN in February; further device fabrication runs

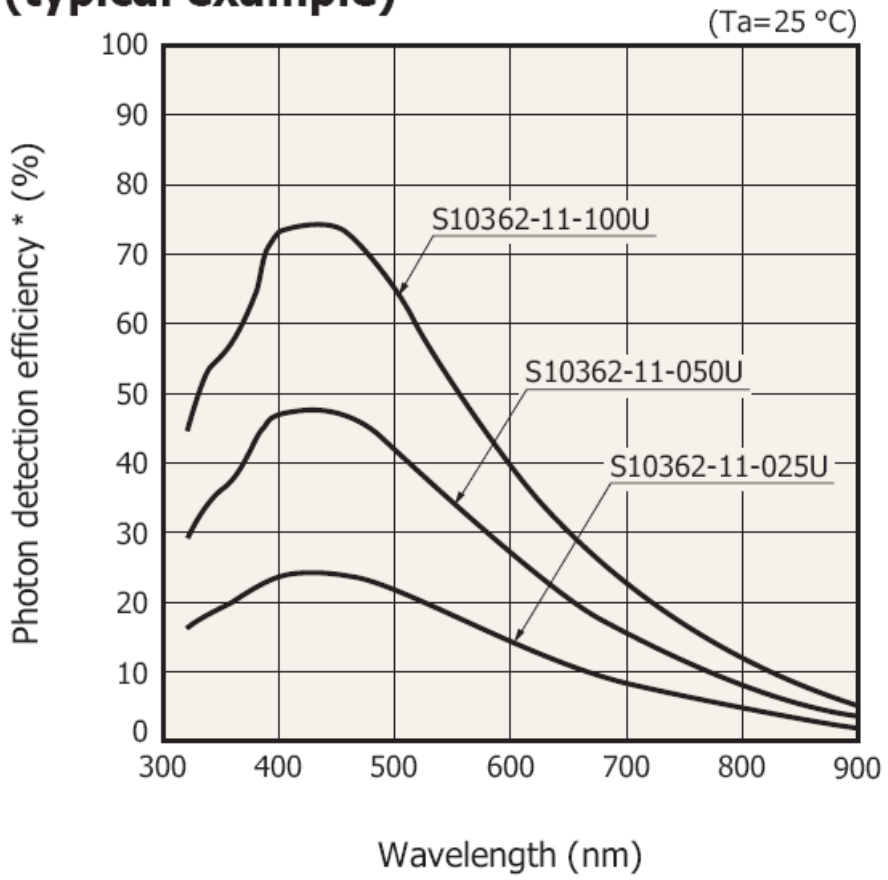
Back-up slides



1, 3 mm^2

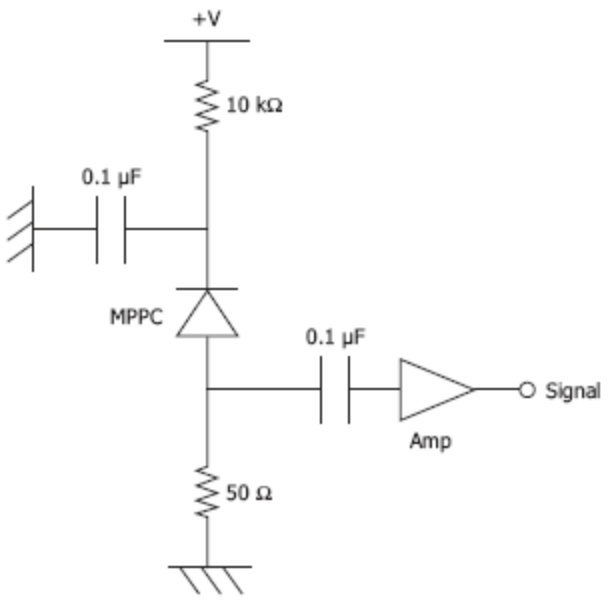
Hamamatsu MPPC

Photon detection efficiecy (PDE) vs. wavelength (typical example)



* Photon detection efficiency includes effects of crosstalk and afterpulses.

Connection example



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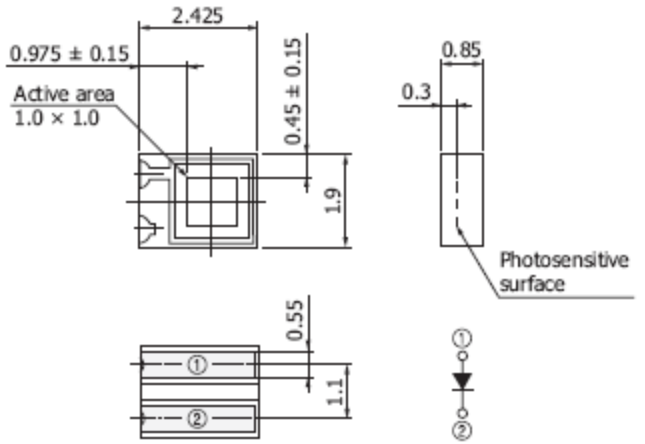
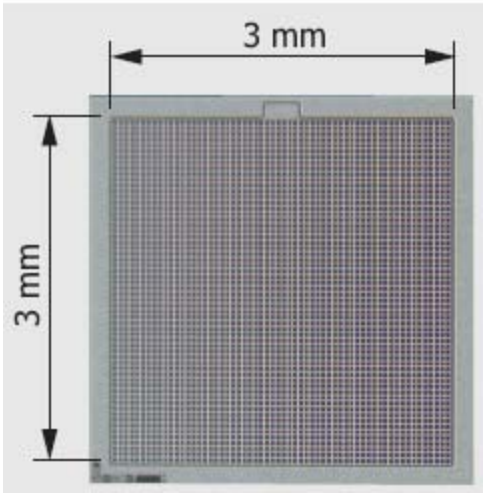
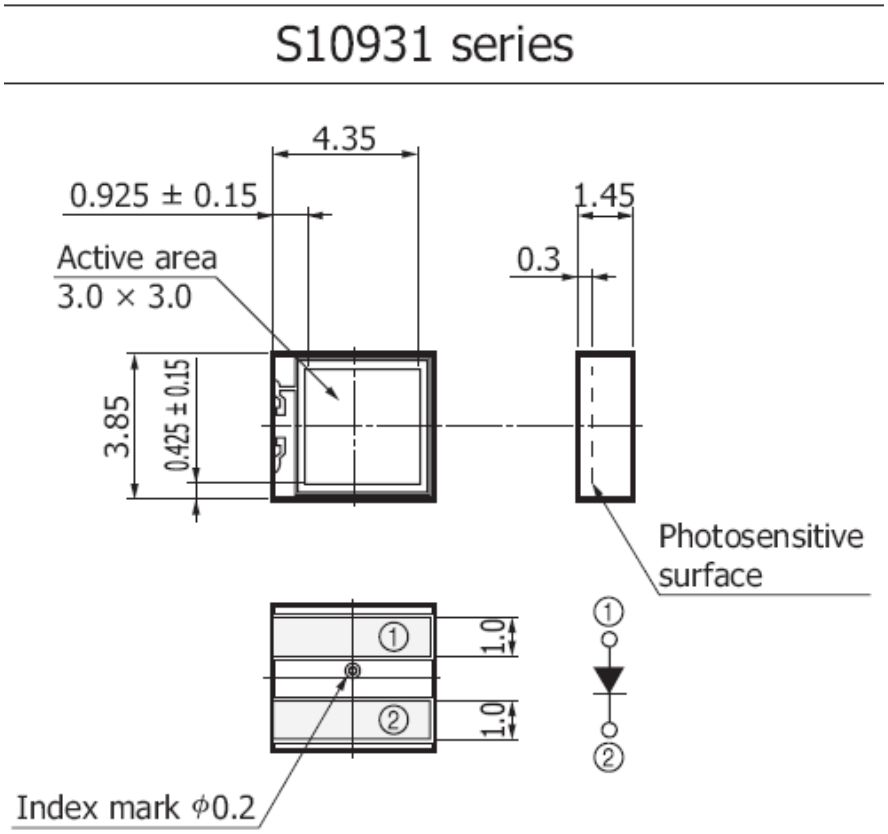


Ordered 10x 1, 3 mm^2

3 mm^2 Hamamatsu MPPC coverage

14,400 pixels for the 25μm pixel case





Better fill-factor for tiling → ~53% active

G = 2.7×10^5

TTS ~ 250ps RMS (single p.e.)

Proto ASIC psTDC1

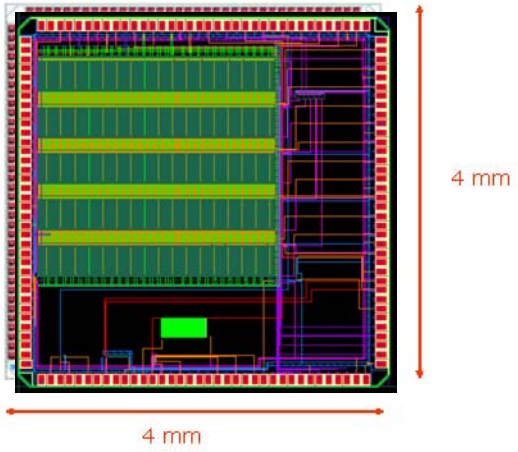
“oscilloscope on a chip”

Specifications

- 10-15 GSa/s
- >= 2GHz analog bandwidth
- 256 sample cells
- 4 channels
- separate timing channel
- on-chip conversion
- IBM 130nm CMOS process
- 25.6μs readout
- 40mW/channel
- Direct interface (stud-bond) to microstrip board

ASIC in evaluation

Chip Layout



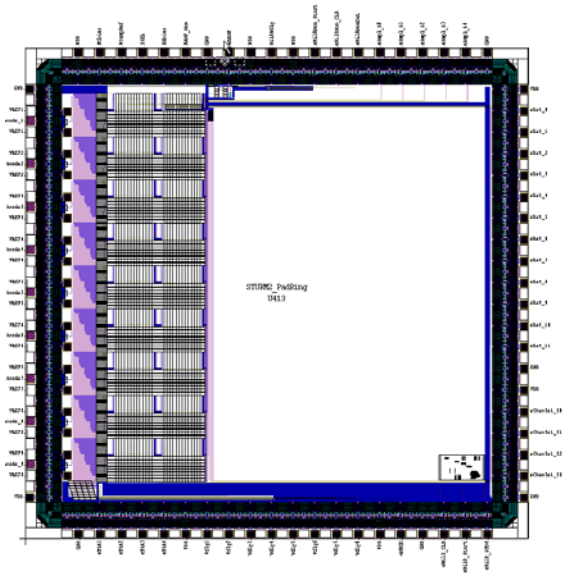
STURM2 Prototype (evol. Step)

"Max bandwidth/throughput"

Specifications

8	channels/STURM sampling
1	monitor channel
4	TSA sample buffers
8	samples/TSA buffer (32x channel)
288	Wilkinson conversion cells
1-200	GSa/s effective (5ps - 1ns Tstep)
1	word (RAM) sample readout
1+n*0.02	us to read n samples
100	kHz sustained readout (orbit)

Chip Layout

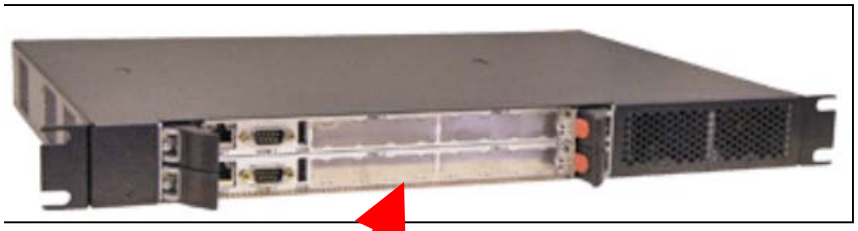


ASIC in fabrication

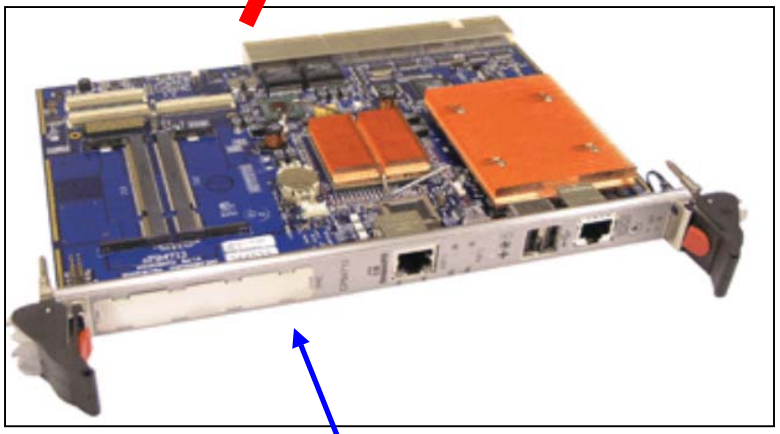
~20GHz (onto ASIC)

2.5GHz (into storage cell)

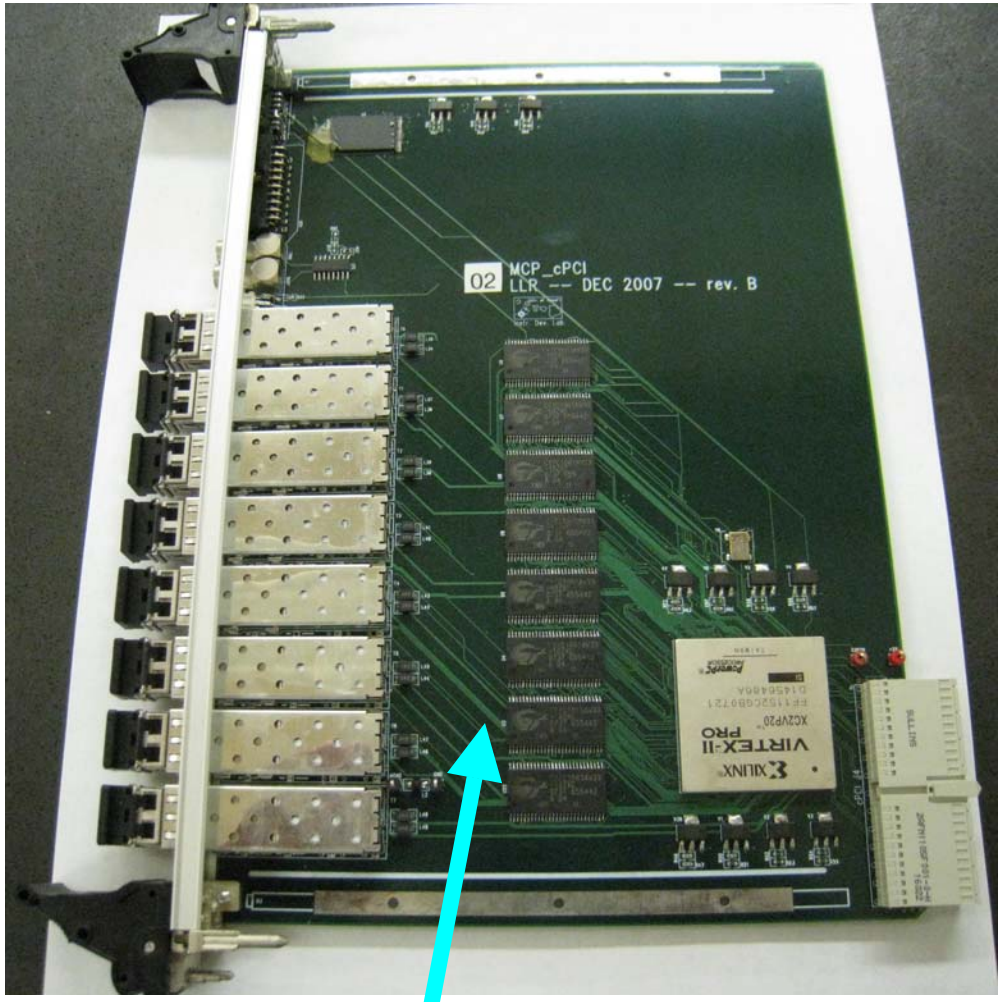
compact PCI Platform



cPCI crate



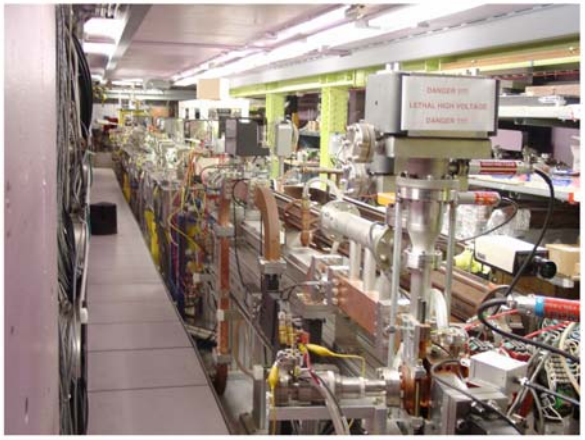
cPCI CPU

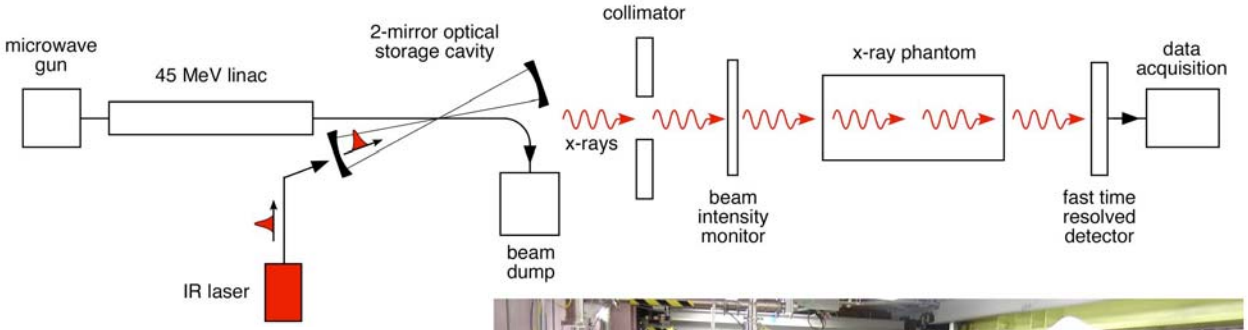


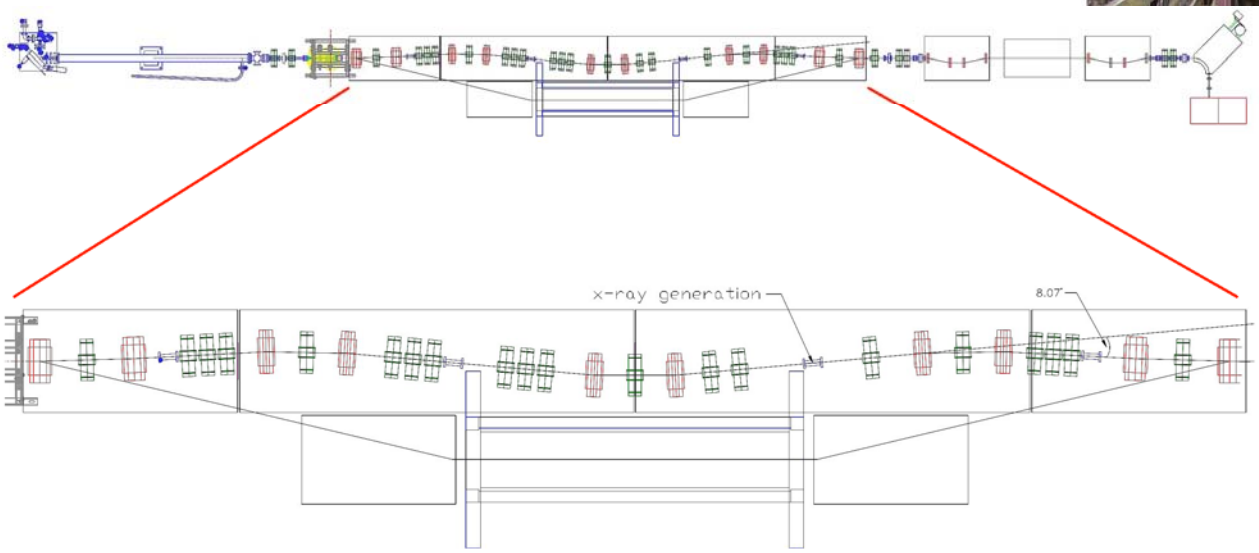
Data processing card

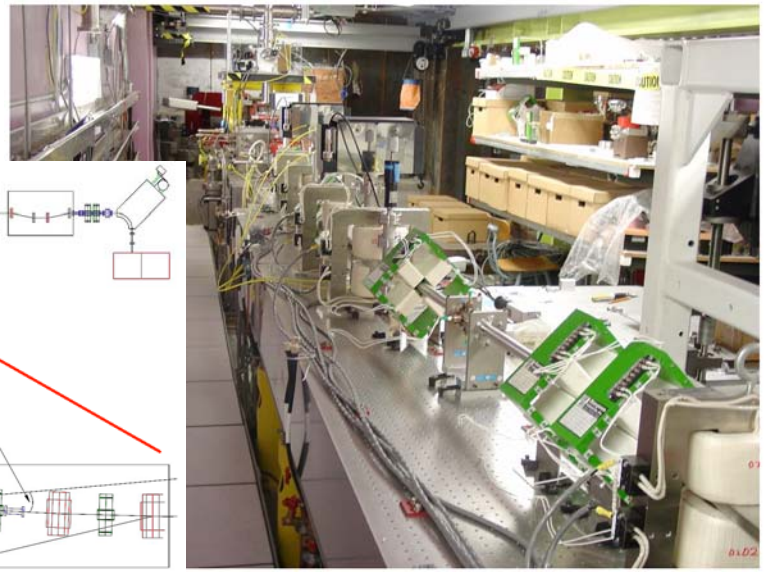
(example – DSP version)

Mono-chromatic x-ray Source









Future Detector Options