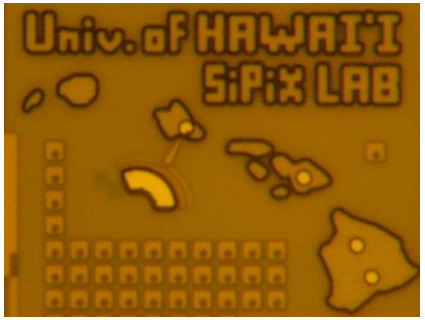
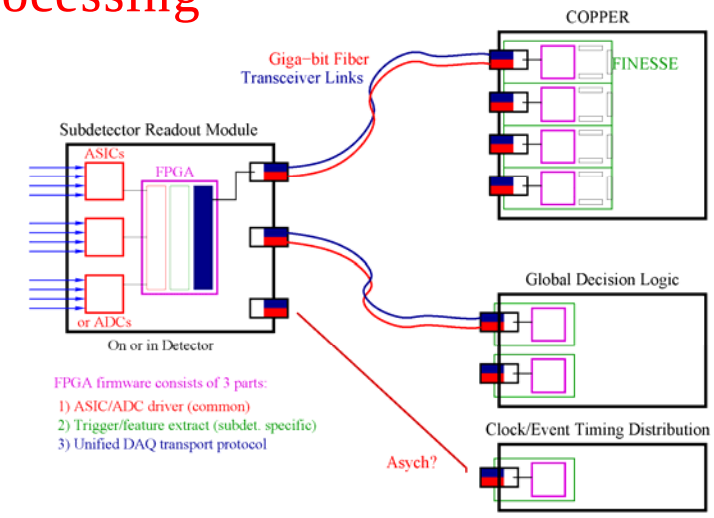
X-ray FEL DAQ Design Reviews



- Tasks update
- Brem beamline sims
  - Flux estimates
  - Detector configuration
  - Data rates
- Proposed 1st run configuration
  - Detectors
  - Electronics/processing

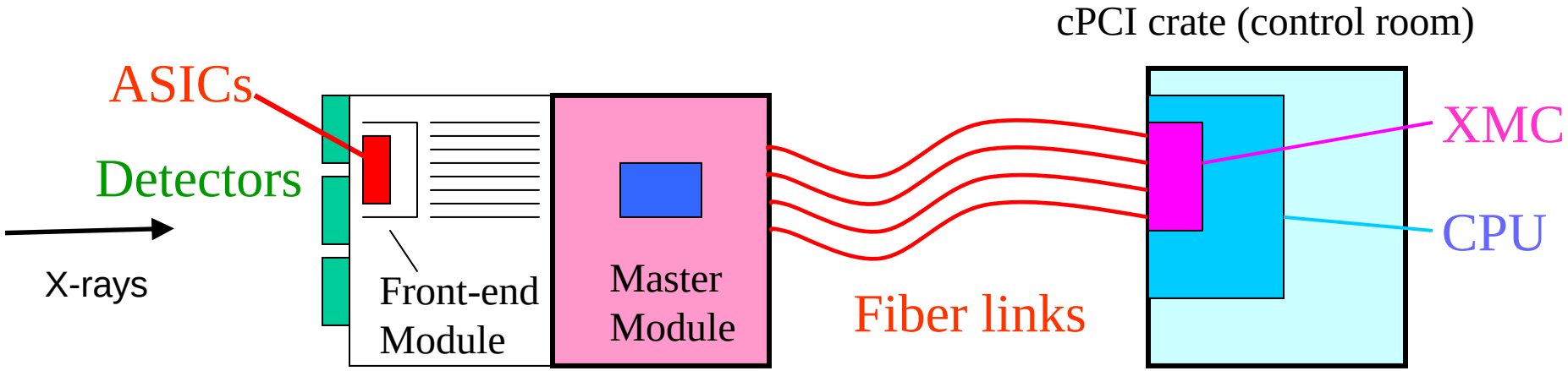


Juaquin Anderson
Matt Andrew
Michael Cooney
Xin Gao
James Kennedy
Luca Macchiarulo
Marc Rosen
Larry Ruckman
Gary Varner

8-JAN-10 Revision

Initial concept for FEL x-ray beamline readout

- Up to 160 Channels
  - 16 detectors or detector channels/layer
  - 10 layers
- Modular system (expandable)
- 100 GSa/s during 10μs spill (10Hz rep rate)
  - 10μs/10ps = 10^6 samples/channel
  - Fiber: 12 Gb/s (4x 3.0Gb/s)



Year 1 Development Schedule for Integrated x-ray Readout/DAQ

Items Today

7-jan-10//GSV

	Task	Subtask	Jan 1	2	3	4	Feb 1	2	3	4	March 1	2	3	4	April 1	2	3	4	May 1	2	3	4	June 1	2	3	4	July 1	2	3	4	Aug 1	2	3	4	Sept 1	2	3	4
1	350ps bunch separation demonstrator	optical comp acquisition																																				
		bench commission																																				
		acquire photodetectors																																				
		CDR																																				
		simple DAQ USB (exist)																																				
		PD/RO interface board																																				
		Specs verification/TDR																																				
		commission																																				
		Measurements																																				
2	Fast DAQ system	XMC readout design																																				
		cPCI crate/CPU acq.																																				
		CDR																																				
		Fast link fabrication																																				
		firmware development																																				
		software development																																				
		Readiness Review																																				
		integration/test																																				
3	ps2 ASIC	Specs confirm																																				
		Preliminary design																																				
		CDR																																				
		Detailed simulations																																				
		Layout																																				
		Design Review																																				
		MOSIS fabrication																																				
		Eval board fab + test																																				
		Integrated module design																																				
		Integrated module fab																																				
		Integration + operation																																				
		first beam																																				
4	Custom Sensor 1	Specs confirm																																				
		design + simulation																																				
		prototype eval																																				
		CDR																																				
		detailed simulations																																				
		Design Review																																				
		fabrication																																				

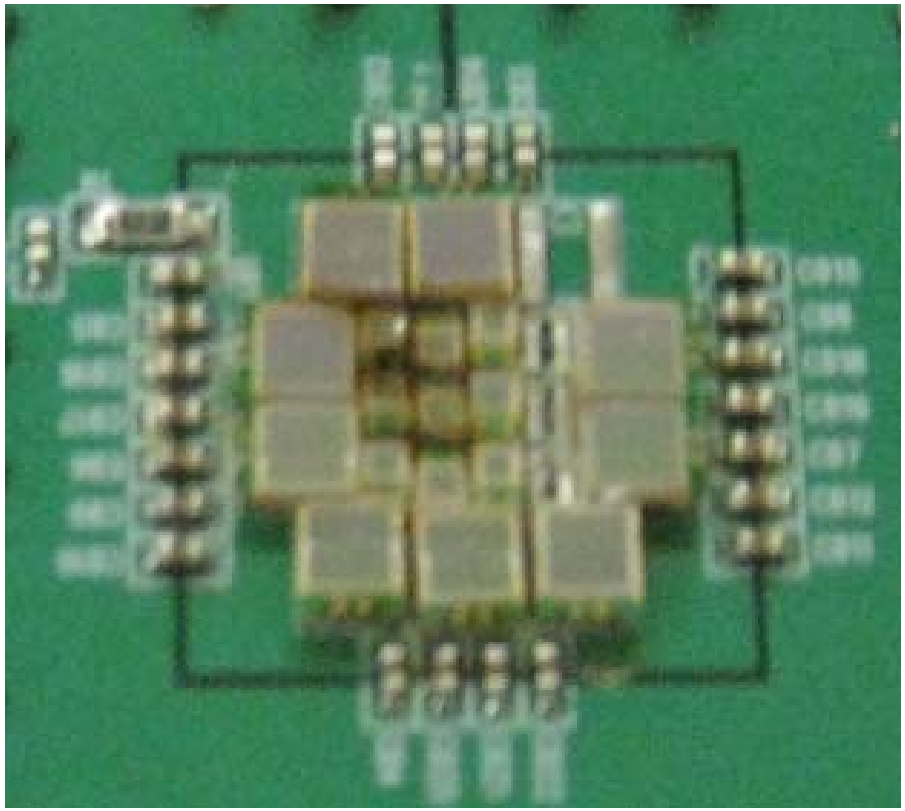
Today

First COTS detector array

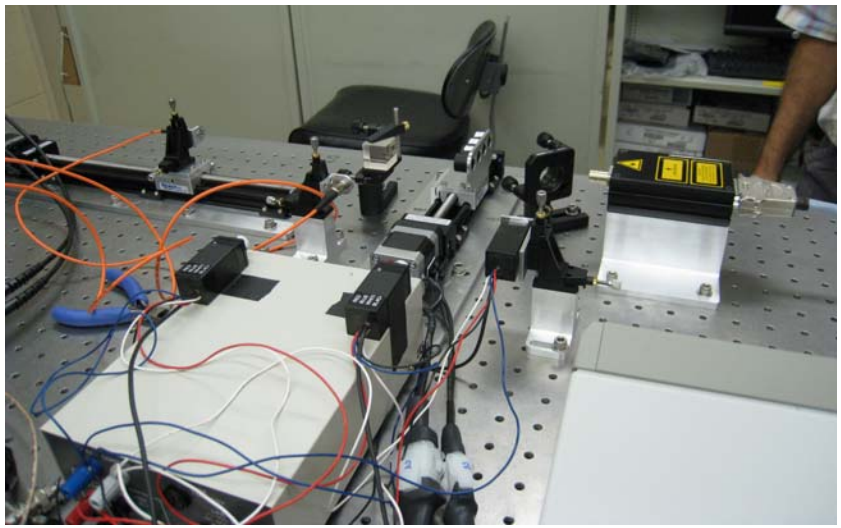
Specifications

- Outer ring 3x3mm active
- Inner 3x3 array of 1 mm-sq active MPPC
- "Geiger-mode" Avalanche Photo-diodes with ~10^6 gain
- Instrument with available electronics prototypes

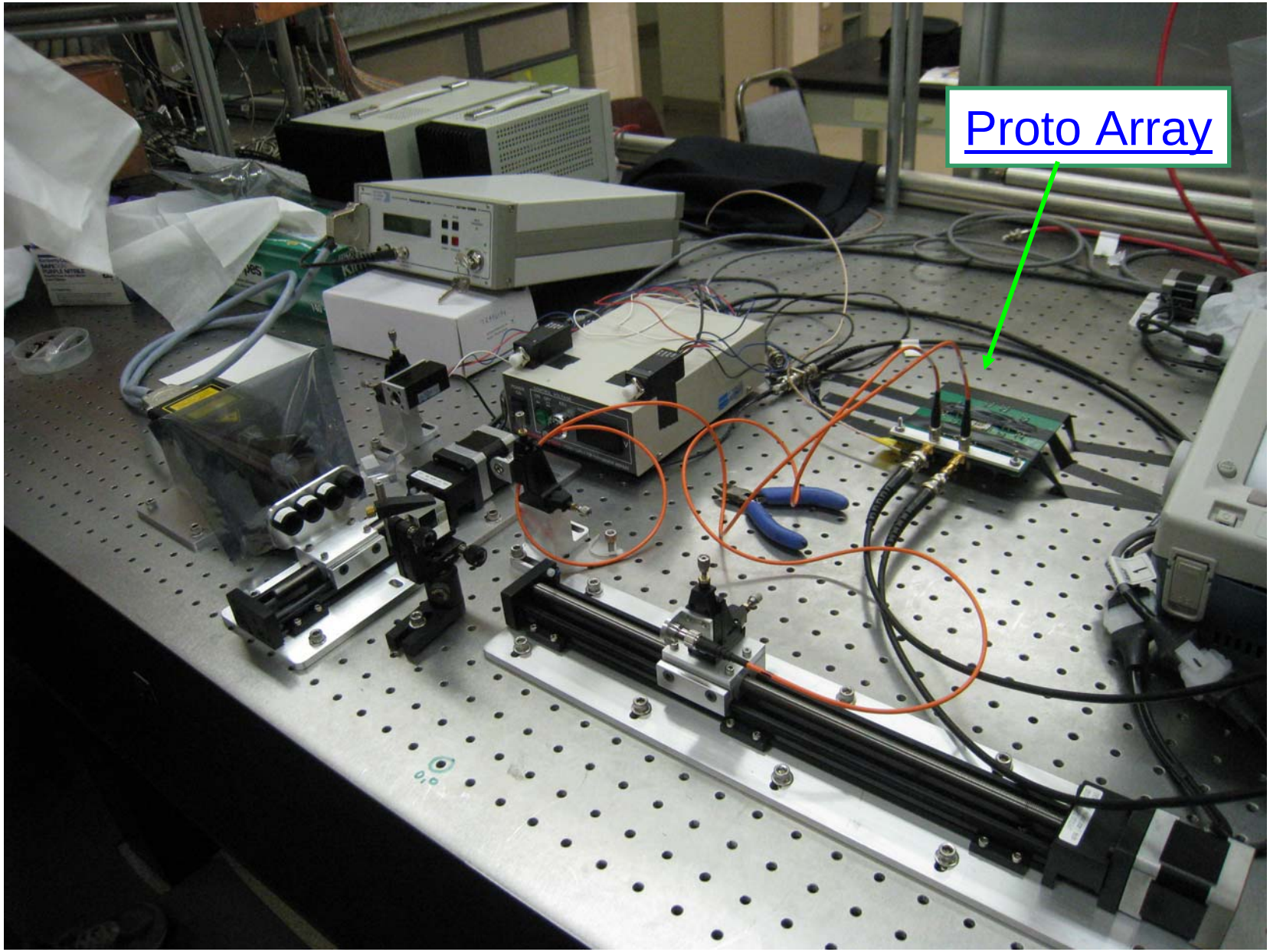
Proto Array Layout



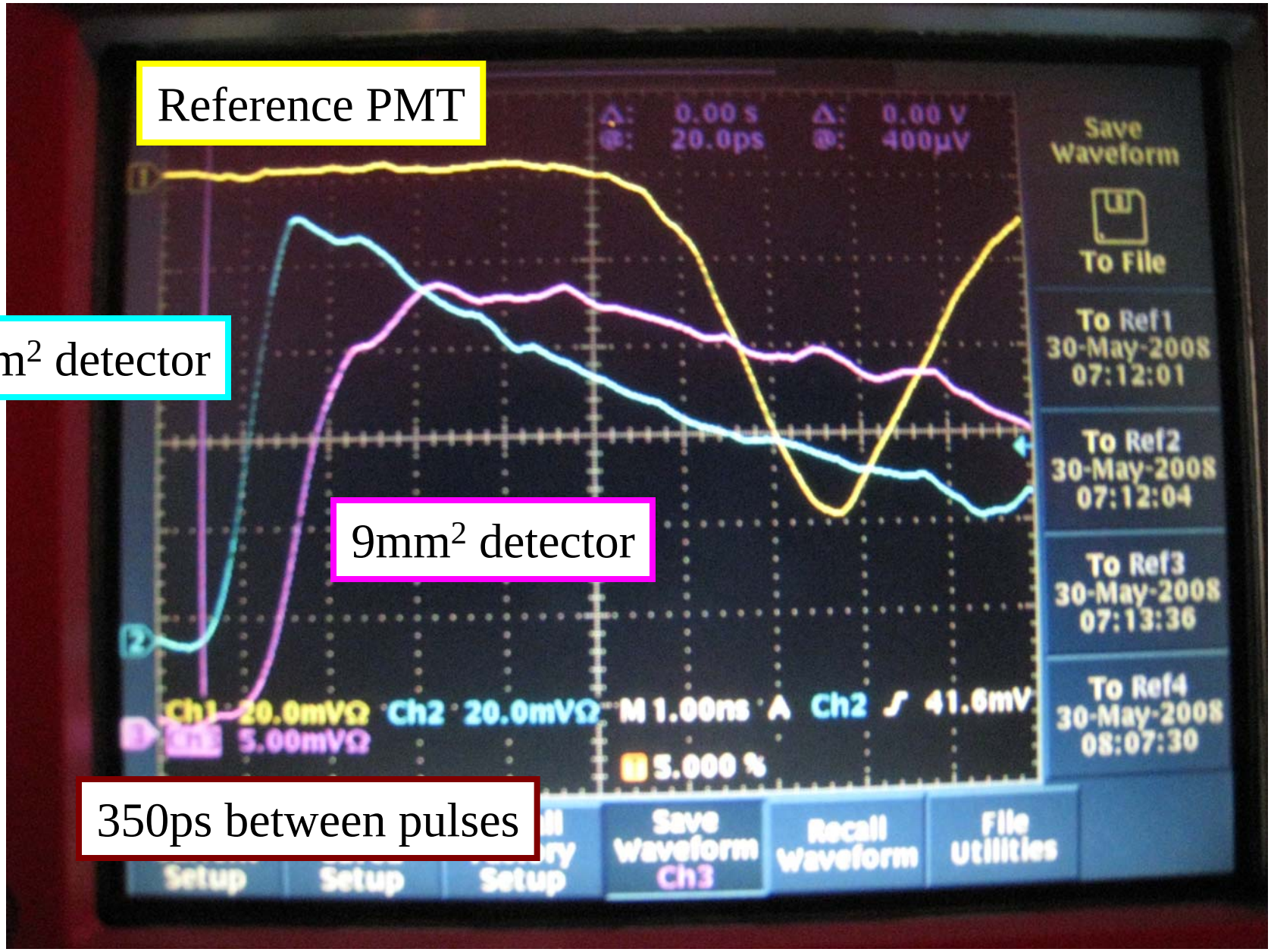
Simulated Bremsstrahlung Flux



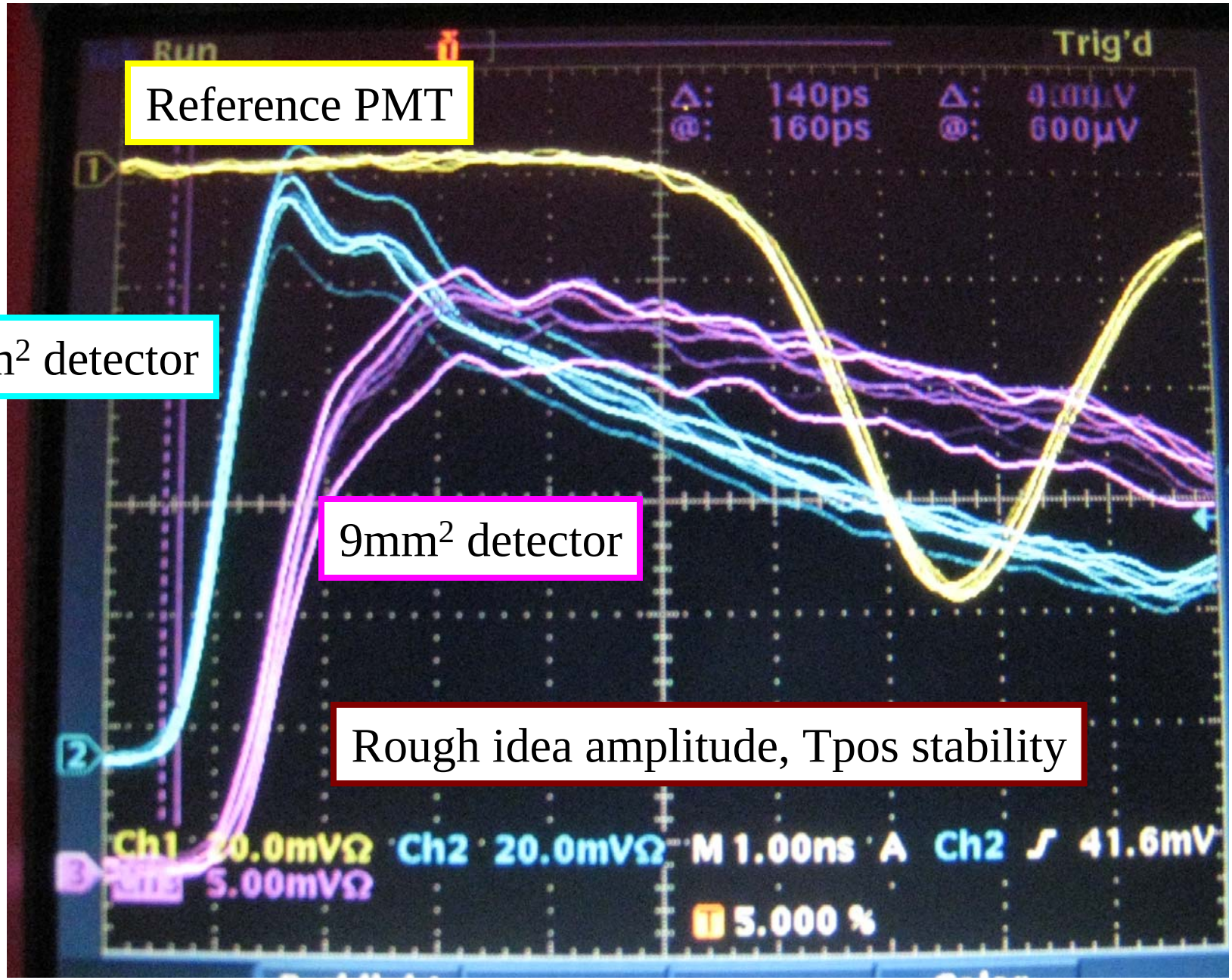
piLas test bench



First measurements (I)



First measurements (II)

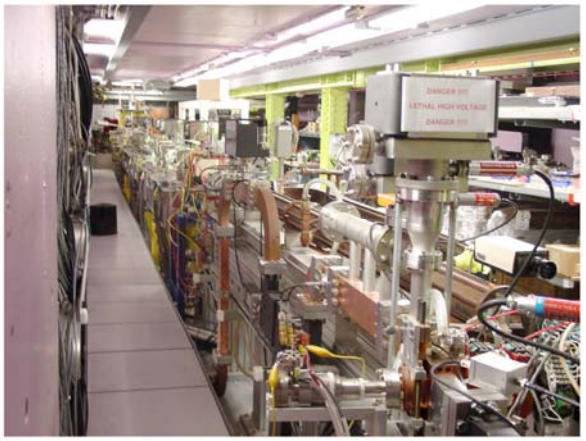


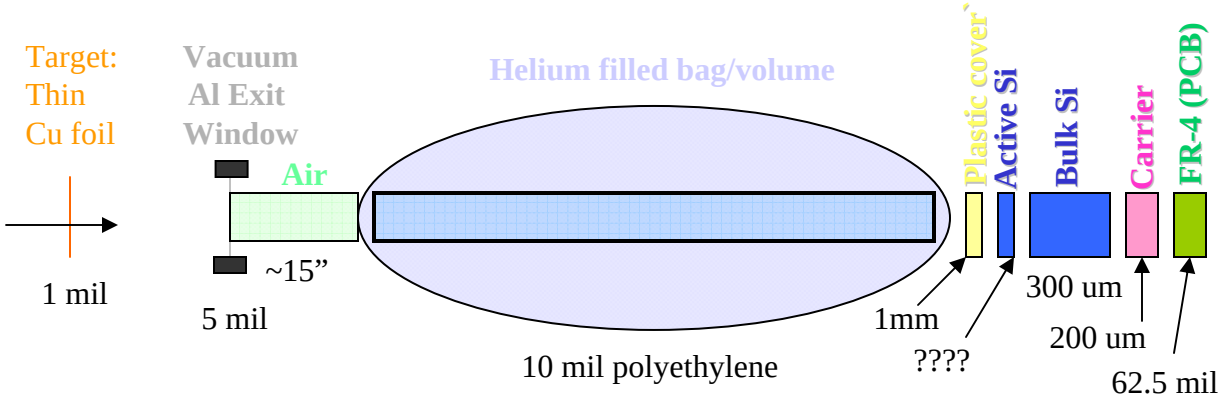
Task 1 Summary

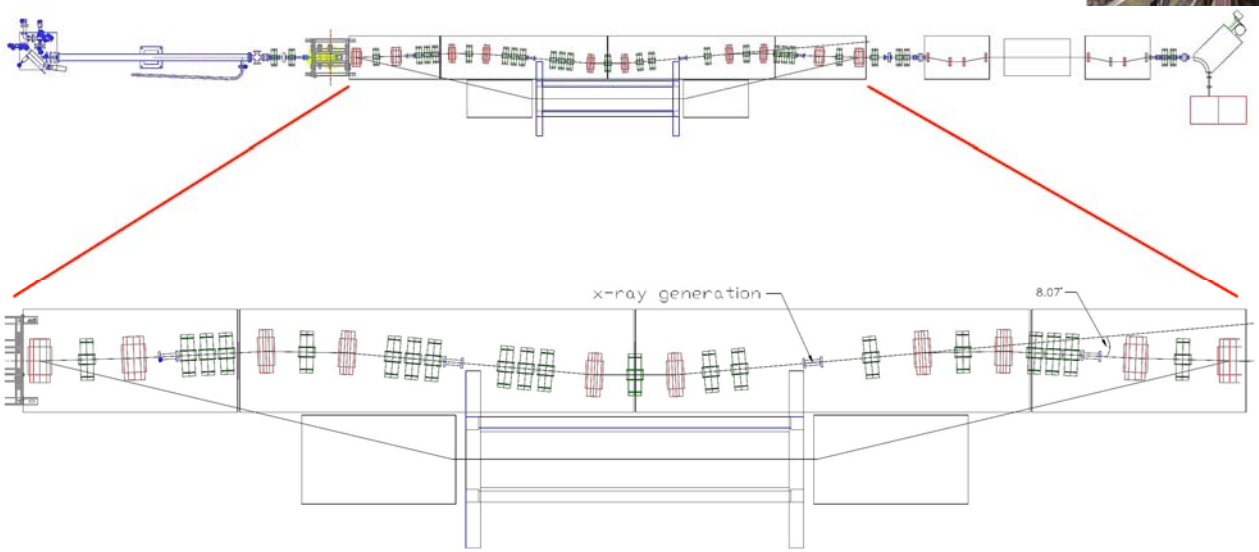
- Prototype PD (MPPCs)
  - Good risetime, stability
  - Well suited for initial testing
- Optical combining to demonstrate bunch separation for same MPPC
- Possibility to emulate short “train”?
  - 99% ND attenuation for test
  - Repeat with ASICs(?)

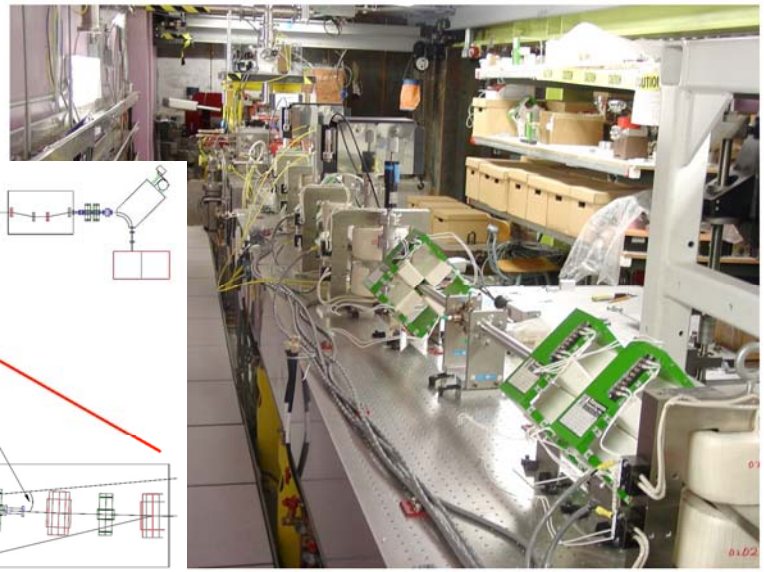
Bremsstrahlung Beamline Estimates

Dec.-2009





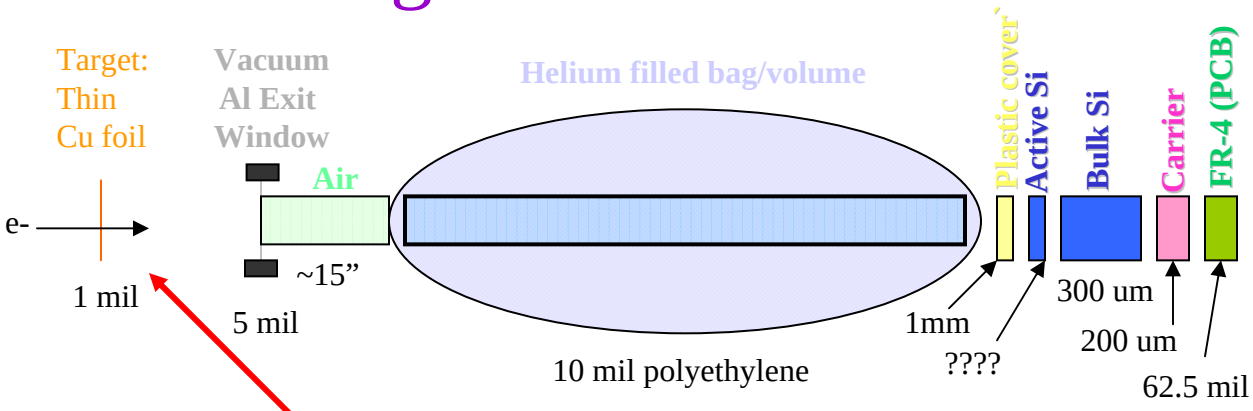




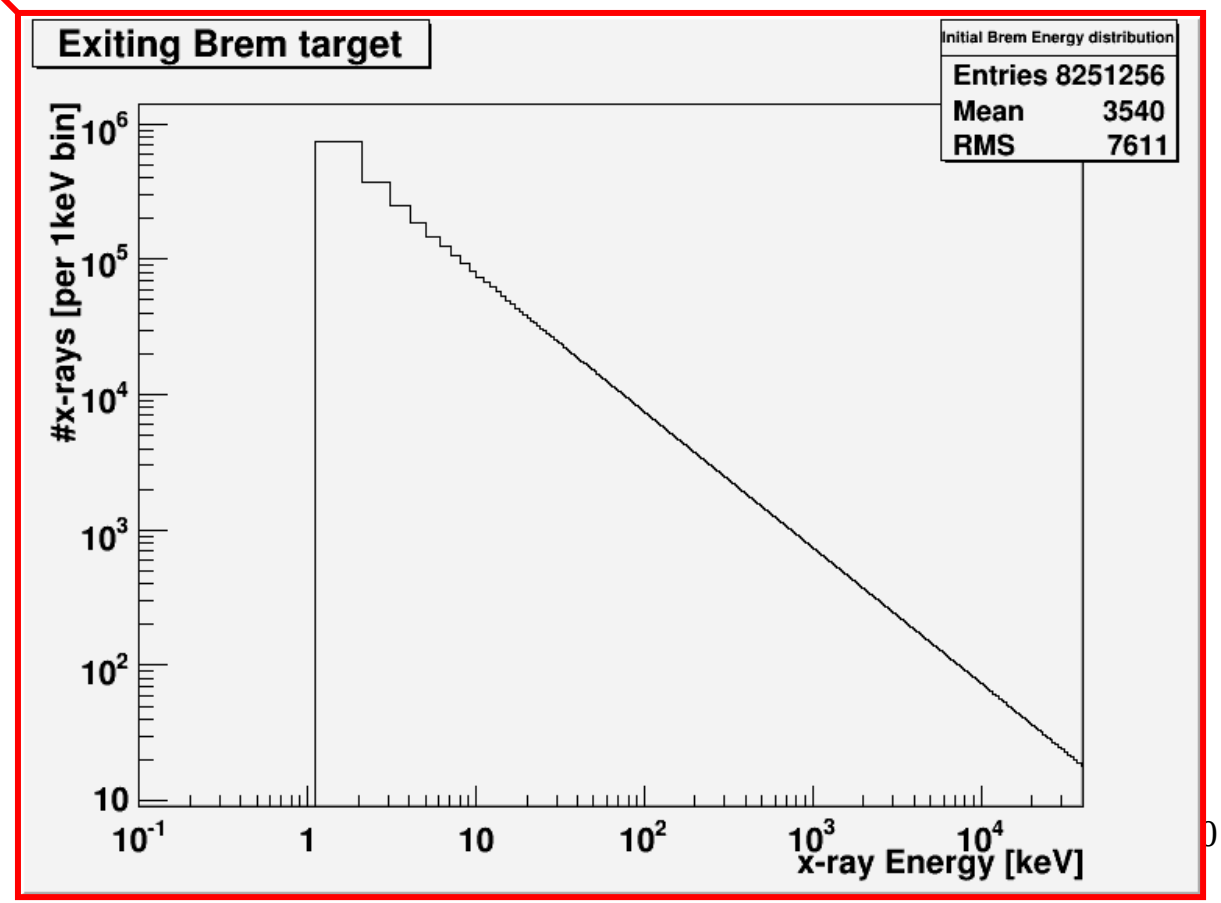
Target Production

Ebeam = 40MeV
200mA

(10-11keV bin)
8.1×10^8 γ/macropulse
~71k γ/bunch



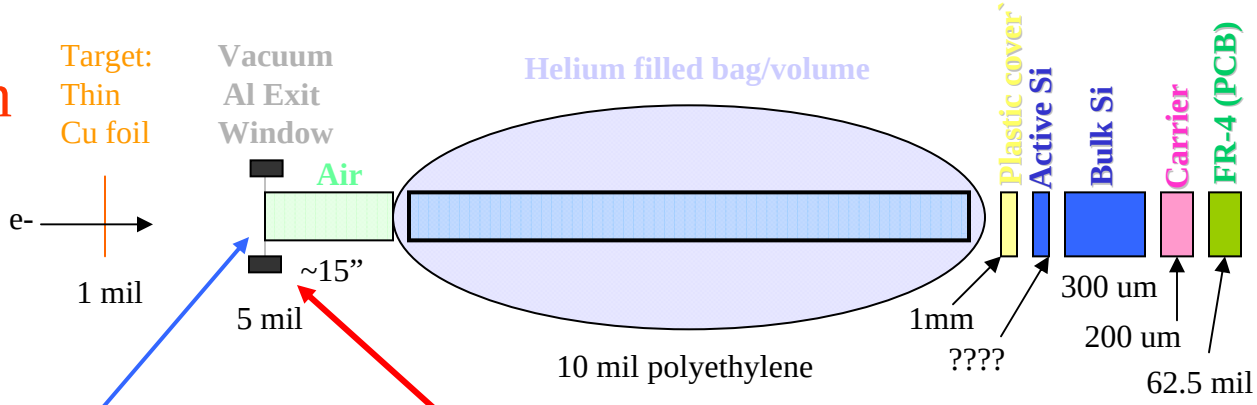
Single bunch

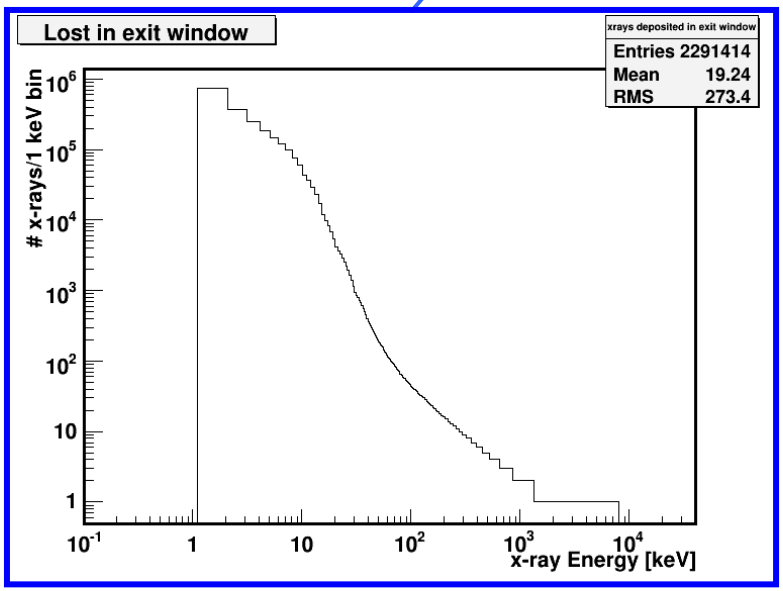


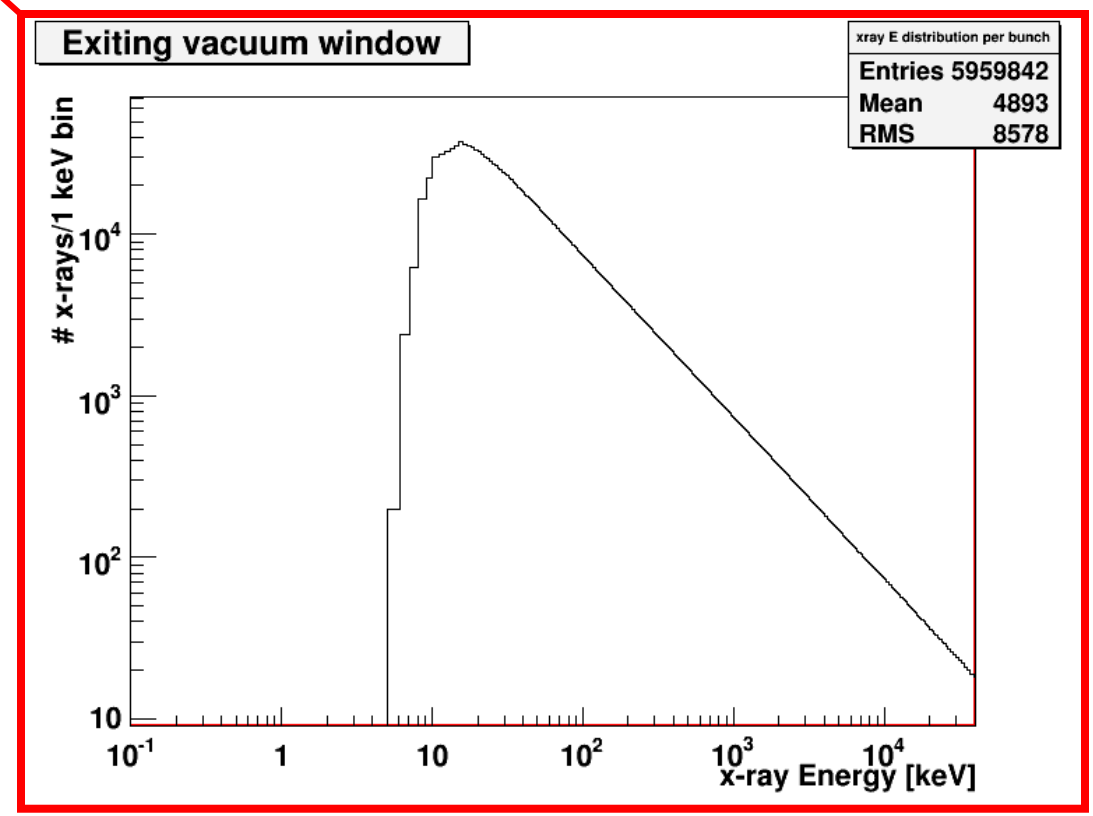
Exit window

Single bunch

Ebeam = 40MeV
200mA

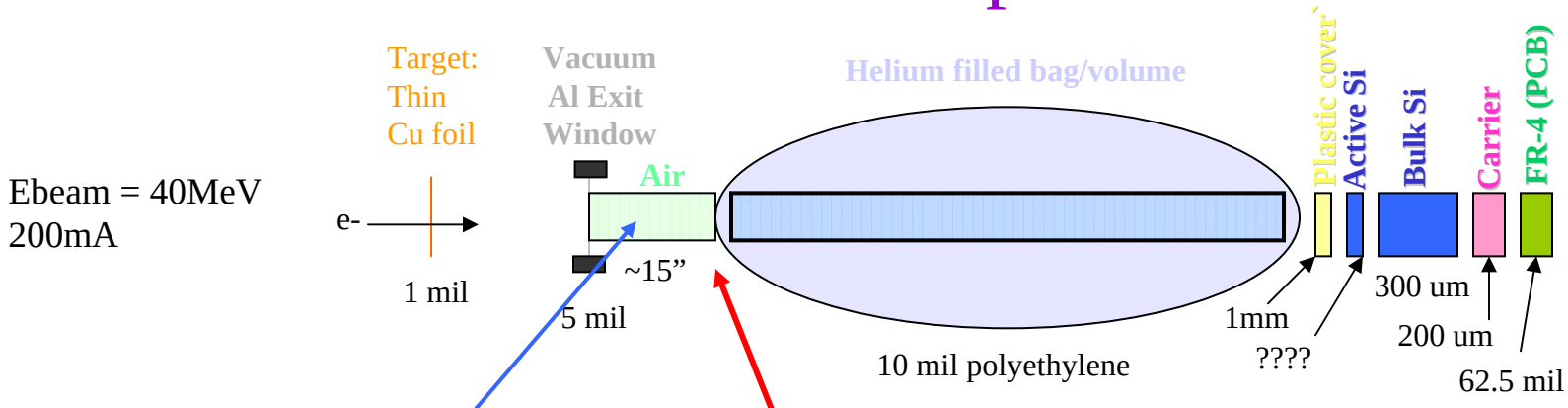


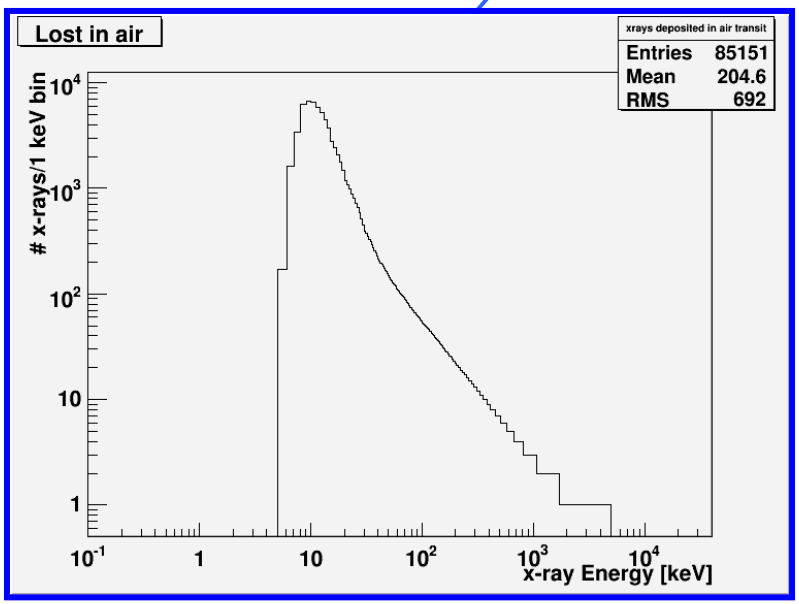


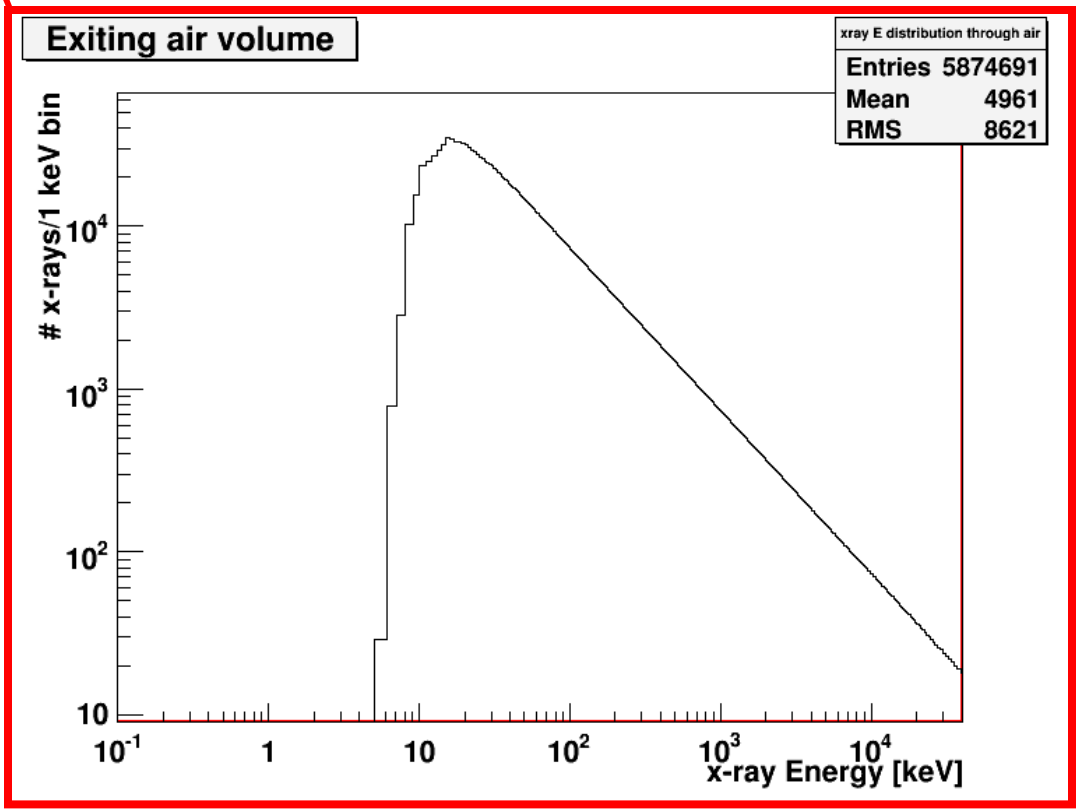


Single bunch (heat loading?)

Air transport

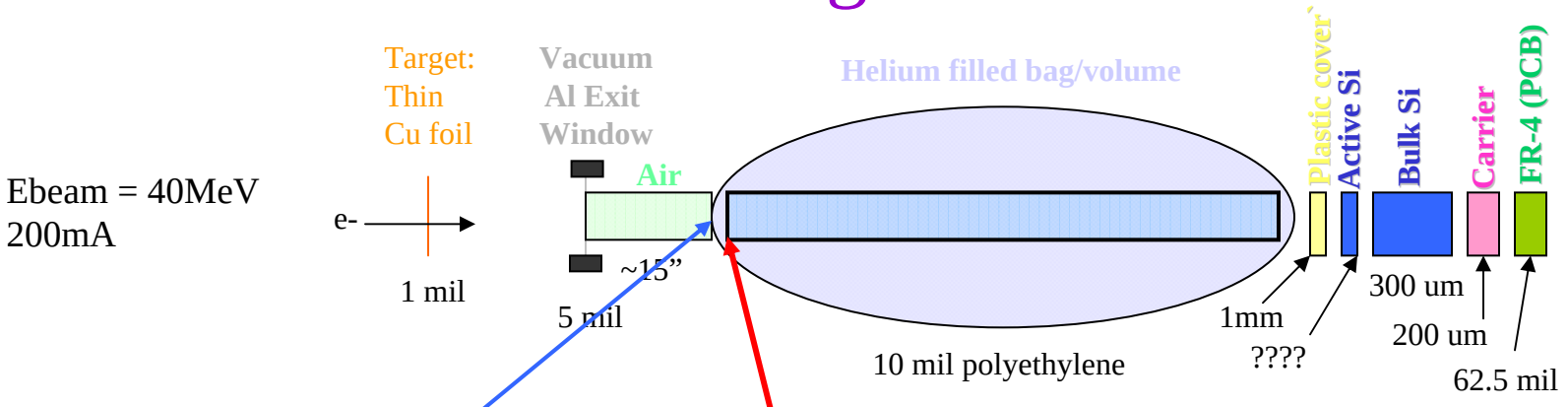


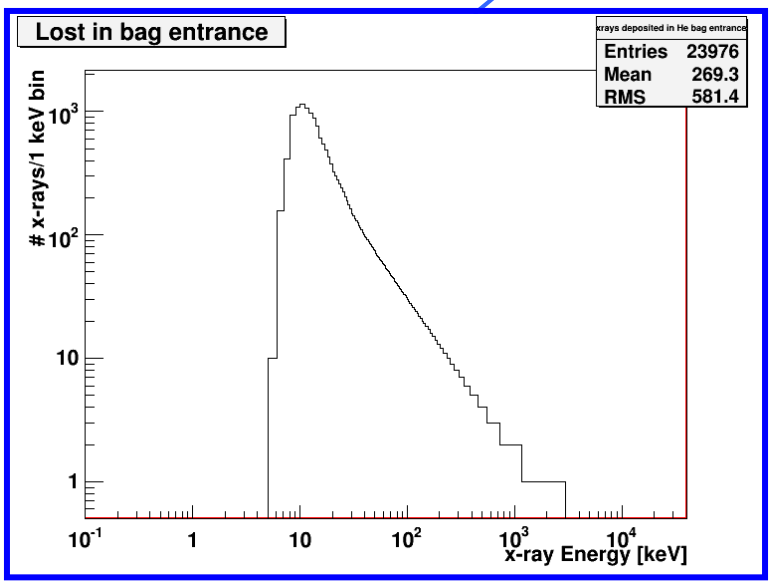


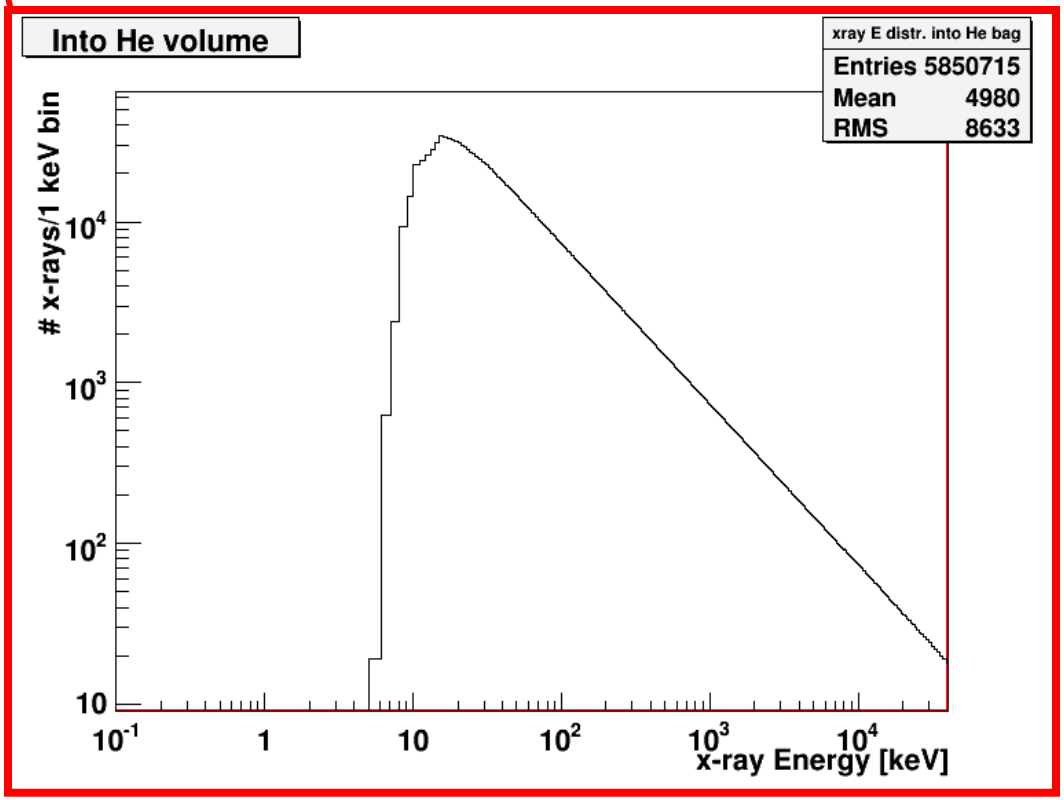


Single bunch

He bag entrance

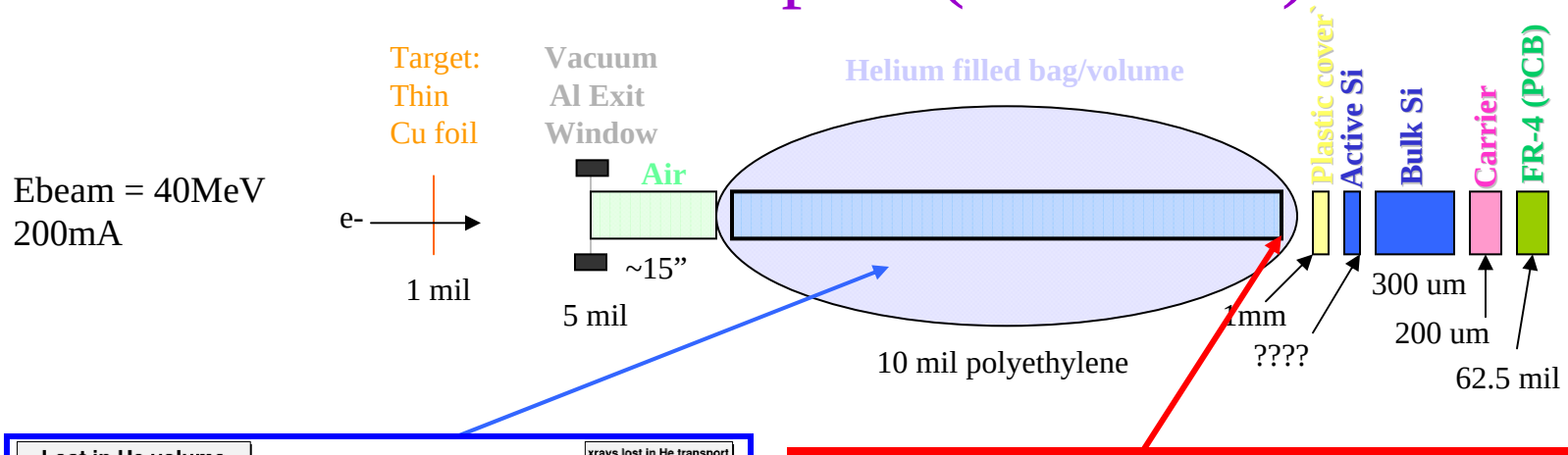


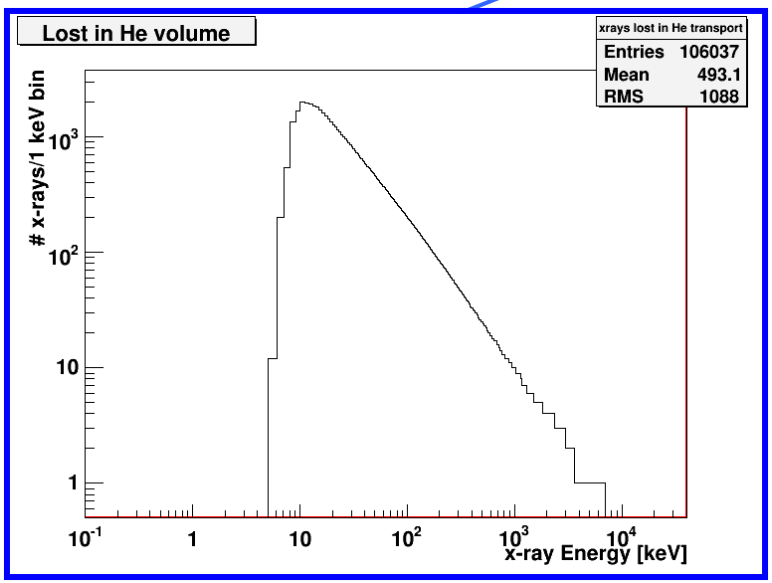


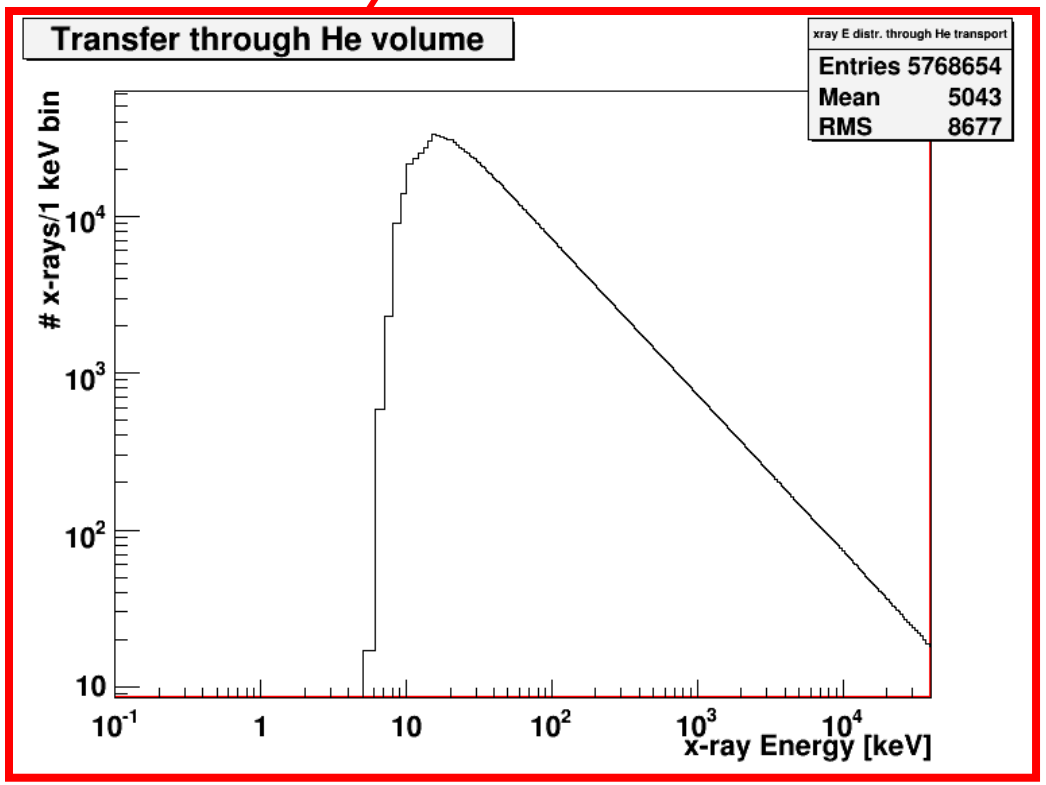


Single bunch

He transport (9.5m line)

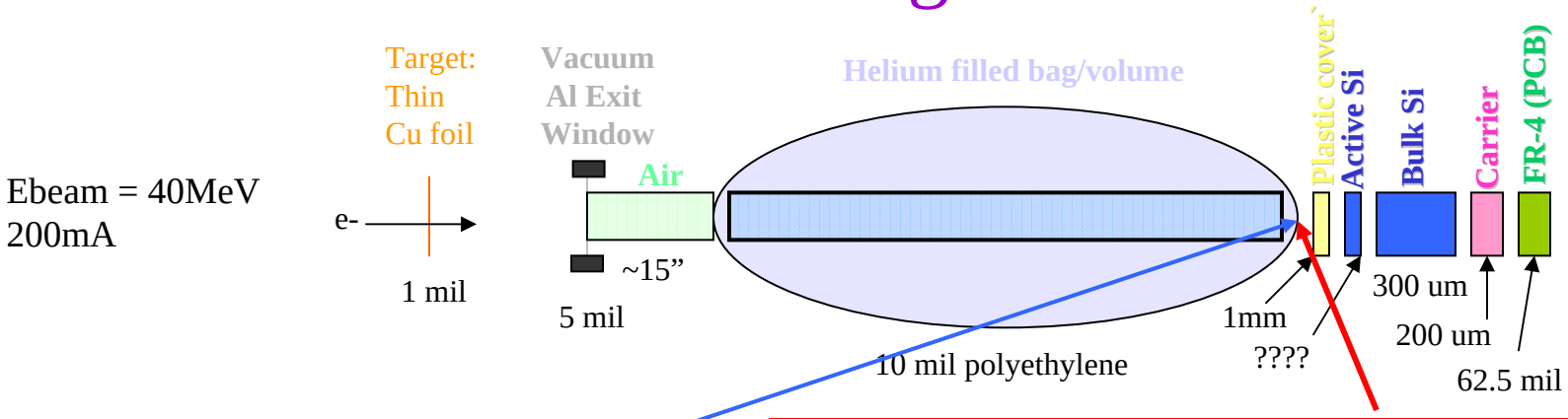


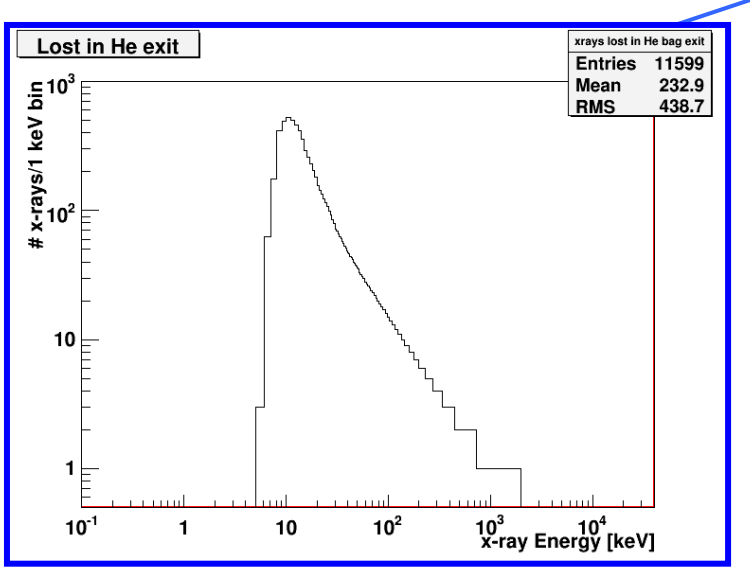


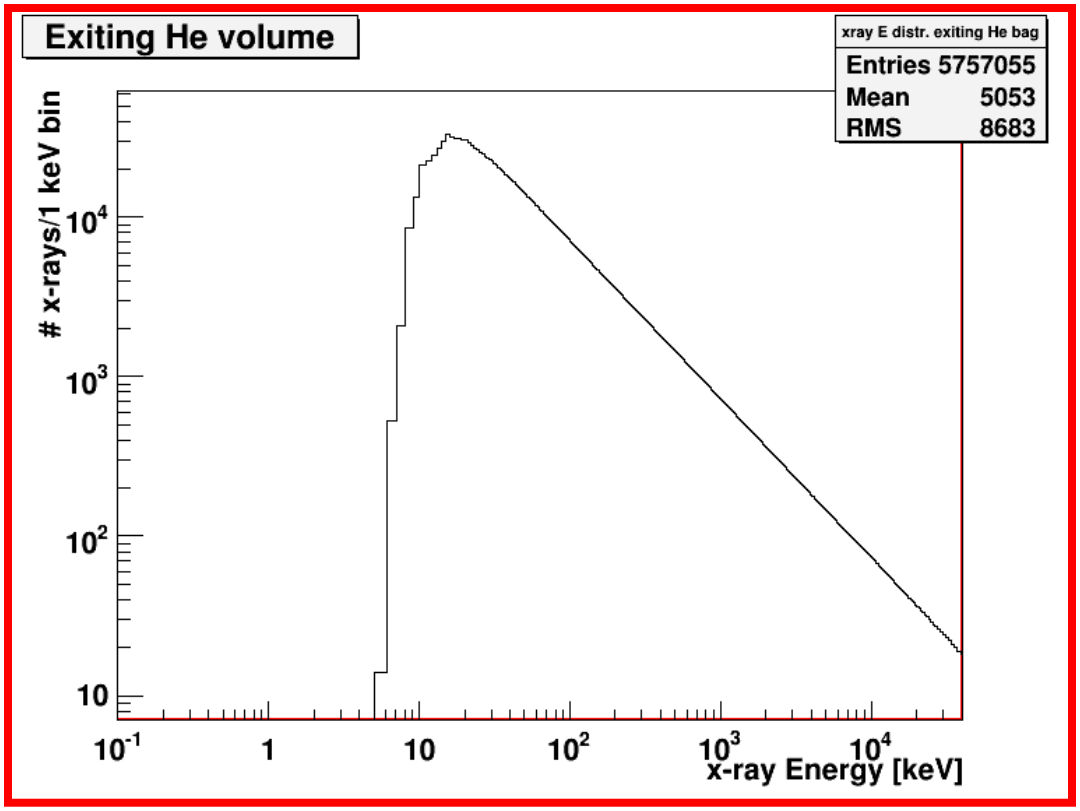


Single bunch

He bag exit

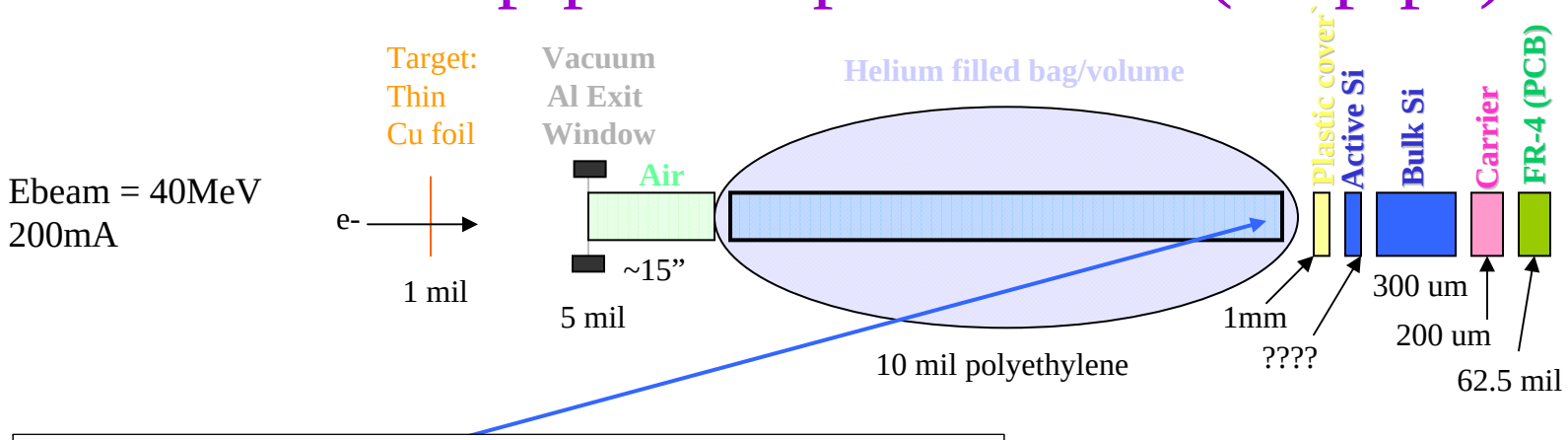


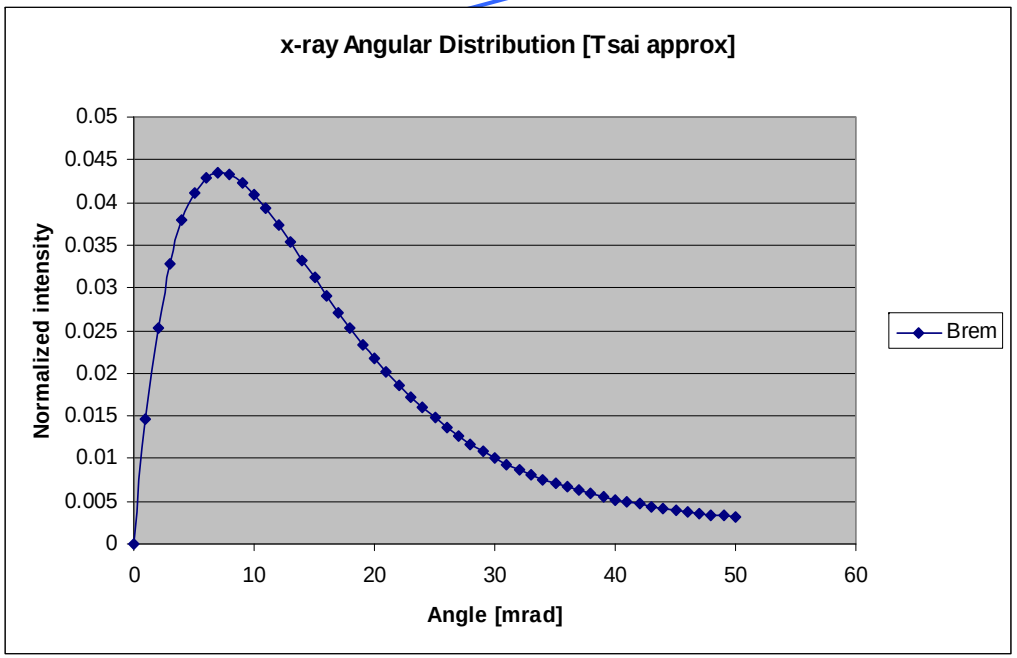




Single bunch

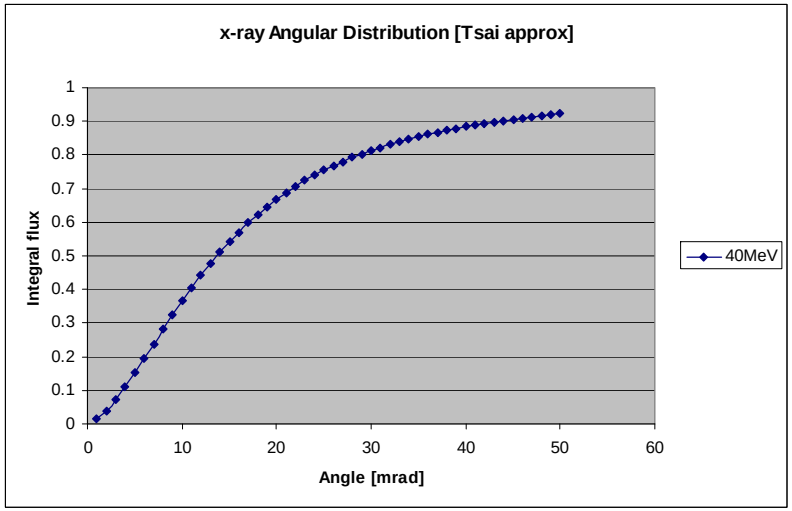
Beampipe acceptance loss (3” pipe)





Assume centered (can put in offset later)
3.81cm rad @ 10m ~ 3.8mrad

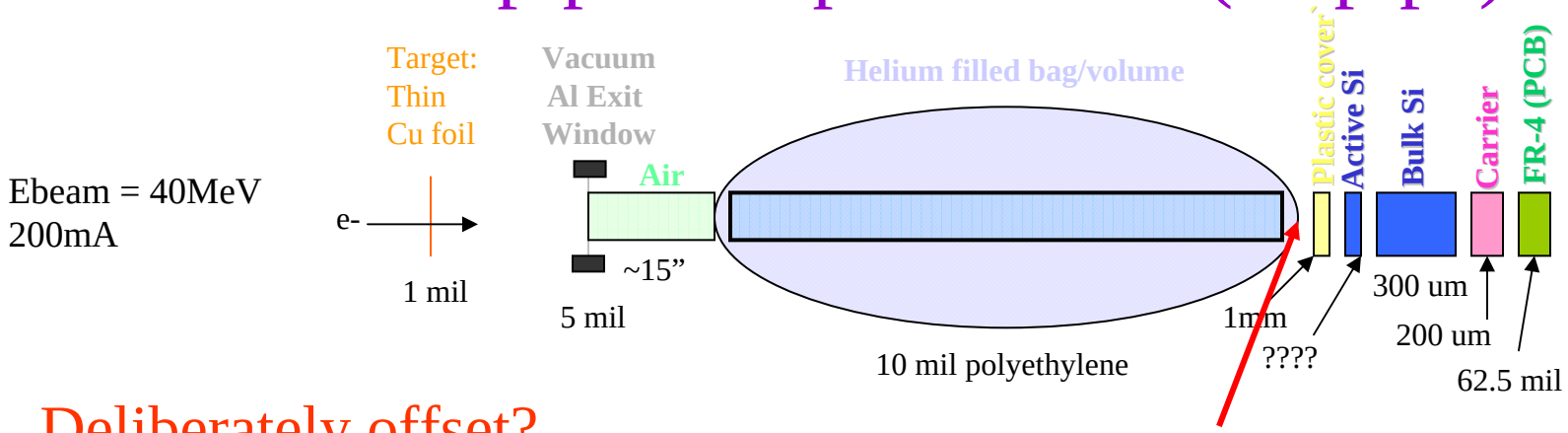
~10% (90% scrape/collimate)



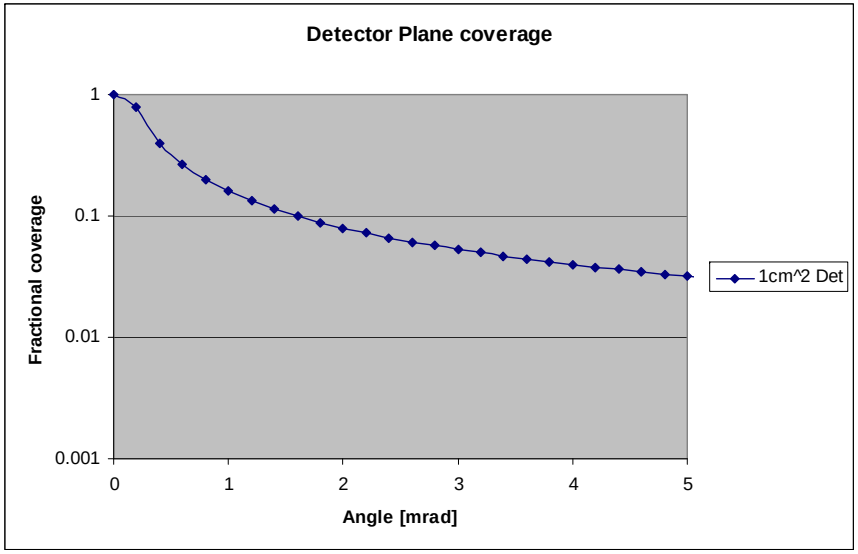
Tsai approximation:
Basically a double exponential

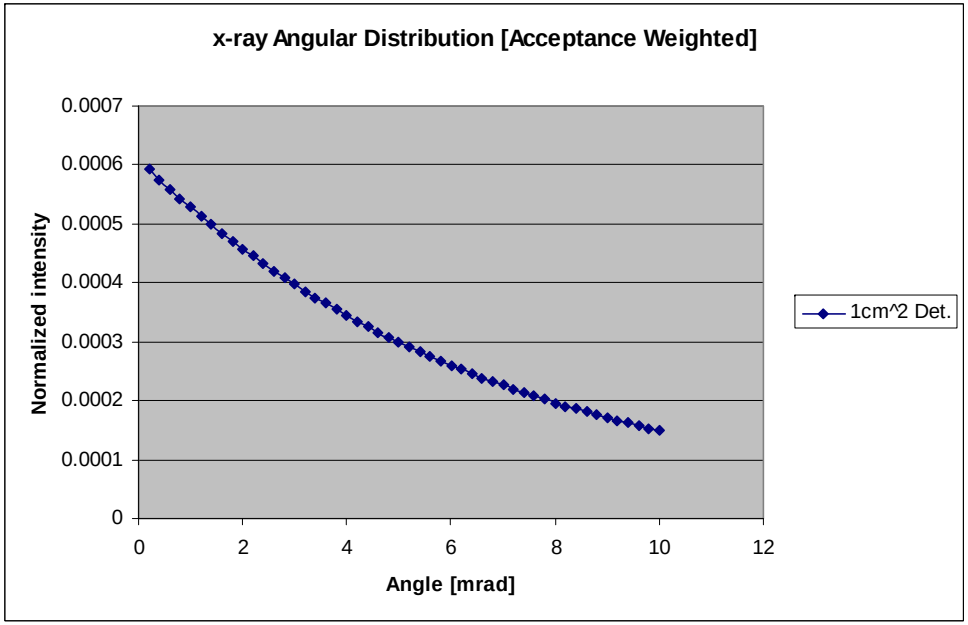
12.5mrad is 50% point

Beampipe acceptance loss (3” pipe)

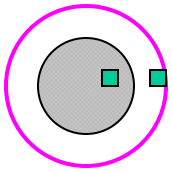


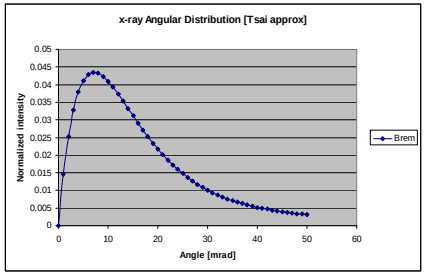
Deliberately offset?





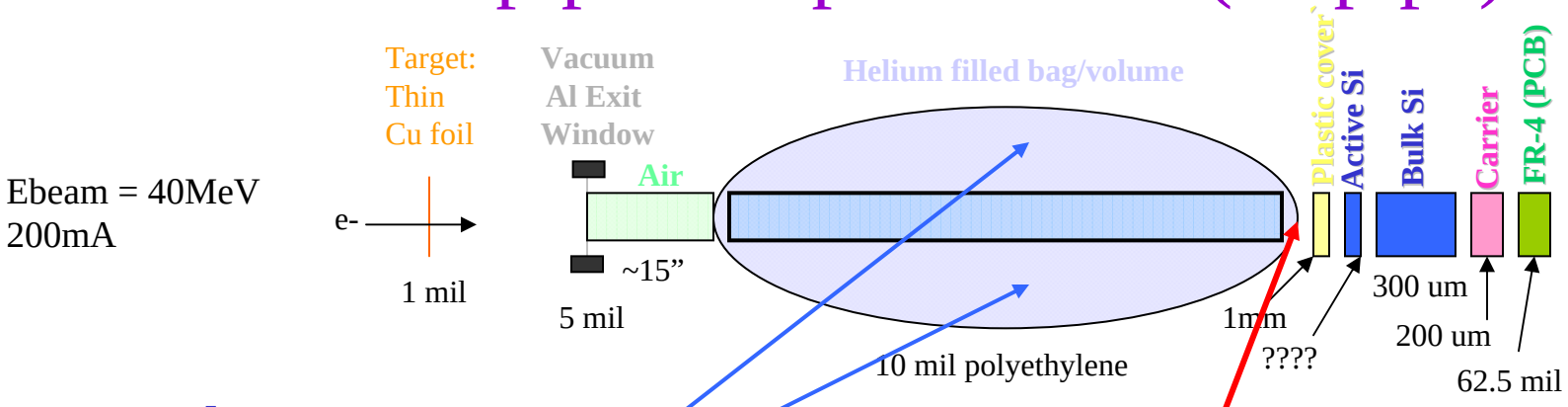
1cm^2



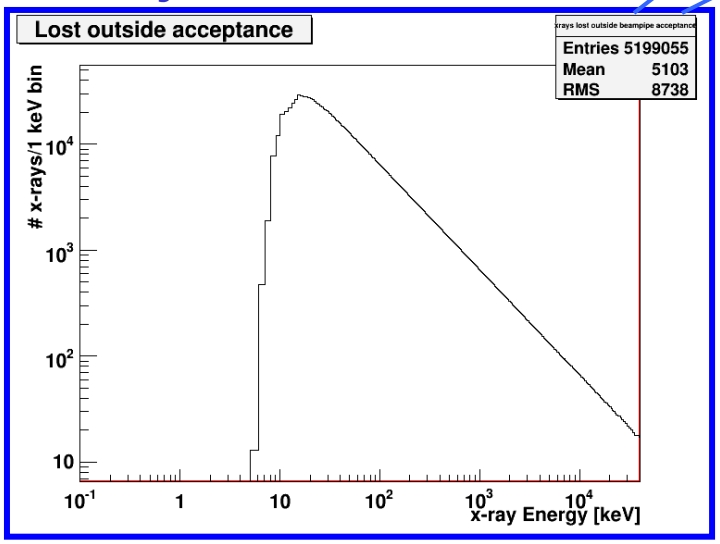


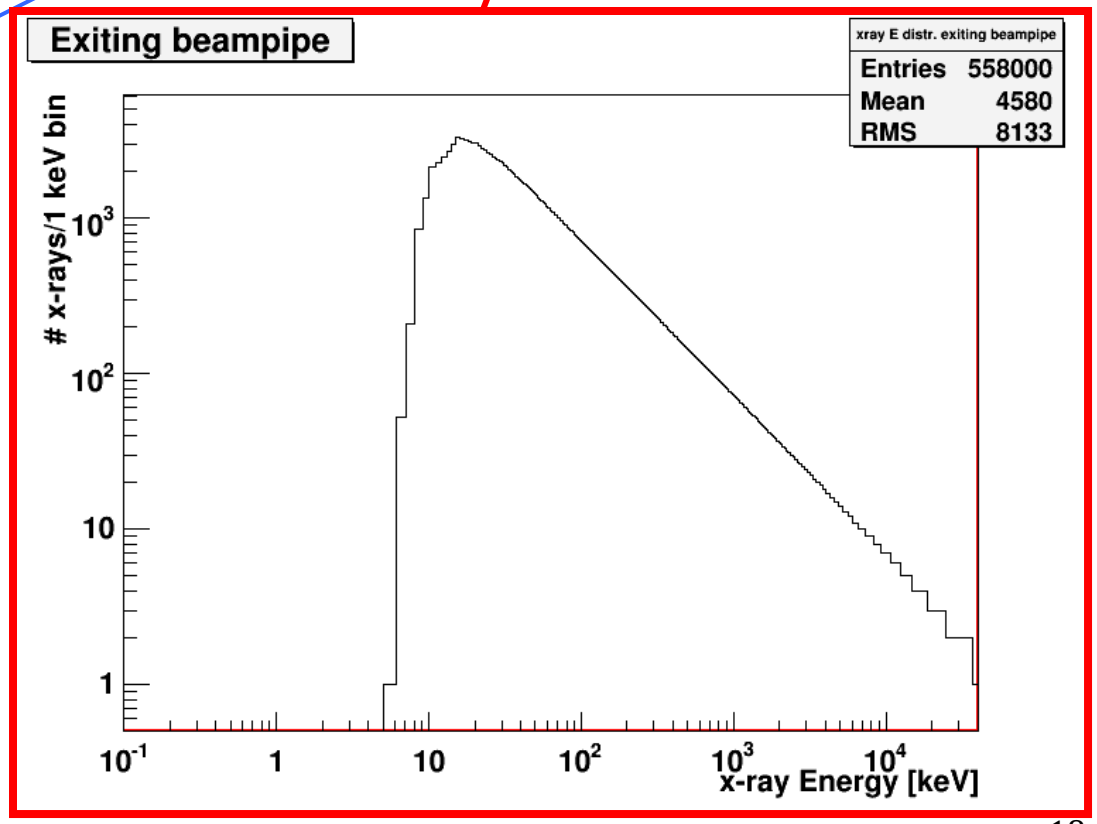
- Not very sensitive to alignment
- Better on axis

Beampipe acceptance loss (3” pipe)



Xrays lost

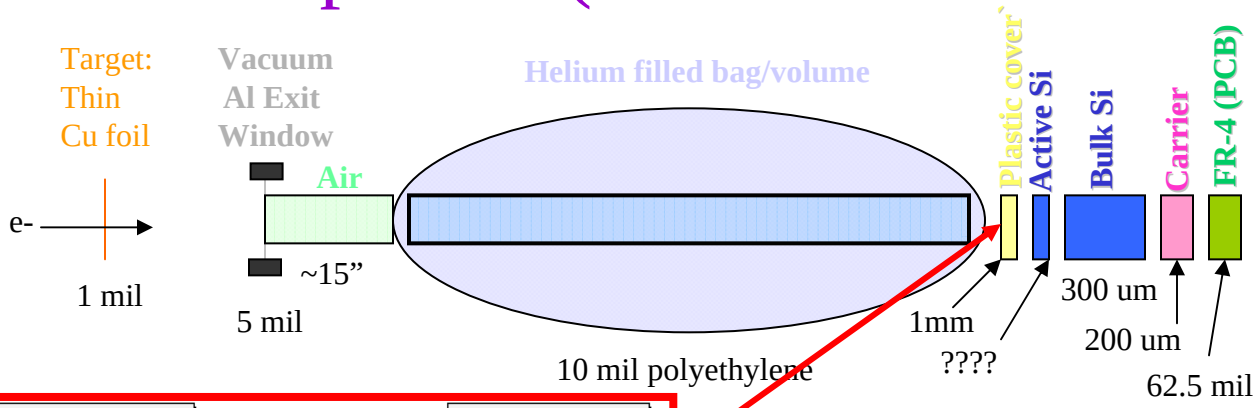


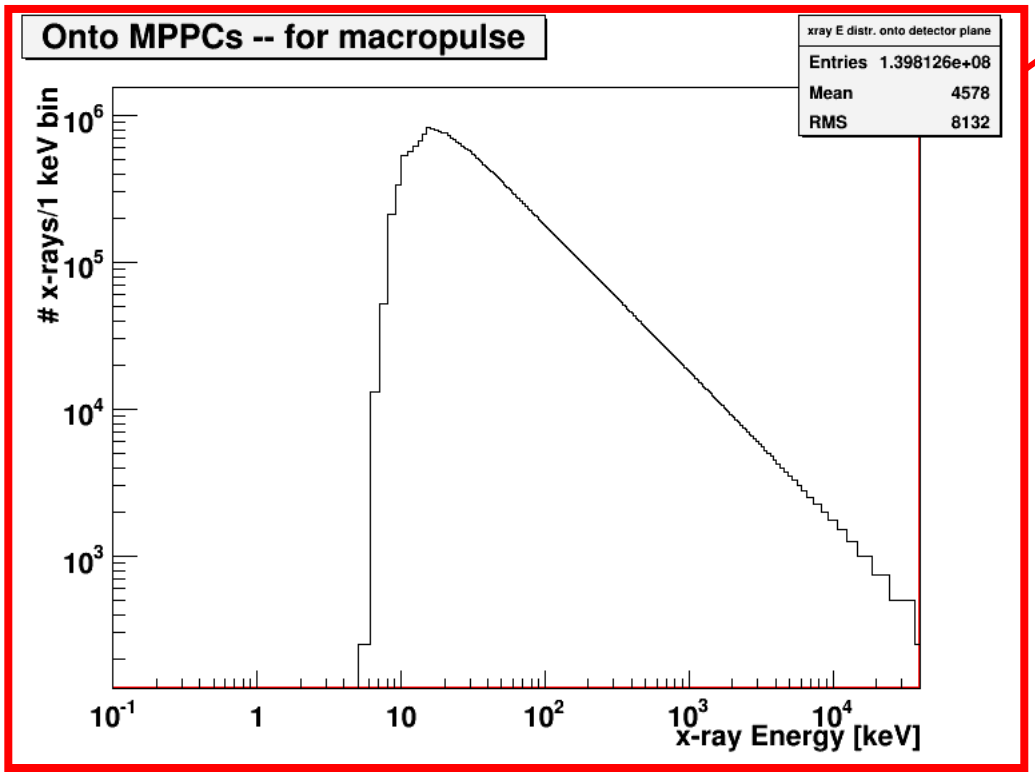


90% lost:
Shielding?

Detector acceptance (1cm^2 instrumented)

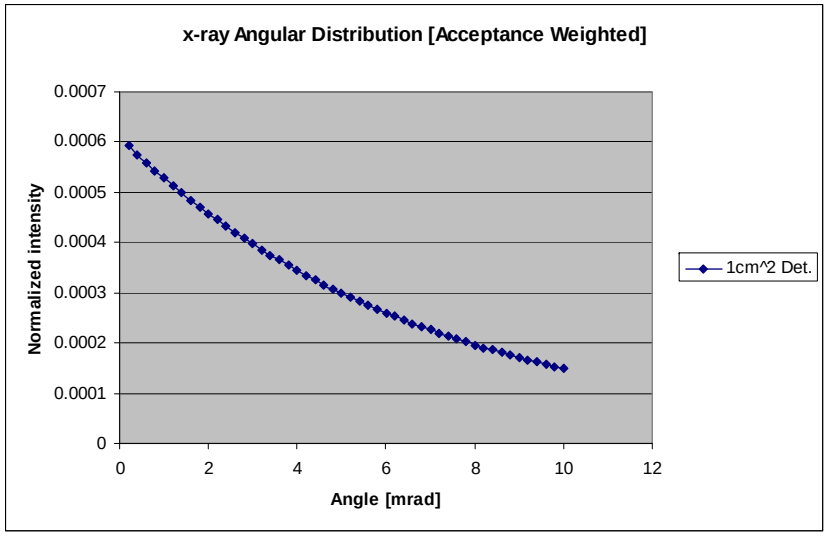
Ebeam = 40MeV
200mA





Assume uniform (can put in offset later)
Adet = ~ 2.2% coverage

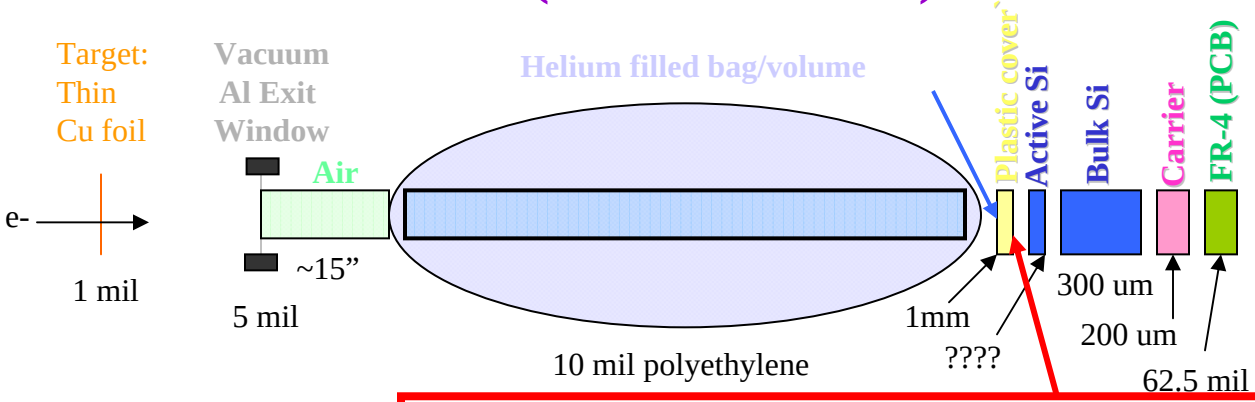
2×10^{-4} per $1mm^2$ detector

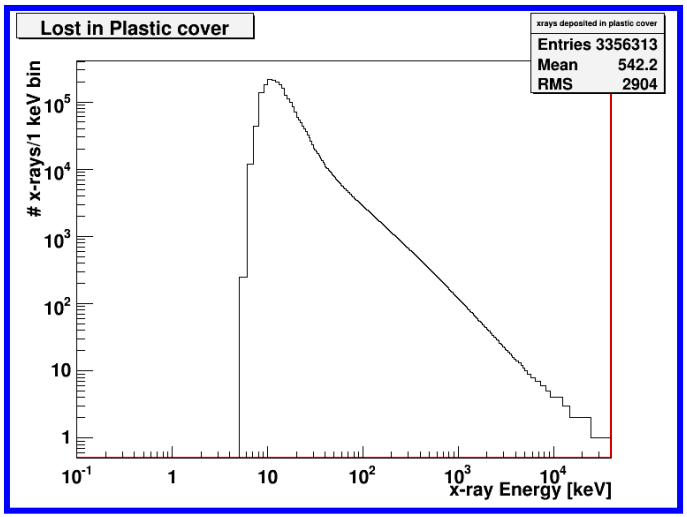


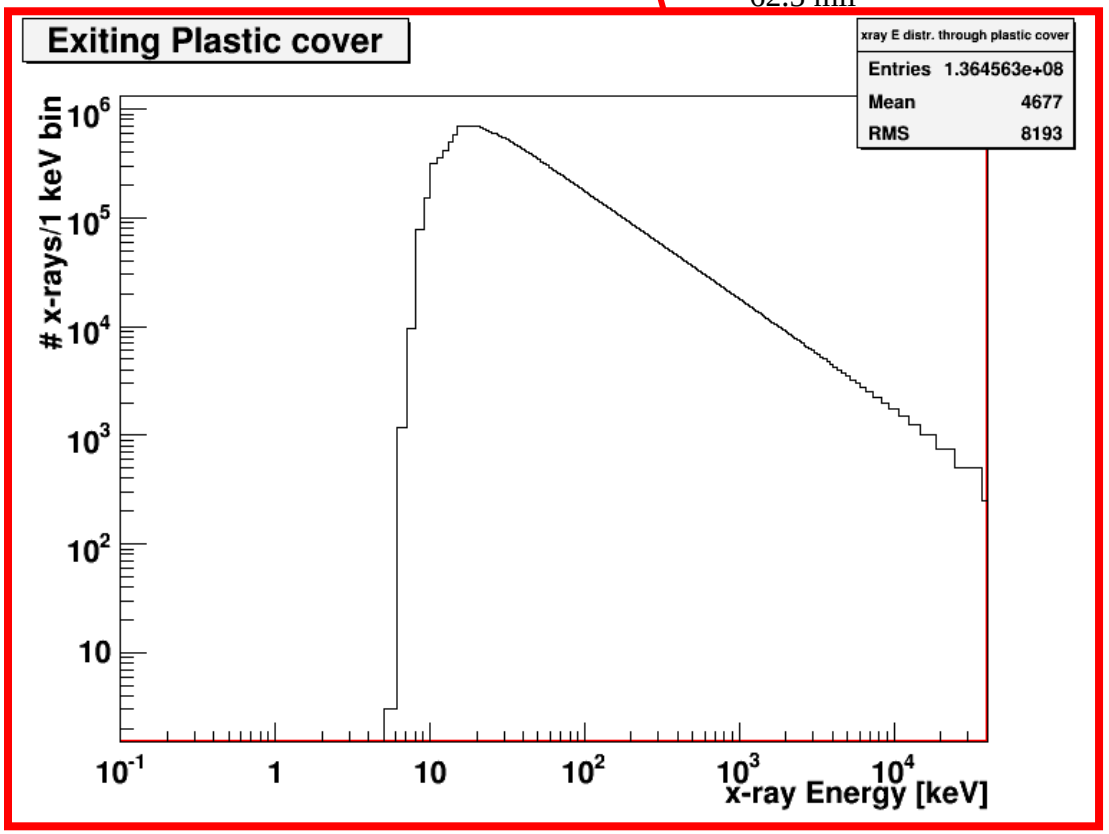
Per train (macropulse) flux estimate

Plastic cover (1mm thick) loss

Ebeam = 40MeV
200mA

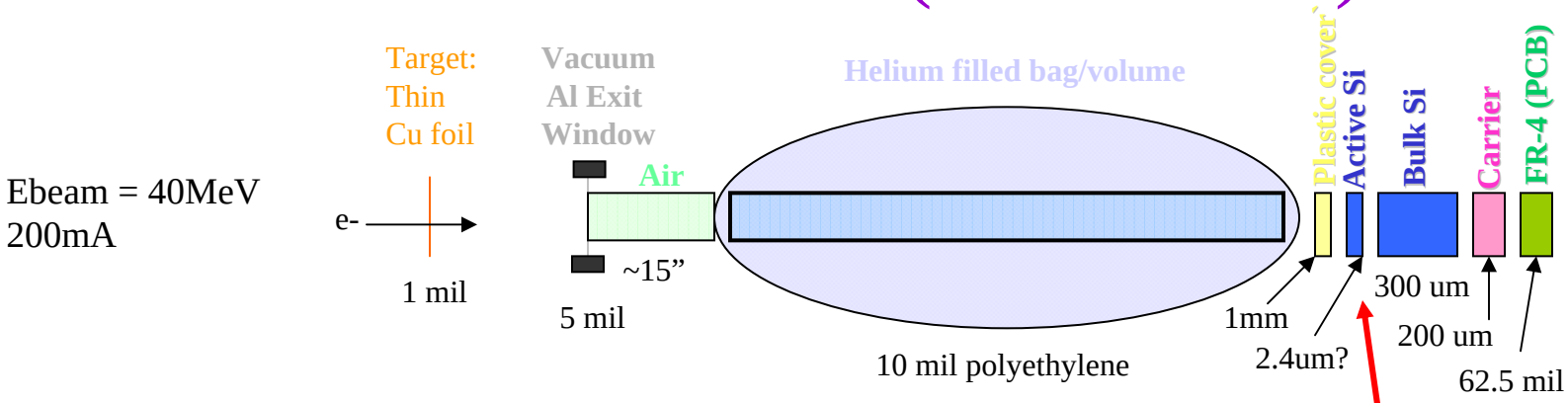






Macropulse

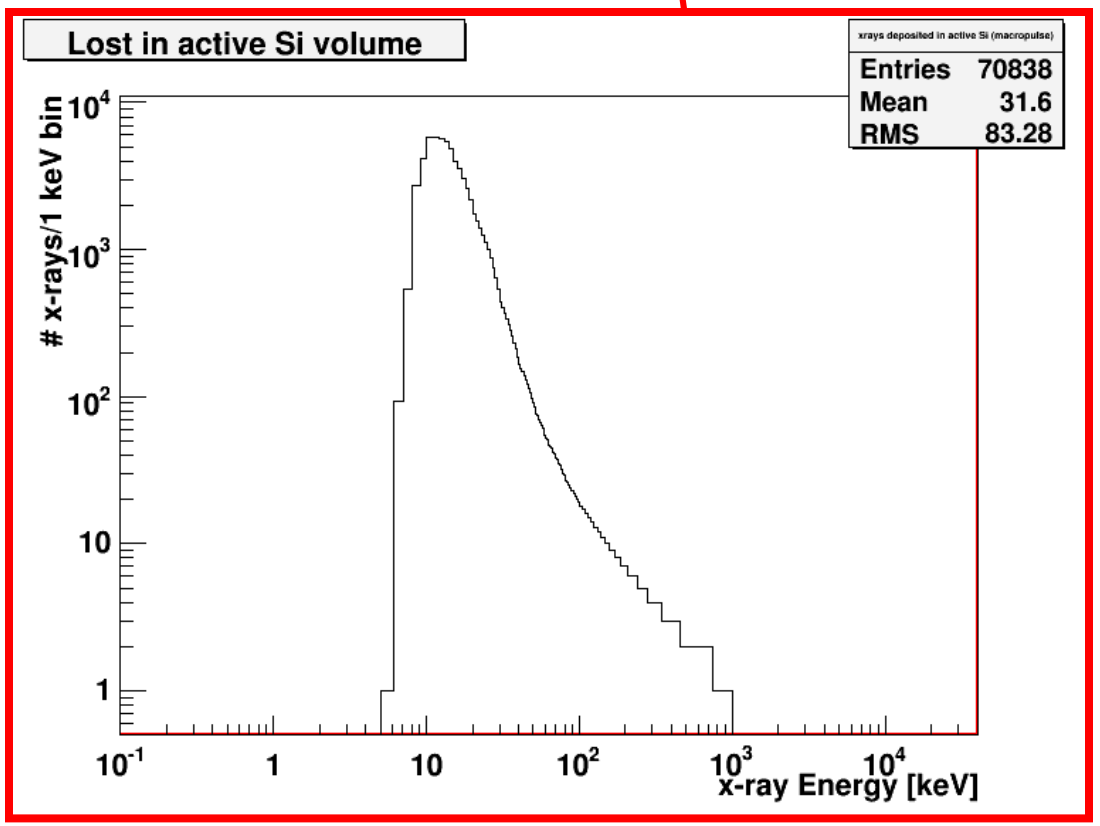
Active Si volume (2.4um thick) loss



Macropulse (guess based on $3x10^5$V/cm breakdown)

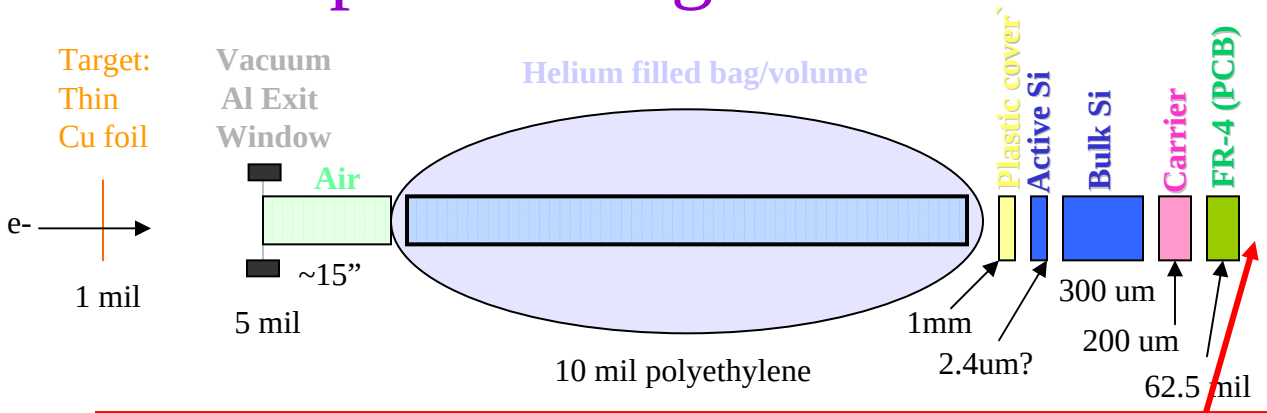
~7 x-ray/bunch
(~1 with fill factor)
Peaked 10-20keV

Propose first layer
As bare devices

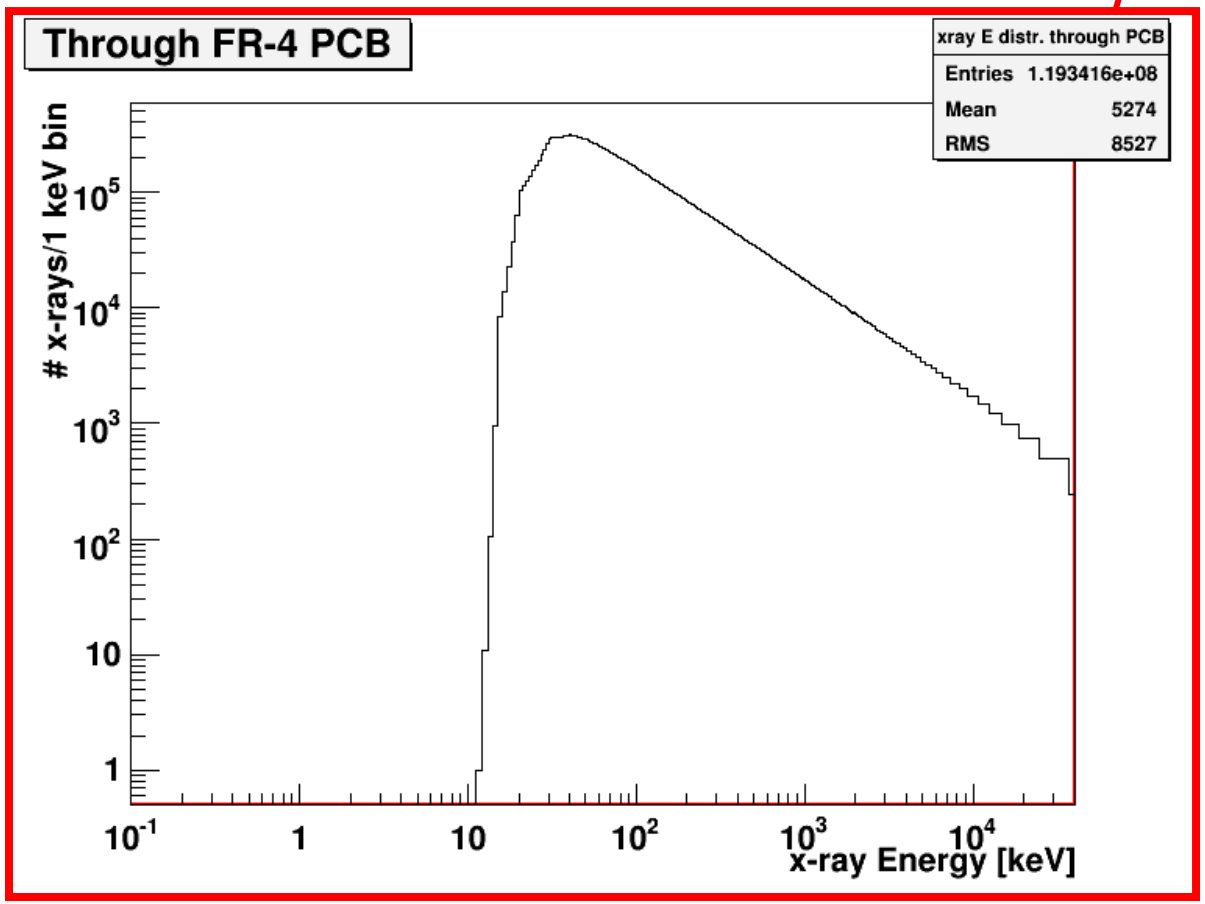


A penetrating beam

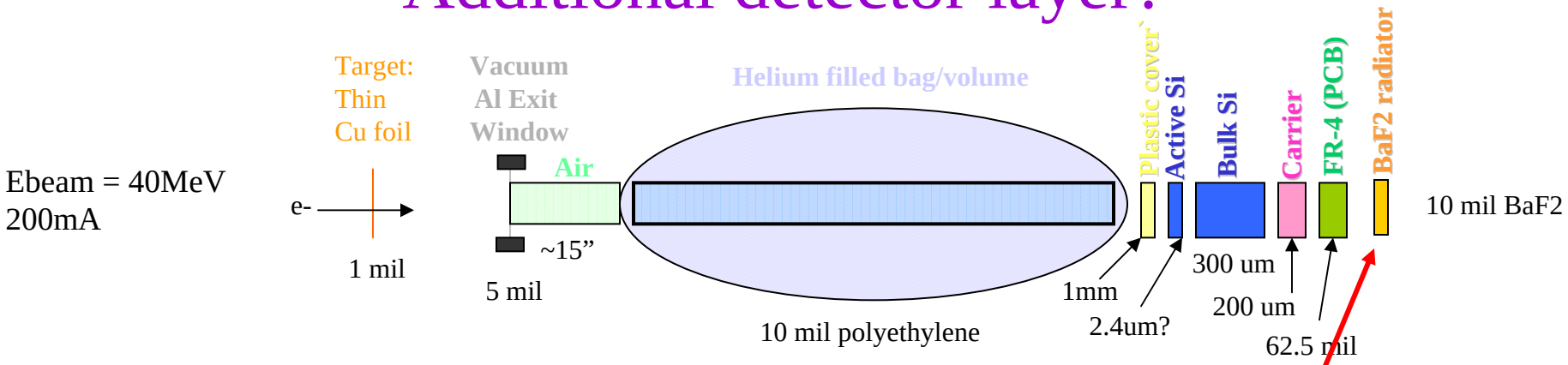
Ebeam = 40MeV
200mA

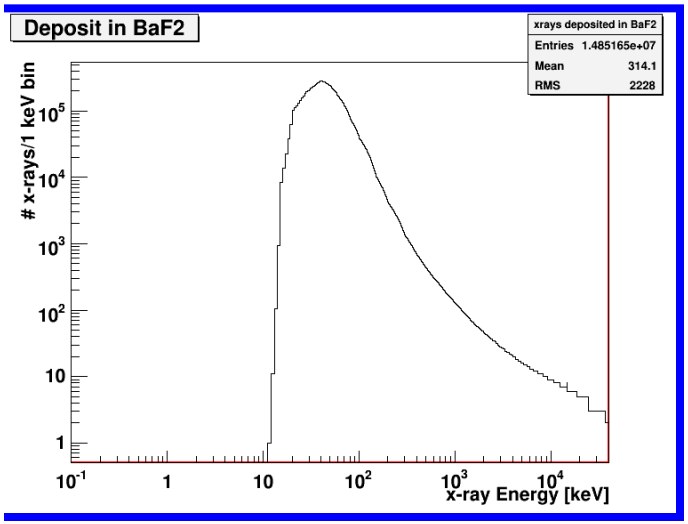


Macropulse

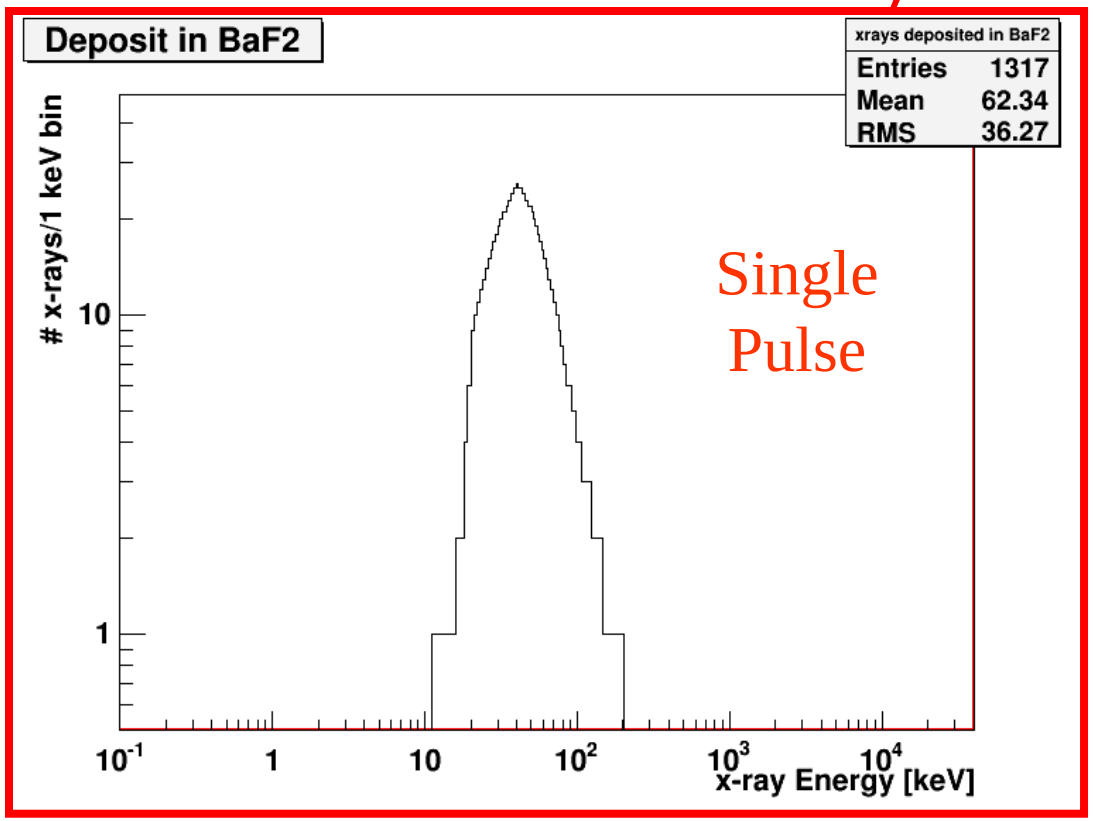


Additional detector layer?





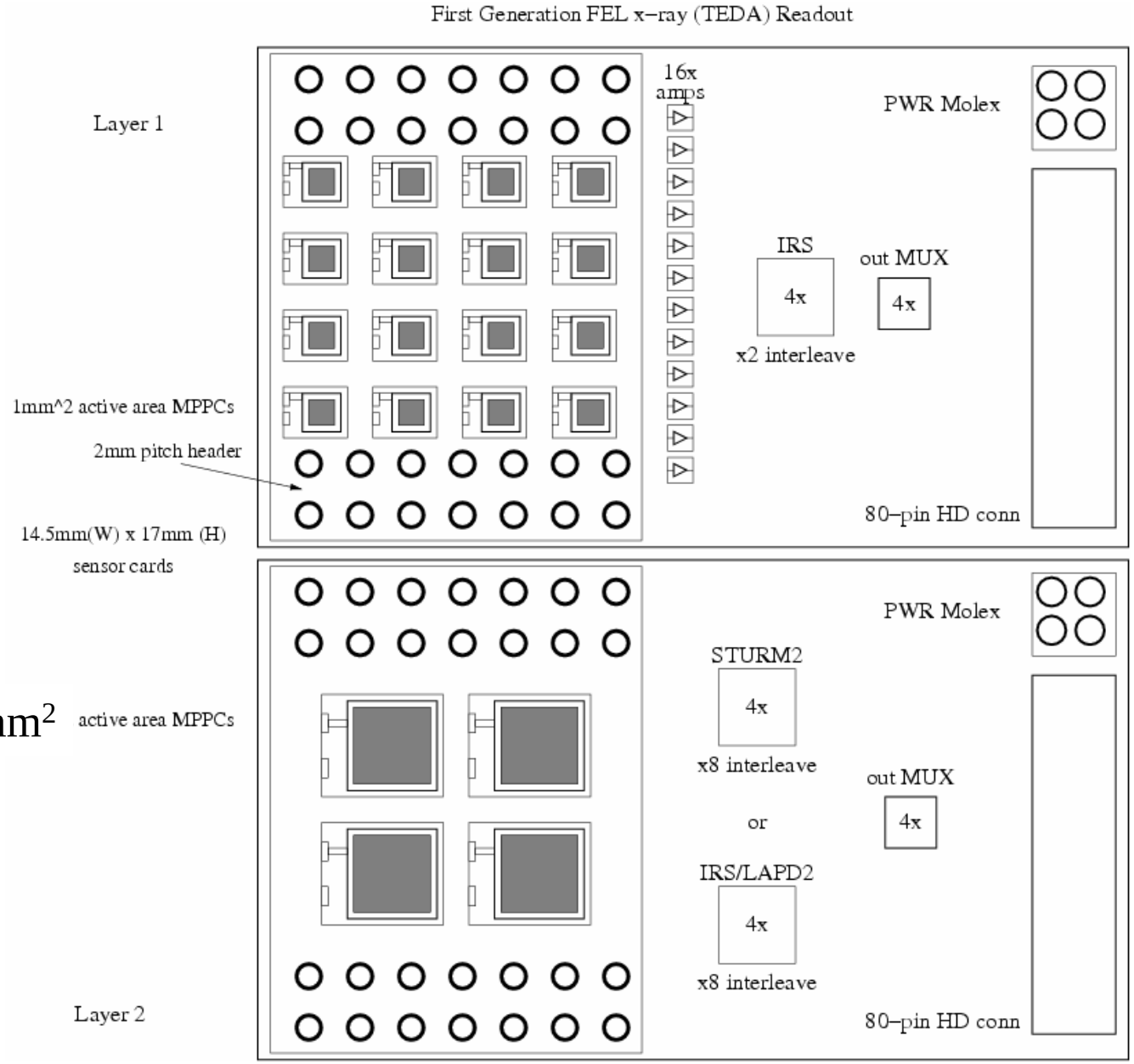
Macropulse



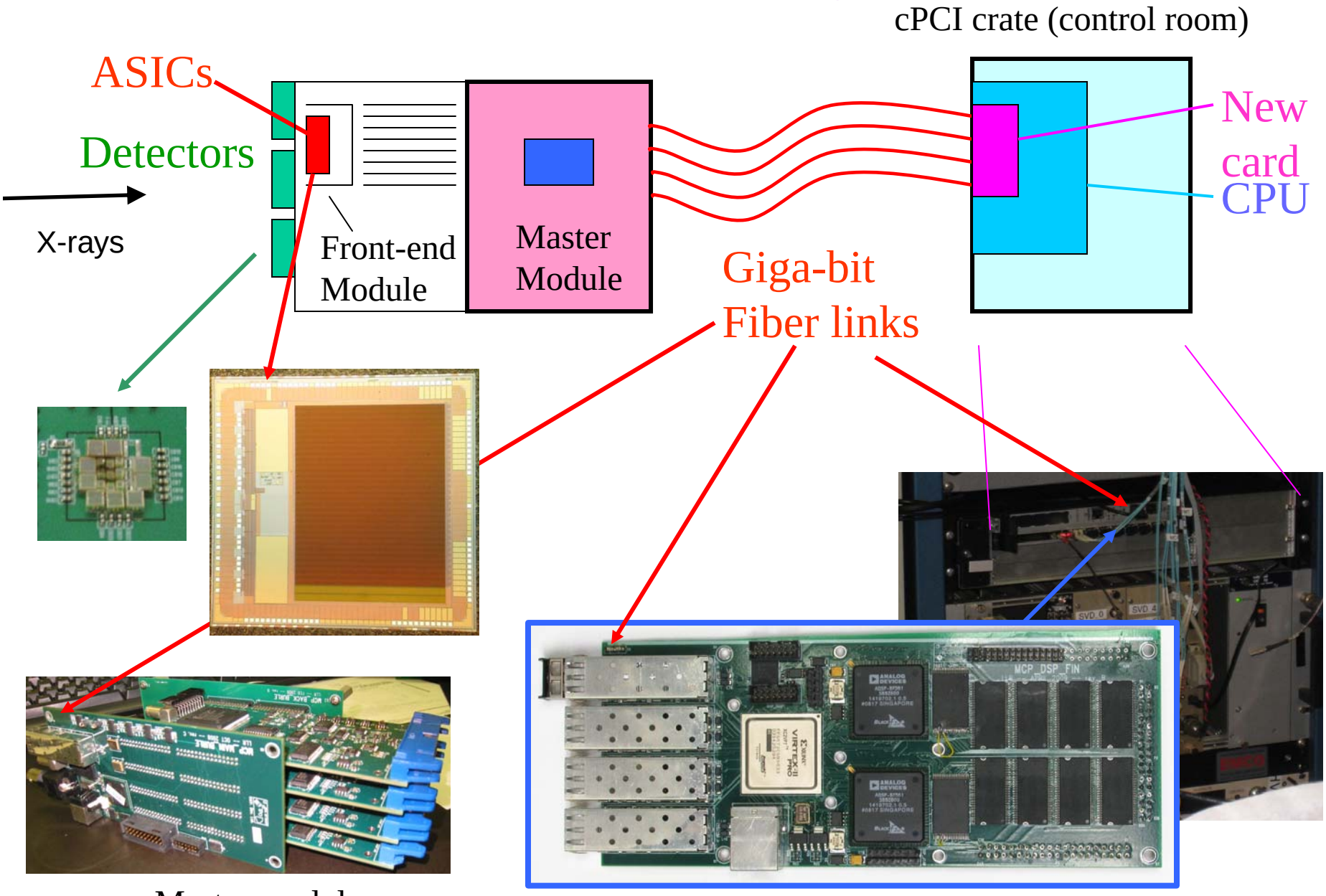
Brem beamline Summary

- Propose 2 detector planes
  - 1mm2 array for “bare” layer
  - 3mm2 array with BaF2 radiator
- More than adequate flux (2nd layer)
- Developed x-ray transport simulation
  - Input to a signal Monte Carlo
  - Fix readout/ASIC design specifications

Proposed First Detector Array

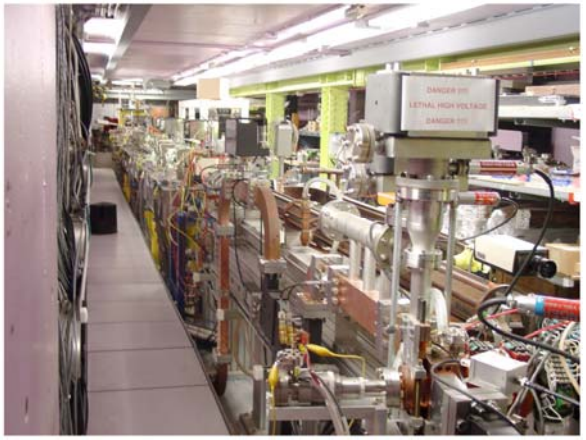


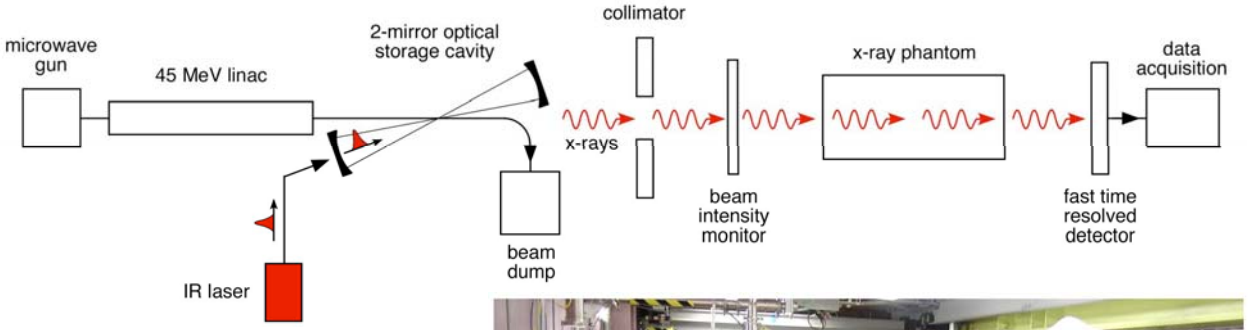
Readout for FEL x-ray beamline

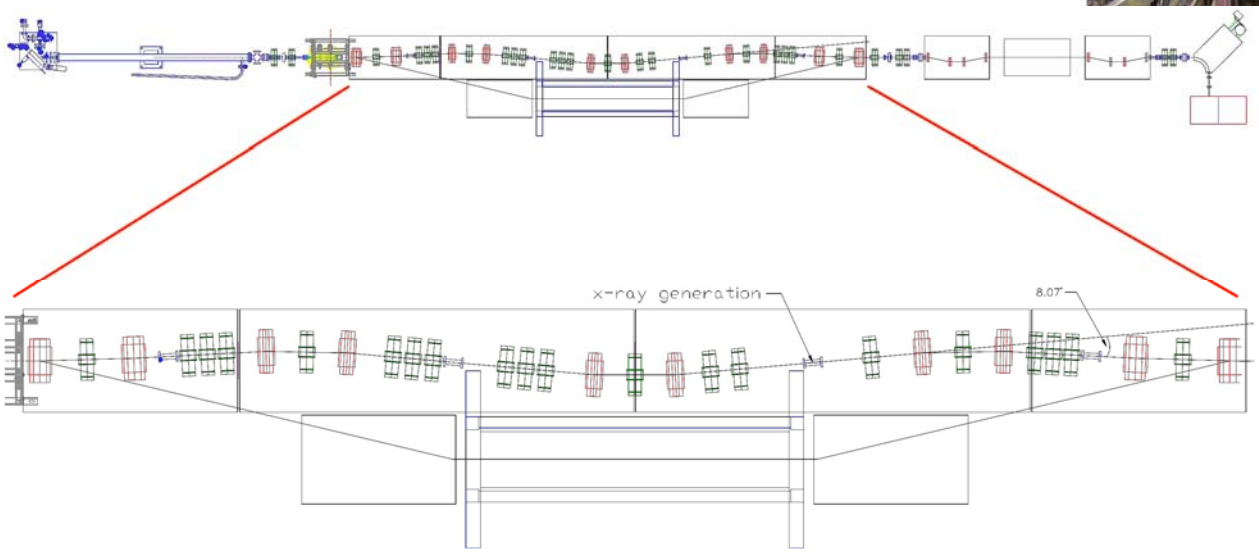


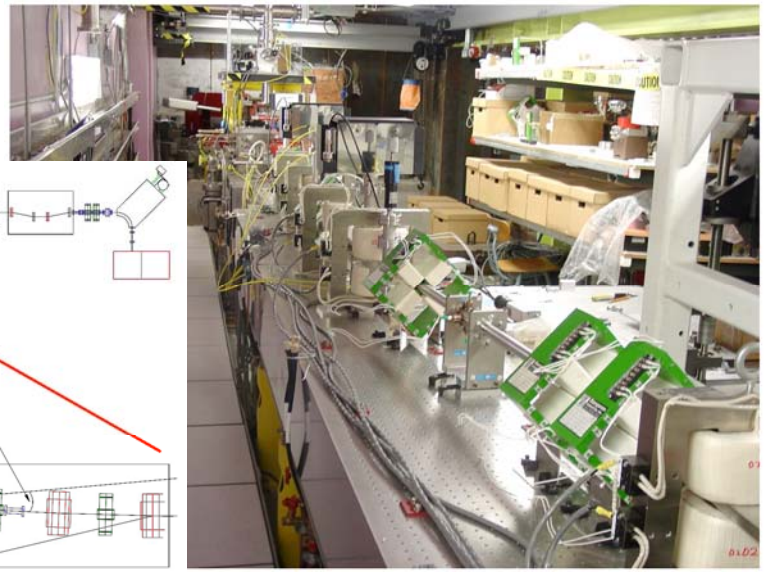
Master module

Eventual Source



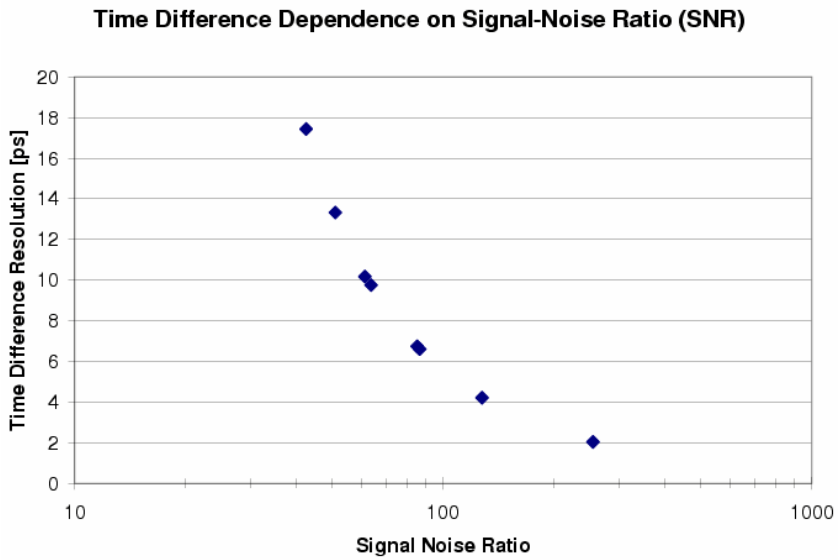






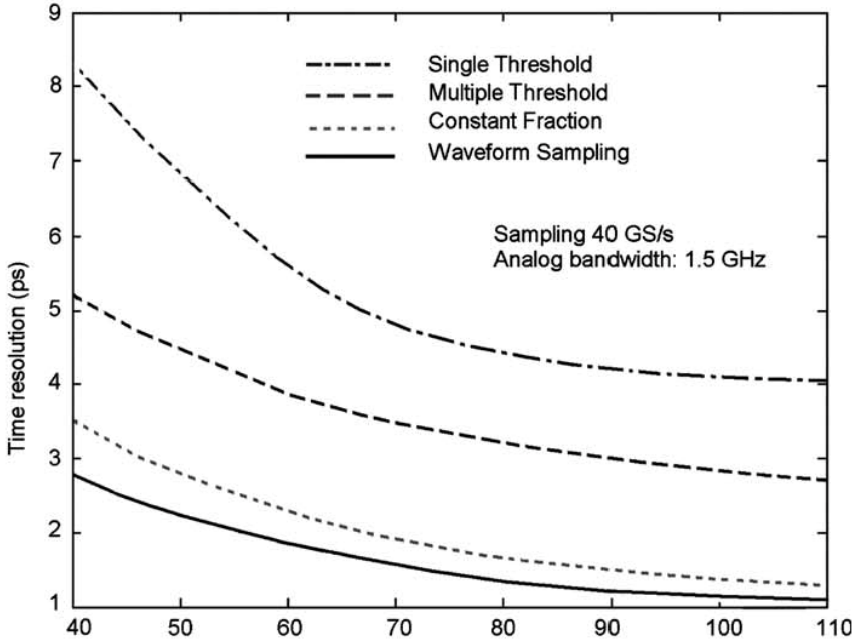
Front-end Electronics studies

1GHz analog bandwidth, 5GSa/s



G. Varner and L. Ruckman
NIM A**602 (2009) 438-445**.

Simulation includes detector response



J-F Genat, G. Varner, F. Tang, H. Frisch
NIM A**607 (2009) 387-393**.

Proto ASIC psTDC1

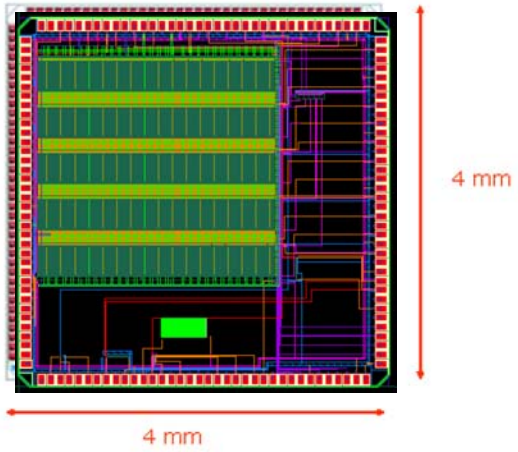
“oscilloscope on a chip”

Specifications

- 10-15 GSa/s
- >= 2GHz analog bandwidth
- 256 sample cells
- 4 channels
- separate timing channel
- on-chip conversion
- IBM 130nm CMOS process
- 25.6μs readout
- 40mW/channel
- Direct interface (stud-bond) to microstrip board

ASIC in evaluation

Chip Layout



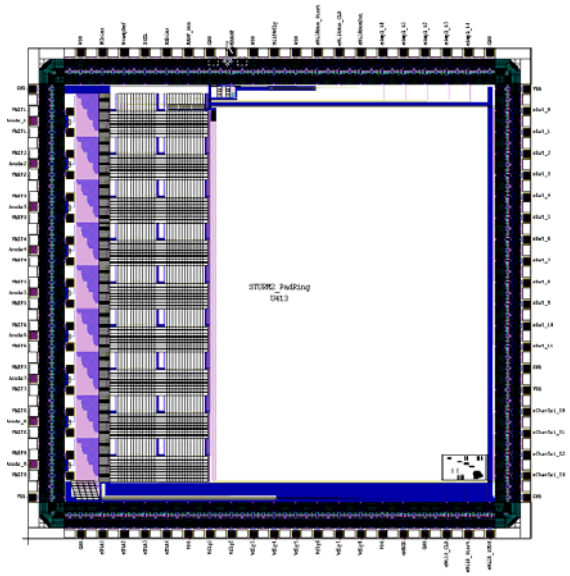
STURM2 Prototype (evol. Step)

"Max bandwidth/throughput"

Specifications

8	channels/STURM sampling
1	monitor channel
4	TSA sample buffers
8	samples/TSA buffer (32x channel)
288	Wilkinson conversion cells
1-200	GSa/s effective (5ps - 1ns Tstep)
1	word (RAM) sample readout
1+n*0.02	us to read n samples
100	kHz sustained readout (orbit)

Chip Layout



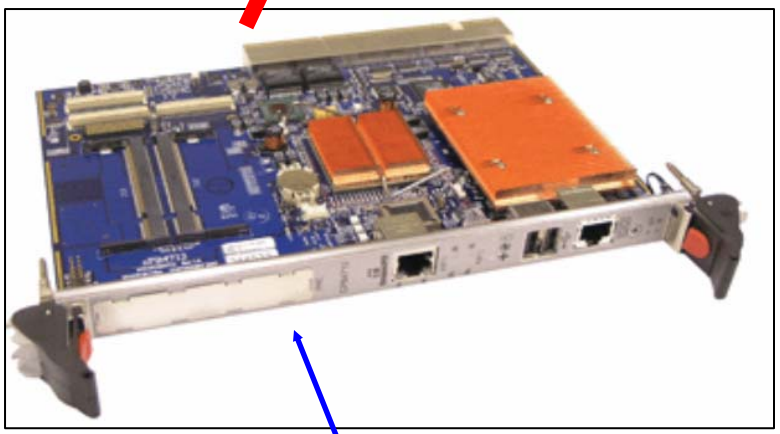
ASIC in fabrication

~20GHz (onto ASIC)

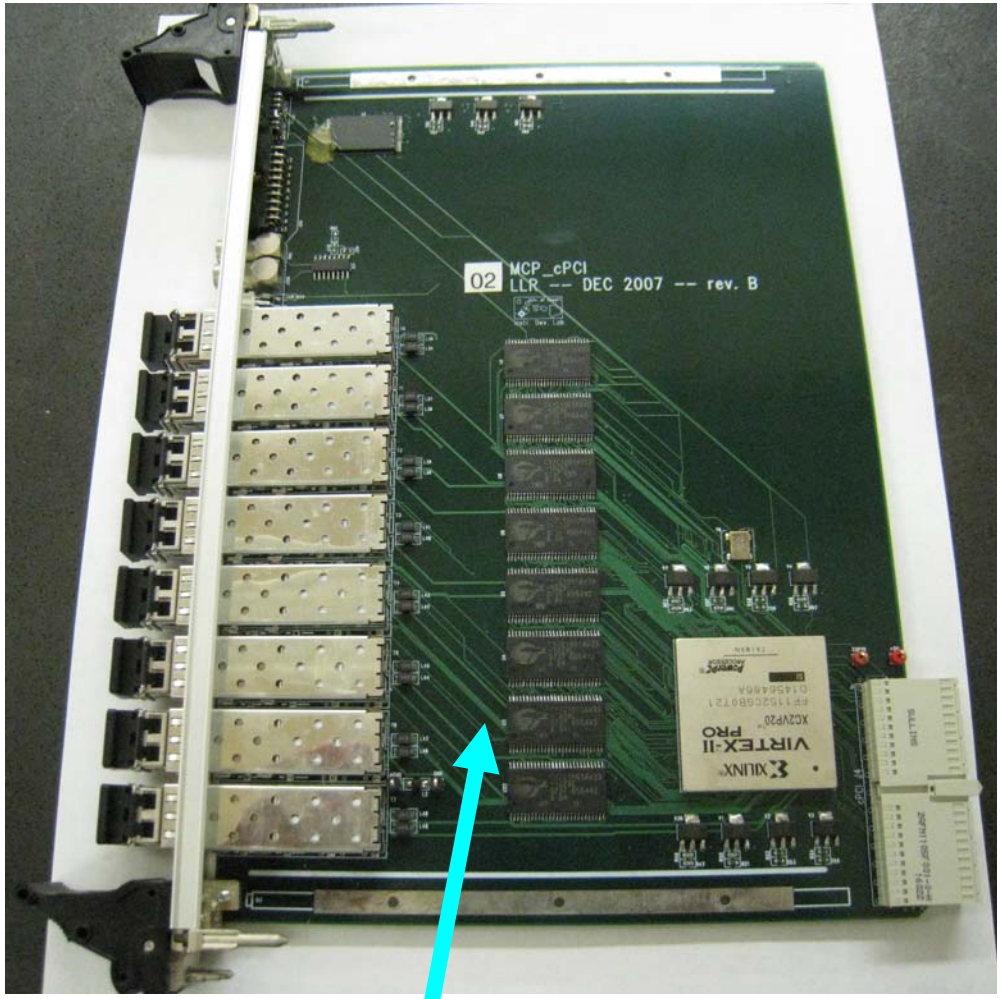
2.5GHz (into storage cell)

compact PCI Platform

cPCI crate



cPCI CPU



Data processing card

(example – DSP version)

First Prototype throughput

- For configuration shown earlier
  - 1 layer = 4 ASICs (8Ch.)
  - 1 “shot” = 4 chip * 8Ch * 32k = 1Msmp/layer
  - (1 shot = 8us recording @ 8GSa/s) [IRS]
- 16Mbit/s/shot
- 320Mbit/s @ 20Hz operation
  - 2x Layers/fiber ~ 0.64 Gb/s (20% capacity)
  - May do 1 fiber/layer for convenience (fibers are inexpensive)
- 40MBytes/s raw data (need to feature extract)

Readout System Summary

Progress on all 4 tasks

- If no major issues raised today, will complete write-ups, get feedback from the gang, and submit for review
- Now have a clear plan for late Feb. first run (on schedule)
- ASIC development path is multi-prong, design effort will intensify this semester
- Data transfer architecture has plenty of margin and is scaleable upward