Front-end electronics of the Compact High Energy Camera

S.A. Leach a,∗, J.S. Lapington a, D. Ross a, J. Thornhill a, C. Duffy a, S. Funk b, A. Zink b, D. Jankowsky b, R. White c, J. Zorn c, L. Tibaldo c, G. Varner d, A. Okumura e, H. Tajima e, J. Watson f

a University of Leicester, UK
b Friedrich-Alexander-Universität Erlangen-Nürnberg (FAU), ECAP, Germany
c MPI für Kernphysik, Germany
d University of Hawaii, United States
e Nagoya University, Japan
f University of Oxford, United Kingdom

A R T I C L E I N F O

Keywords:
CHEC
TARGET
CTA
Front-end electronics
Silicon photomultipliers
Readout
SST-2M
Full-waveform readout

A B S T R A C T

The Compact High Energy Camera is a focal plane camera designed for two mirror Schwarzschild-Couder design imaging air Cherenkov telescopes such as the SST-2M variants on the Cherenkov Telescope Array. It utilises a 2048-pixel array of silicon photomultipliers arranged in thirty-two 8 x 8 pixel tiles. Each detector tile is instrumented with a front-end electronics module designed to provide single photon counting with sub-nanosecond timing, full-waveform digitisation and event triggering capabilities based around TARGET ASICs. Performance results including triggering, digitiser noise, signal crosstalk, linearity and dynamic range from initial laboratory tests have been collated and are presented.

1. Introduction

The Compact High Energy Camera (CHEC) is an ultra-sensitive single-photon counting camera being developed to image Cherenkov light flashes, peak \( \lambda \approx 400 \text{ nm} \), generated during gamma-ray initiated particle showers. CHEC-S is the second prototype version camera and uses silicon photomultiplier (SiPM) pixels whereas CHEC-M, the first prototype, is based on multi-anode photomultipliers. The development and characterisation of CHEC-M, in the laboratory and on-telescope, validated the CHEC concept [1] and enabled several technical improvements to contribute to a new design. CHEC-S is currently undergoing full characterisation with on-telescope observations being planned for spring 2019. This article describes the new Front-End Electronics (FEE) modules developed and optimised to instrument imaging air Cherenkov telescope cameras equipped with SiPM photodetectors.

2. Front-end electronics

The new CHEC-S FEE camera modules (Fig. 1: schematic layout, Fig. 2: photograph) each accommodate 64 identical channels, enabling 2048 discrete pixels to be read out by 32 modules in each camera. CHEC-S uses \( 3 \times 3 \text{ mm}^2 \) SiPMs grouped in fours resulting in 6.4 mm\(^2\) pixels. Each signal channel comprises a fast analogue shaper to optimise the pulse characteristics (\( \approx 8 \text{ ns FWHM} \)) for the high-speed digitiser, and a slow readout of pixel photon count rate to enable star tracking for telescope pointing determination. Designed around full-waveform digitisation, the CHEC-S modules utilise the latest generation TARGET switched capacitor array ASIC for fast, low power digitisation [2].

Optimisation. The updated FEE module design, led by the University of Leicester in the UK, includes physically separate analogue and digital functionality, to minimise crosstalk, split trigger and digitiser operation, and optimised electromagnetic shielding. Power conditioning for the FEE and silicon photomultiplier array has been moved to a separate PCB which also houses additional housekeeping monitoring functionality (Fig. 3). Module temperature is stabilised (\( \approx 23 \degree \text{C} \)) by circulating cooled air inside the camera with excess heat extraction via an external water chiller.

TARGET CHIPSET. Conditioned event pulses are fed to the latest generation TARGET chipset which consists of a high speed 1 GS/s 12-bit digitiser (TARGET C) in parallel with a trigger chip (TSTEA), acting on summed groups of 2 x 2 channels known as “super-pixels”. The latter provides a first level over-threshold trigger which is processed by a pattern-matching algorithm to generate a camera trigger for a validated event. Valid event determination results in a full readout of the camera,
Fig. 1. CHEC-S schematic layout with the FEE module section indicated.

Fig. 2. One of 32 identical FEE modules for CHEC-S. Each has 64 independent pixel channels optimised for Cherenkov flashes with full-waveform digitisation of the 8 ns shaped event pulses.
each of the FEE modules providing 64 digitised waveforms of typically 96 ns duration, and can be elongated if required.

**TARGET module features.**

- 64 signal channels
- 4 x T5TEA ASIC (trigger) - 16 LVDS trigger signals per module
- 4 x TARGET C ASIC (sampling) at 1 GSa/s
- 4 μs (16 μs possible) deep ring buffer
- Data via simple User Datagram Protocol (UDP)
- Firmware upgradable via UDP
- Slow signal path for pointing and Night Sky Background analysis
- ns trigger timing on module
- Tunable offset (voltage pedestal) for each channel (trigger and sampling)
- 3 PCB stack (Primary, Auxiliary, Power)
- 16 HV bias groups

**Full-waveform capture advantages.** A major feature of the CHEC design is the ability to digitise and read out a complete event signal with 1 ns resolution. This has many advantages over peak detect counterparts: The signal dynamic range is extended from \(\approx 500\) to over 2000 photo electrons (pe) by using pulse reconstruction of the saturated waveforms, precise (per pixel) event arrival time spanning the typical 100 ns readout window (essential for transit tracking high-energy gamma-ray events), background event rejection and can be used for advanced image cleaning.

3. **Trigger performance**

The FEE module triggers on an analogue sum of four channels (super-pixels) and is configured through several T5TEA parameters which are established during module calibration, performed at ECAP, Erlangen. These parameters include a per channel voltage pedestal, a per trigger-group DC offset and trigger width trim, and a signal threshold level. Fig. 4 illustrates the minimum trigger threshold for each channel with a typical triggering performance of \(<3\) mV (0.6 pe), compared to the previous TARGET T7/T5 results of 50/20 mV respectively [3]. Trigger noise is measured at 0.33 mV (0.1 to 0.15 pe) for all channels with sampling on \(23\,^\circ\mathrm{C}\) ambient.

4. **Digitising performance**

TARGET C digitiser noise has been measured on-module (without the photodetectors or buffer-preamplifier attached) using an external trigger. A unique electronic pedestal, value per storage cell/sample, is subtracted from the 96 ns readout window. Each ASIC channel used 4096 storage cells (of the 16384 available) and has a dynamic range of 1.9 V. Typical measured noise illustrated in Fig. 5 is 1.2 ADC counts \(\approx 0.6\) to 1 mV (RMS) (equivalent to \(\approx 0.2\) pe) across the whole module.
5. Signal crosstalk

Signal crosstalk between channels has been measured for both the primary and auxiliary boards (32 channels on each). By injecting a known amplitude signal pulse into a channel and measuring coincident crosstalk levels (pedestal calibrated) on the 31 corresponding channels illustrates all channels have <1% crosstalk (Fig. 6).

6. Calibration

Each FEE module requires a calibration process to compensate for slight variations in performance characteristics that occur along each signal path. Calibration normalises and linearises the response of each pixel channel. This process requires generation of Transfer Functions (TF) to correct for the non-linearity in the ASIC switched-capacitor response to signal amplitude. The TF, along with pedestal subtraction, is then used to reconstruct the charge. For TARGET, the TF also depends on the relative signal position in the storage array, plus AC effects (signal ≈80 MHz) of TF below ASIC bandwidth (>500 MHz). Therefore, the adopted approach for TARGET C is to measure the AC TF as follows:

- Contain module in a temperature controlled chamber;
- Inject signal-like pulse of known amplitude;
- Read ADC value of peak position (storage cell) and then step increase the amplitude to generate a cell-dependent lookup table. This procedure results in ≈100 MB of TF data per module which is stored and applied offline and used to calibrate camera image data.

Fig. 7 illustrates typical TFs measured across a complete module (64 channels × 4096 storage cells). These TFs are calculated and stored on a per-module basis and subsequently applied to camera acquired data for detailed calibrated analysis.

7. Conclusion

A new TARGET C/T5TEA ASIC based module has been designed for use with the SIPM based CHEC prototype camera. With a measured performance of: Trigger (2.38 ± 0.33) mV and digitiser noise of <1 mV RMS (≈0.2 pe), 32 calibrated modules have been integrated into the complete camera system at MPIK, Heidelberg. CHEC group members are currently performing detailed characterisation in the laboratory and are preparing for the first on-telescope trials in spring 2019.

Acknowledgements

We gratefully acknowledge financial support from the agencies and organisations listed here: www.cta-observatory.org/consortium_acknowledgments.

References