Aerogel RICH Readout

S. Nishida
KEK
Belle2Link

Nov 26, 2010
Introduction

Aerogel RICH Readout (Front end electronics)

HAPD (144ch)

ASIC (SA)

Preamp  Shaper  Comparator

Readout (Digital Part)

L1 buffer

Belle2Link

Total ~ 500 HAPDs.
ASIC: 36ch per chip (i.e. 4 chip / HAPD).
Quite limited space (~5cm) behind HAPD.
~500 Belle2Link is too many: need Merger.

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Aerogel RICH Electronics

- Front-end (FE) board: 4 ASICs and 1 FPGA to read out 1 HAPD.
- Merger board collects hit data from ~4 HAPDs (FE boards).
- Merger board has the interface to Belle2Link (i.e., Merger board is the “front-end” board in terms of unified DAQ).
- Conservative raw data rate = 100 Mb/HAPD.
  - 16 b/ch is assumed.
  - Zero-suppression is requested at merger board (or FE board).
• Prototype FE board is now being developed at Ljubljana.
  ✓ Main board with 4 SA02 ASICs and 1 FPGA (Spartan6).
  ➢ 12 layer board.
  ✓ Piggy board for SiTCP (for standalone readout).
• Unfortunately, delay due to a problem in the production.
  ✓ Production at Elgoline (Slovenia) : design submitted in September....
  ✓ Another candidate: PCBCORE (China).
Merger

- Prototype Merger boards need to be developed.
- Issues
  - Data transfer from FE board to Merger (including FIFO at FE board).
  - Zero suppression (just start considering).
  - Interface to Belle2Link.
    - Discussion with DAQ group will be done.
- Test board production within this JFY.
What we want…

• We would like to design a new board (merger) soon.
  ✓ Components on the merger board.
    ➢ FPGA (Virtex 5), optical connector …..
    ➢ Copy-and-paste from CDC readout board is fine?

• Specification for the readout signals.
  ✓ How to pass our hitdata to Belle2Link interface (inside FPGA).
  ✓ Lists of ports (signal lines, flag, clocks etc.)

• Slow control (parameter setting).
  ✓ How to receive/send parameter (or read-back values) from
    (to) Belle2Link interface.
  ✓ Lists of ports (signal lines, flag, clocks etc.)
  ✓ A-RICH FE parameters.: 
    \[(17 \times 144 + 26 \times 4 + 50?) \times 4? \sim 10^4 \text{ bits} / \text{Belle2Link}.\]
Backup
• SA01 (12ch) has been used for the beam test, HAPD measurement.
  ✓ No major problem (minor problem : gain too high).
  ✓ Only 12ch, not compact.
• SA02 (36ch) is tested.
  ✓ LTCC package is developed.
  ✓ No system yet to read out one entire HAPD.
  ✓ Now producing additional ~90 SA02 with LTCC packages.
• Development of SA03 (36ch) has just started.
  ✓ Shorter shaping time (to deal with neutron irradiation).
  ➢ Minimum 250ns peaking time (SA01/02) → 125ns.
  ✓ Production schedule : 2011- in earliest case,
  ➢ depends on the result of the HAPD neutron test and prototype FE board.
Front-end Board

1st version of FPGA logic is ready, but not tested.

parameter

hitdata

FPGA

SA02

SiTCP Wrapper
(WRAP_SiTCP_GMII_XC6S_32K)

tmp100

pmt_ad5235

init

selctl2

prmset2

tcpsender

hdrs144

trigctl

rbcp_sa02

tmp. monitor

Vth, testpulse

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Zero Suppression

Zero suppression at Merger

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<th>Channel</th>
<th>143</th>
<th>142</th>
<th>141</th>
<th>140</th>
<th>139</th>
<th>138</th>
<th>137</th>
<th>136</th>
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</table>

- Main purpose is to reduce the load at COPPER.
- Effective only when hit occupancy is low (e.g. <10%).
  - May not always be effective, but worth doing only for HAPDs with few hits.
- Naive logic takes 144 (×4) clocks : 2.2 (×4) µs latency.
  - How fast the data must be ready at L1 buffer after L1 trigger?
Zero Suppression

Faster logic?

channel

100011110010 (143)
100011010100 (141)
100010010010 (137)

1 + 1
2 + 2
4 + 4
8 + 8

~ 10 clocks
Zero Suppression

Unfortunately, this seems to be difficult in terms of resources.

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<td>12+12</td>
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<td>18+18</td>
<td>15173</td>
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<td>36+36</td>
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</table>

LUT = Look Up Table

c.f.) XC6SLX45 : 27288 LUTs
      XC6SLX150: 92152 LUTs
      XC6VLX760: 474240 LUTs

• Not OK
• Some latency @ zero suppression.
Schedule shown at the previous B2GM

Schedule

SA02 board

SA02 test board

Prototype Flame
Summary and Plan

• We will have additional 90 SA02 soon (enough for 10-20 HAPDs).
• SA02 board
  ✓ Still waiting for production. Logic is prepared.
  ✓ Test will be in Dec-Jan (?).
• Merger
  ✓ Just start considering the design.
  ✓ Need discussion with DAQ people for interface.
  ✓ Prototype module.
• Plan
  ✓ Beam test around April?
  ✓ Need to finish the test (debug) of SA02 board in Jan., and produce a few more boards.
SiTCP

![SiTCP Diagram]

- Ethernet
- Ethernet PHY
- MII
- FPGA
- TCP FIFO I/F
- RBCP
- Remote Bus Control Protocol
- User Logic

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Threshold Scan

Threshold Scan for SHP107 \((5 \times 10^{11})\)

Shaping time 1000 ns

\[\text{S/N} \approx 6\]

Shaping time 250 ns
読み出し用ASIC
ASIC for HAPD

4 trial productions of prototype ASICs (S01-S04) at VDEC.

- Used in the beam test.
- Successfully readout 1 p.e. signal from HAPDs.

New Prototype ASIC (SA01, SA02).

- Production at MOSIS (TSMC 0.35 μm process)
- Digital part for readout is provided with external FPGA for more flexibility to Super Belle DAQ
- More channels per chips (SA02: 36ch)