

IRS-based Readout Schedule

Key Points – 2-stage development to completion:

1. Intermediate development stage (Autumn 2013):
 - qualify single-stage amplifier (nominal PMT gain)
 - improved timebase stability & feedback
 - Prototype near-final electro-mechanical-optical configuration
2. Final system design (Winter 2013):
 - Final IRSX ASIC
 - Final SCROD (FPGA – on board stack sparsification)
 - Final opto-mechanics, cooling & cabling.

➔ Complete all testing for nominal HV operation this autumn

➔ Pre-production available for final CRT, beam test early 2014

➔ Production thereafter – operate on production modules

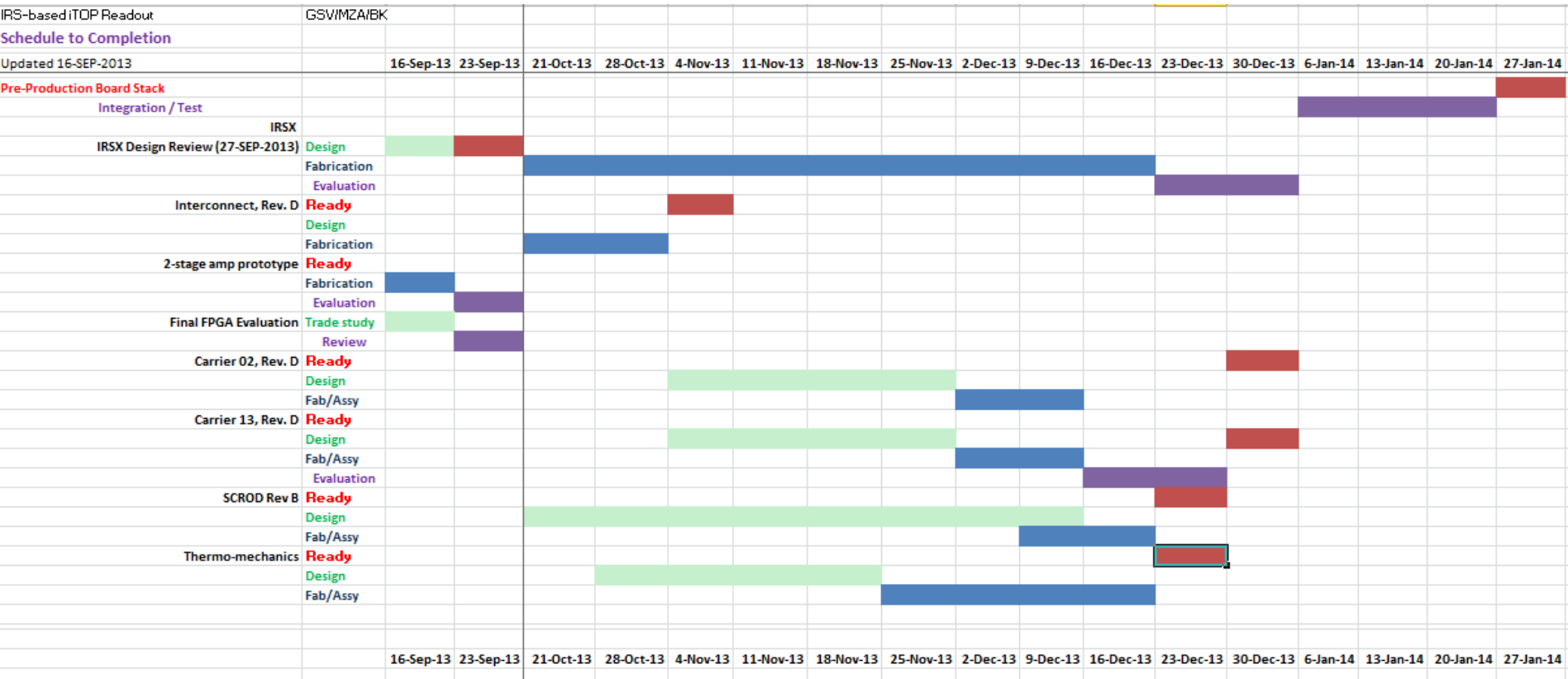
Intermediate Prototype Development

IRS-based iTOP Readout		GSV/MZA/BK									
Schedule to Completion											
Updated 16-SEP-2013			16-Sep-13	23-Sep-13	30-Sep-13	7-Oct-13	14-Oct-13	21-Oct-13	28-Oct-13	4-Nov-13	11-Nov-13
IRS3B/C-based Gen-2 Board Stack											
Integration / Test											
SCROD A3	Ready										
	Fab/Assy										
Carrier 02, Rev. C	Ready										
Carrier 13, Rev. C	Ready										
	Design										
	Fab/Assy										
Interconnect, Rev. C	Ready										
HV, Rev. A	Ready										
Front-board, Rev A0	Ready										
	Design										
	Fab/Assy										
Interposer (HV-A & Carrier Rev C <--> Front A0)	Ready										
	Design										
	Fab/Assy										
Thermo-mechanics	Ready										
	Design										
	Fab/Assy										

- **Demonstrate improvements:**

- Improved Single Stage amplifier (x4 gain, x2 risetime)
- Increased stability timebase feedback logic
- Reduced noise timebase control

Pre-Production Prototypes



- **Final Configuration:**

- 2-Stage amplifier (5×10^5 gain operation)
- Final ASIC (IRSX)
- Final SCROD with production FPGA (demonstrate can use HSLB)