IRS-based Readout Schedule

Key Points – 2-stage development to completion:

1. Intermediate development stage (Autumn 2013):
   - qualify single-stage amplifier (nominal PMT gain)
   - improved timebase stability & feedback
   - Prototype near-final electro-mechanical-optical configuration

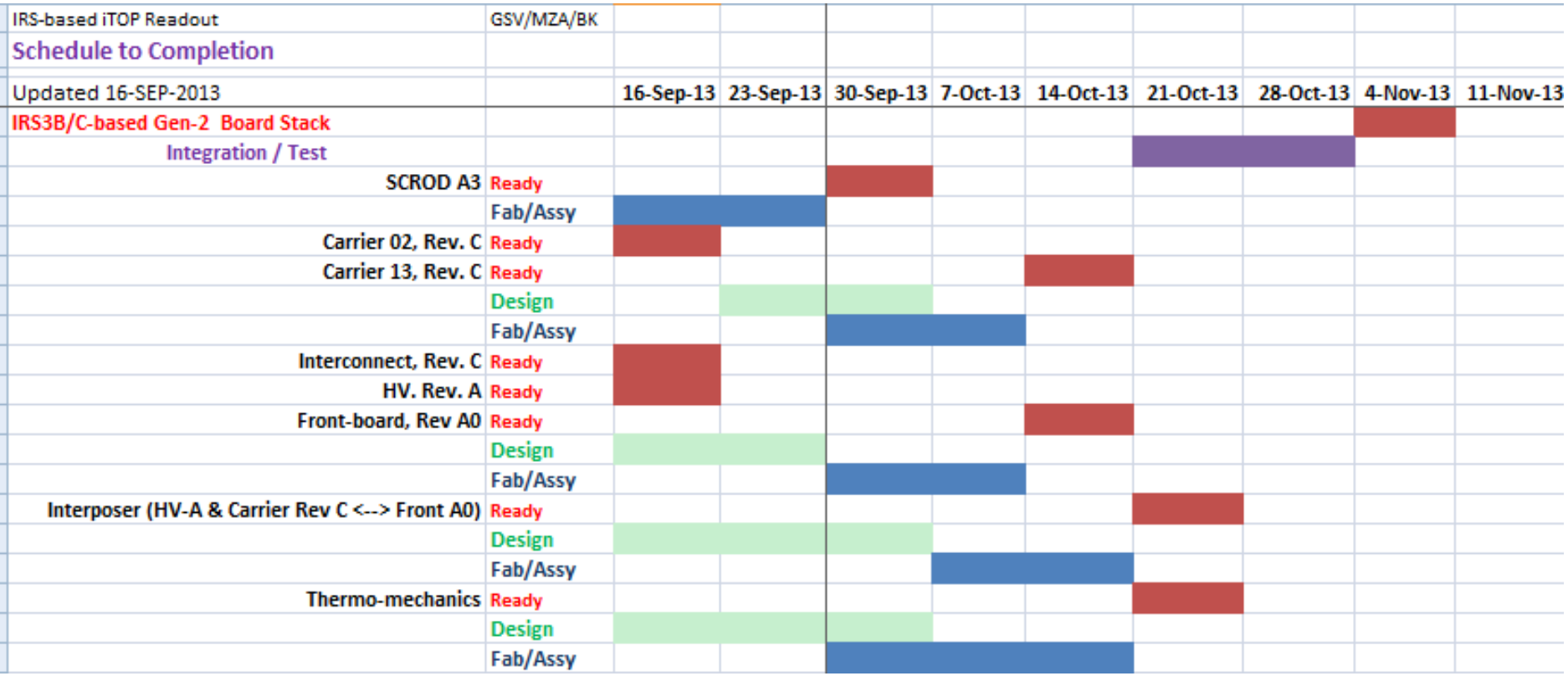
2. Final system design (Winter 2013):
   - Final IRSX ASIC
   - Final SCROD (FPGA – on board stack sparsification)
   - Final opto-mechanics, cooling & cabling.

➔ Complete all testing for nominal HV operation this autumn

➔ Pre-production available for final CRT, beam test early 2014

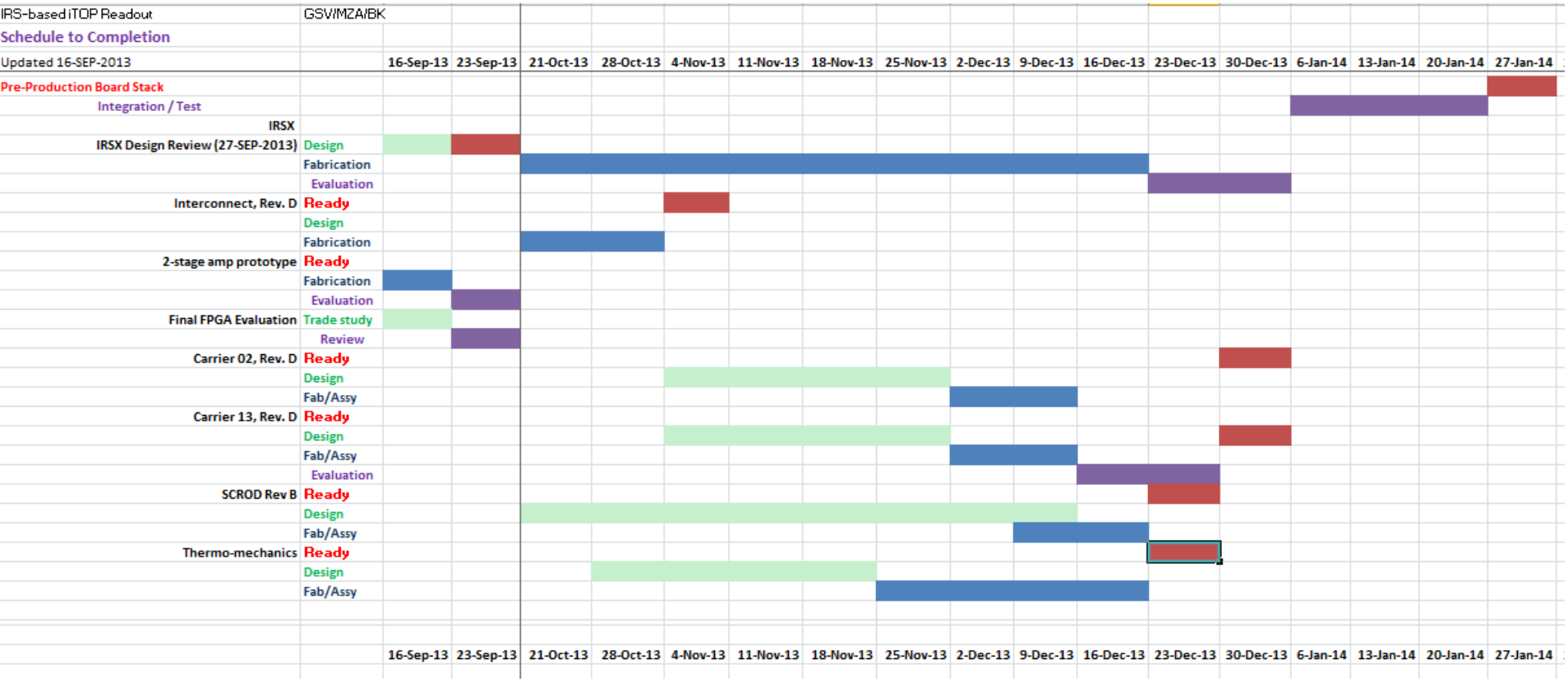
➔ Production thereafter – operate on production modules

Intermediate Prototype Development



- **<u>Demonstrate improvements:</u>**
  - Improved Single Stage amplifier (x4 gain, x2 risetime)
  - Increased stability timebase feedback logic
  - Reduced noise timebase control

Pre-Production Prototypes



- **Final Configuration:**
  - 2-Stage amplifier (5x10^5 gain operation)
  - Final ASIC (IRSX)
  - Final SCROD with production FPGA (demonstrate can use HSLB)