Electronics Updates

1. Confirming Event T0
2. Carrier02 Thermal Modeling
3. SciFi Tracker & Schedule Update (Brian/Xiaowen)
4. Carrier Board Status (Matt A)
5. All required HV boards in hand (to be tested)
6. Back-end report from PNNL

6-FEB-2013 update

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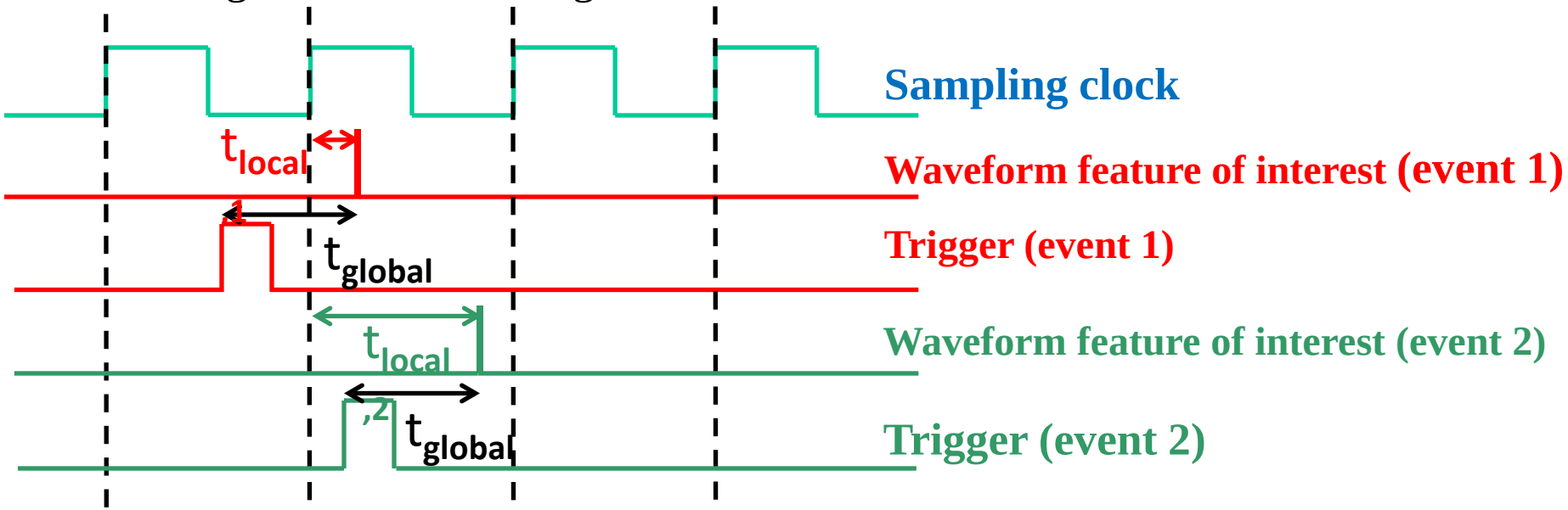
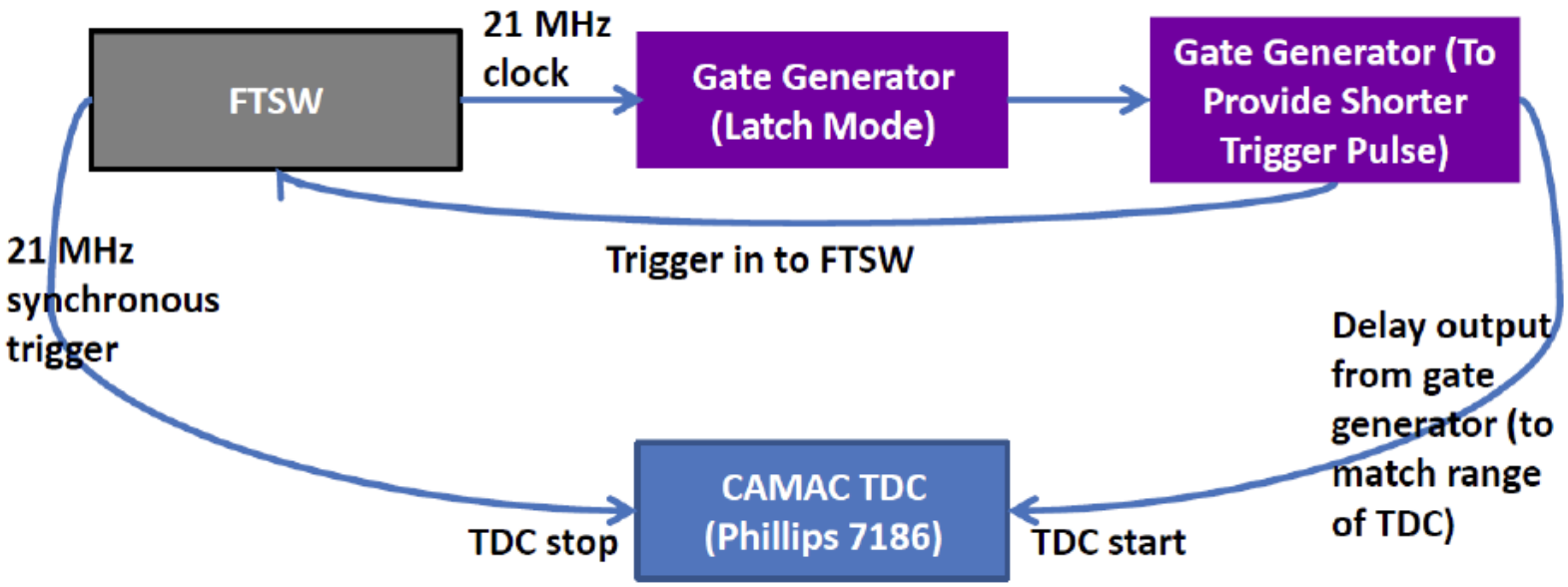
Clock Alignment w.r.t. Trigger

- Final Belle-II system:
  - The distributed clock is derived from accelerator clock ➔ waveforms are already synchronized to bunch crossings.
- Bench/cosmic/beam test systems:
  - Triggers are random relative to distributed clock ➔ we need a way to align waveforms to a global timebase.



➔ **Two events with same time relative to trigger (t_{global}) have different timing within a waveform (t_{local}).**

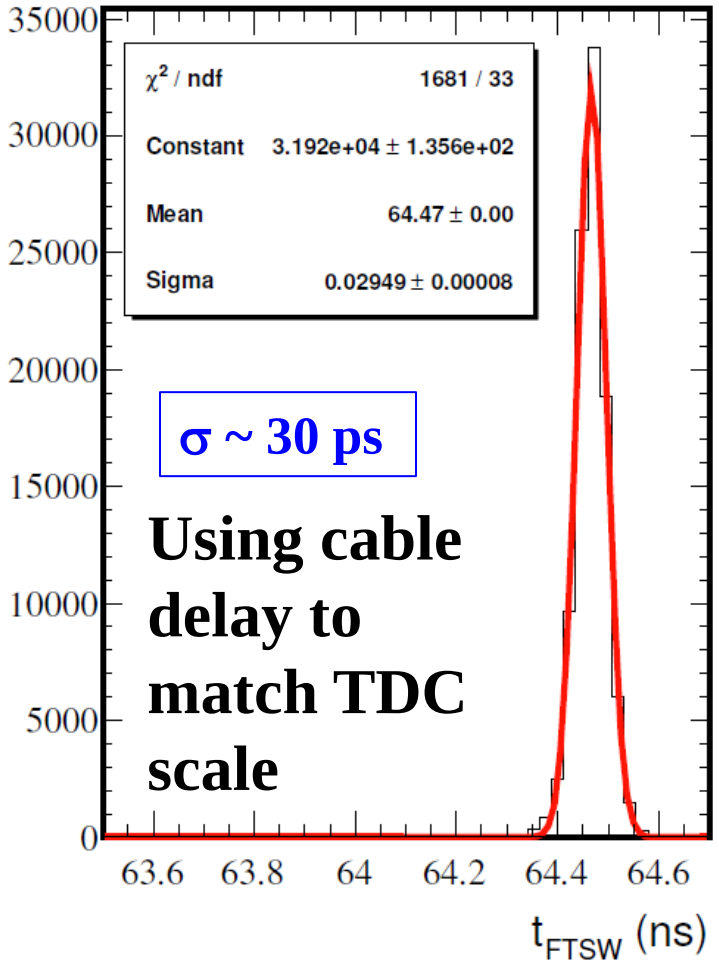
Clock/Trigger Phase Resolution

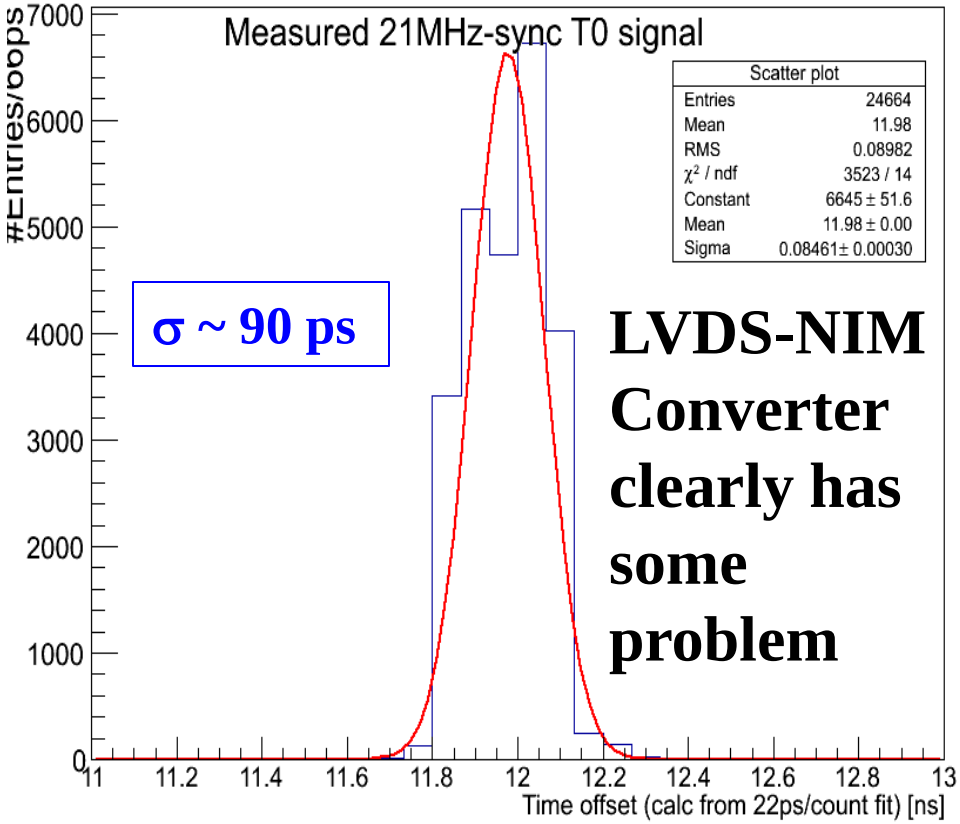


- Resolution of phase measurements directly impacts all bench/cosmic/beam results, **so it is important to know limitations**.
- Evaluated clock/trigger phase resolution by triggering based on 21 MHz clock (compared with February 2012 measurement).

  ➔ Clock phase should always be the same relative to the trigger in this configuration.

Clock/Trigger Phase Resolution

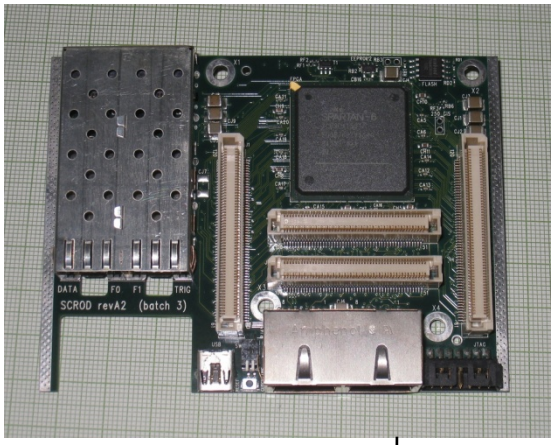




- Left is previous (Hawaii), Right is new (Fuji) w/ COPPER readout of CAMAC

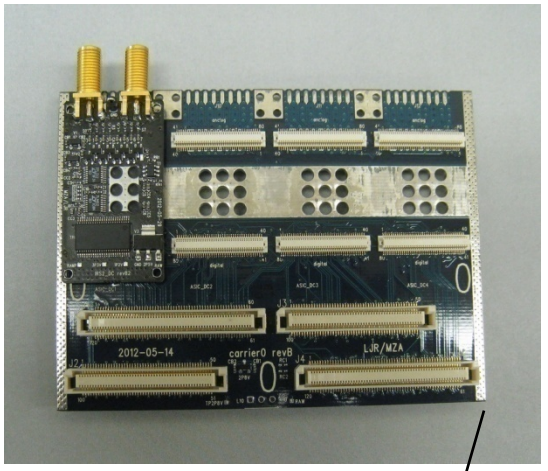
Reminder: Rev. A2 “board stack”

new
PCB
designs

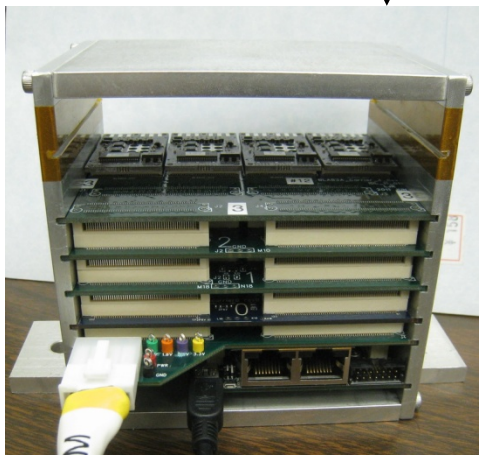


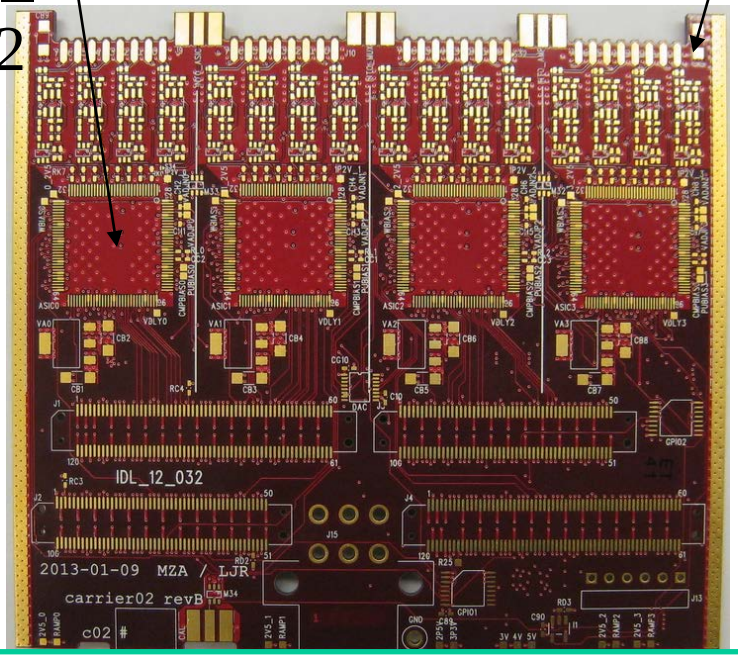
SCROD
revA2

IRS2_DC
revB2



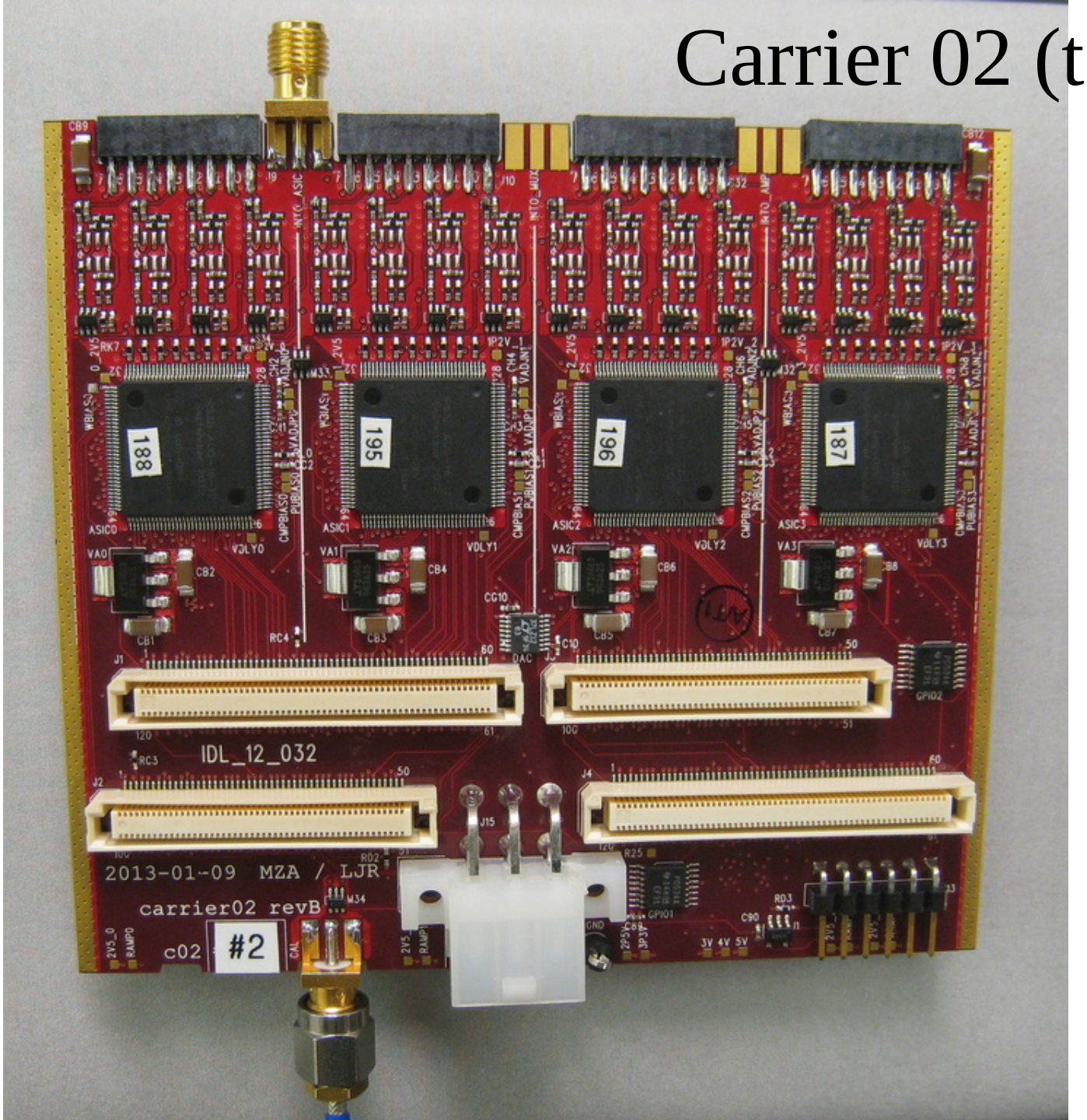
carrier0 revB



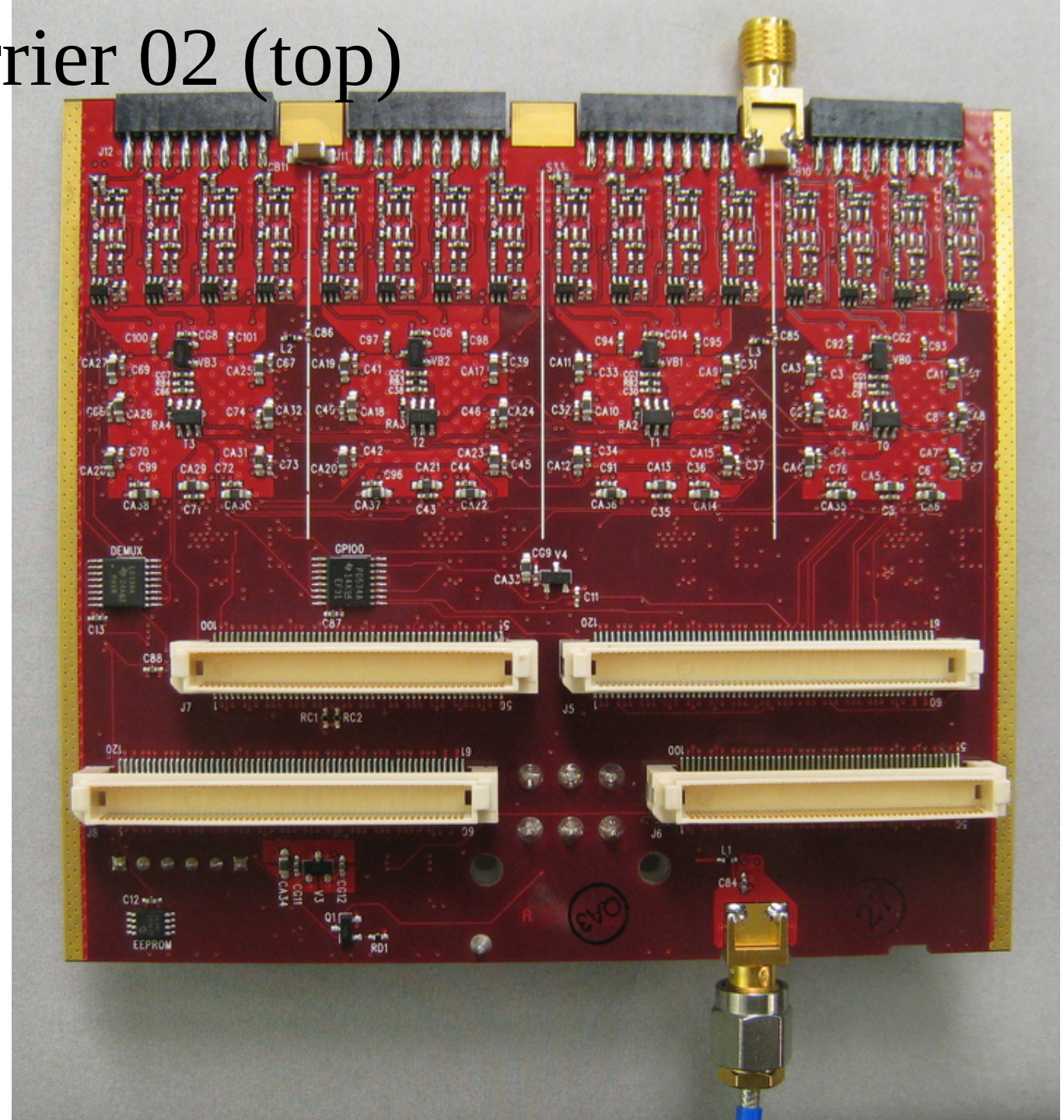


- **Removed ASIC Daughtercards, added amplifiers on carrier**

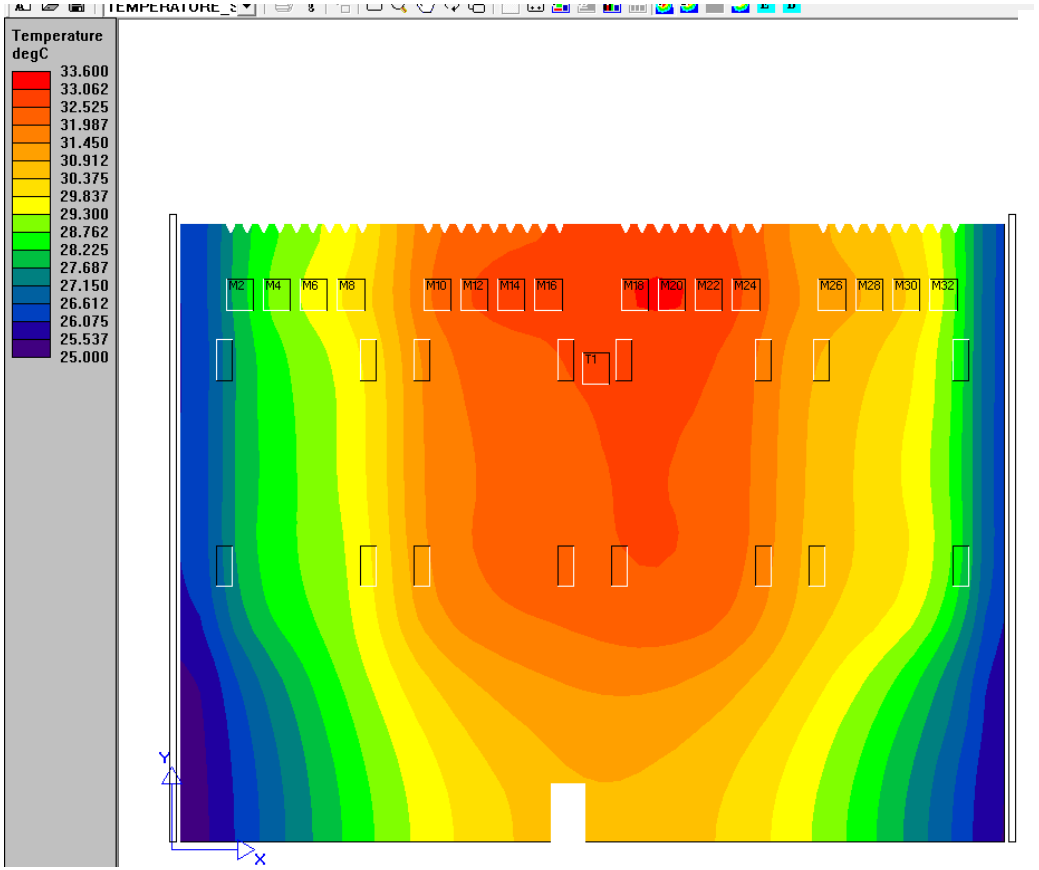
Carrier 02 (top)



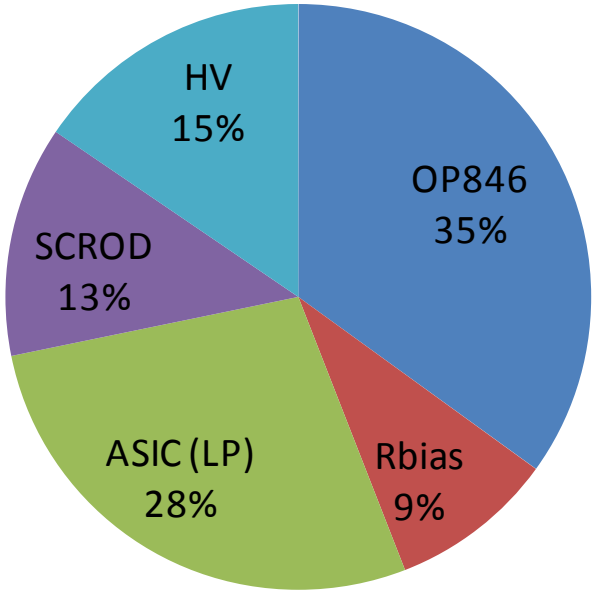
Carrier 02 (top)



Previous (initial) Thermal Simulations



iTOP Power (88W/bar box)

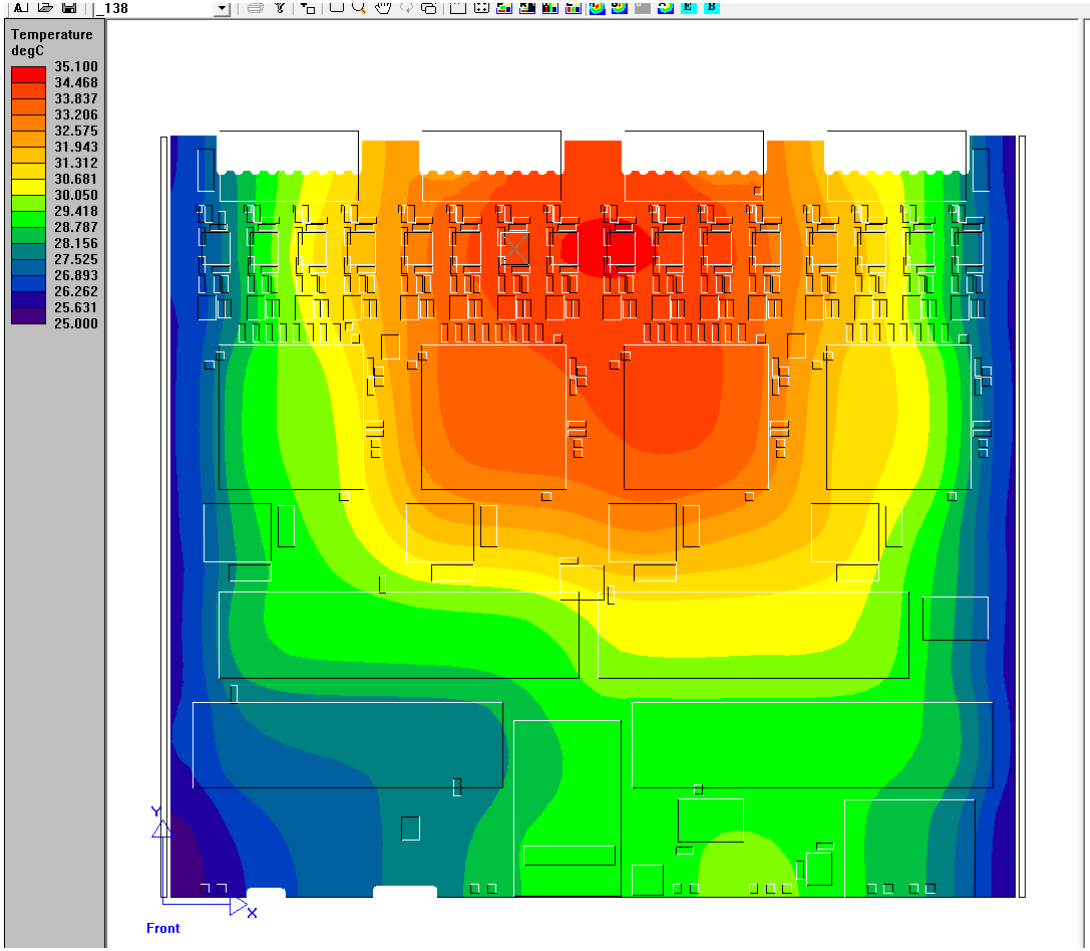


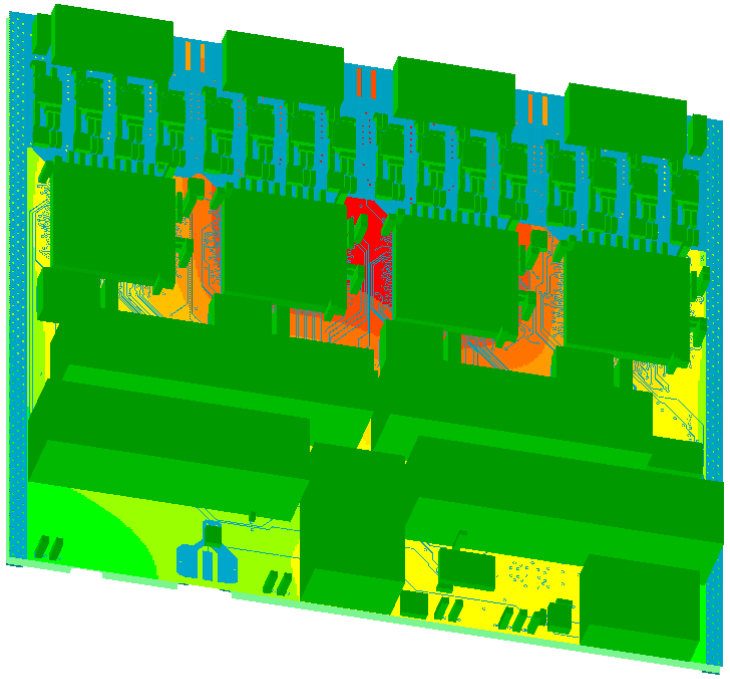
OP846	**OP846**	30.7W
	Rbias	8W
	ASIC (LP)	24.3W
	SCROD	11.2W
	HV	13.6W
Total		88W

- No air flow (without good side coupling >100 C!)
- Aluminum sidewalls held @ 25C with 0.4C/W coupling
- Can add refinements (tool is very powerful)

(22W/board stack)

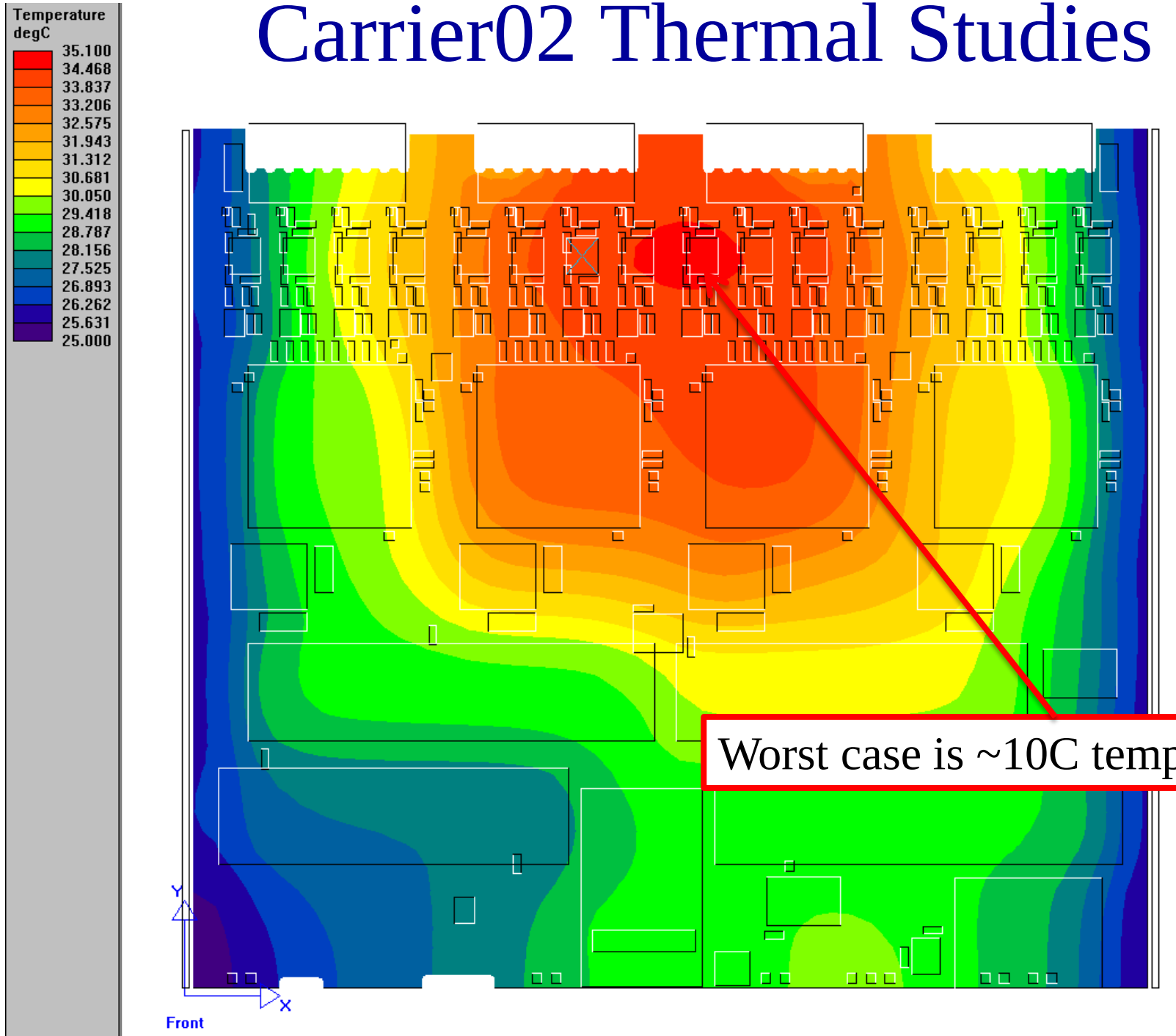
Carrier02 Thermal Studies



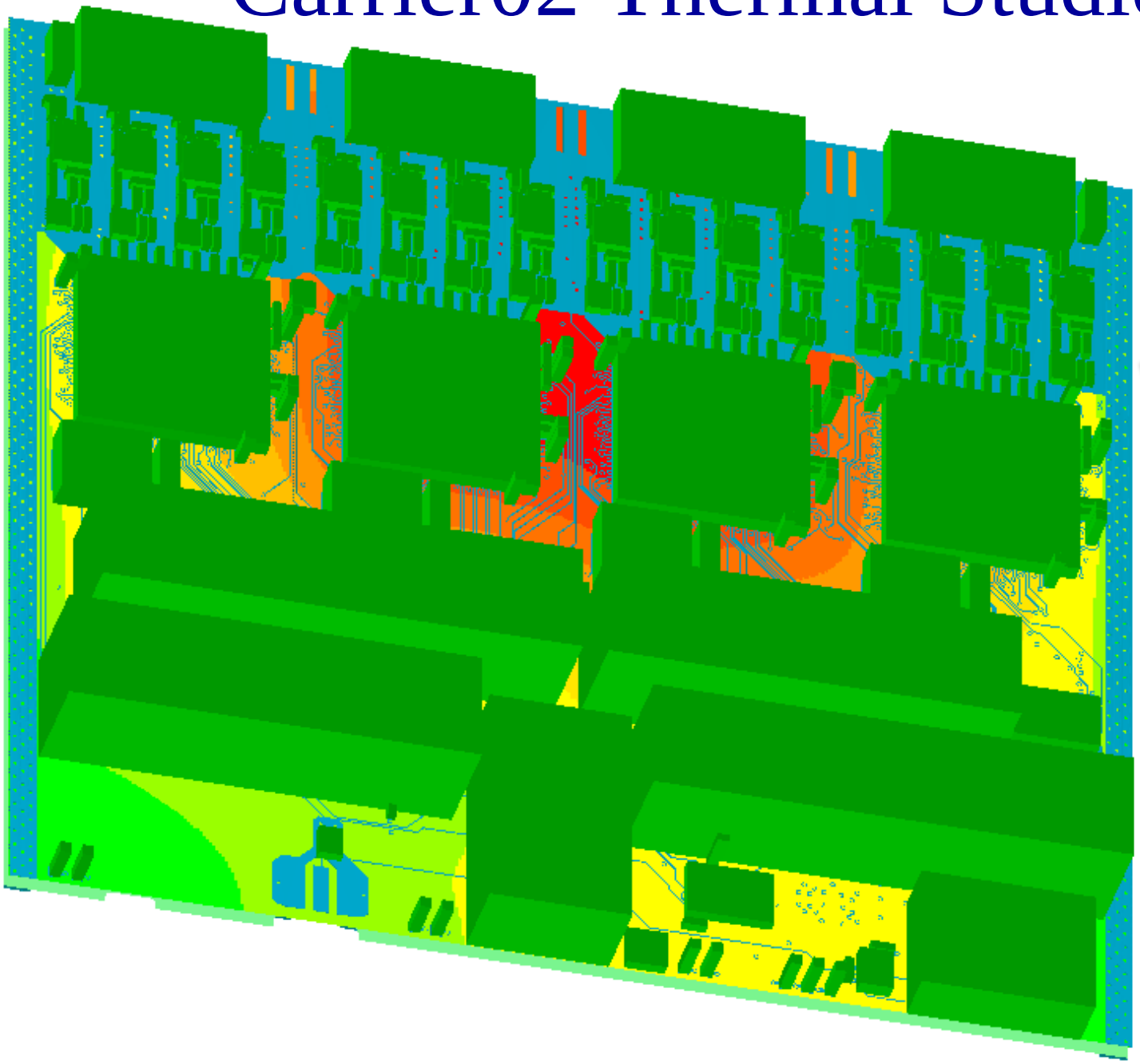


- No air flow
- Brass sidewalls held @ 25C with 1C/W coupling (calc shows 0.4, but coupling ineff.)
- Stitching vias to ground planes really help
- Measurements during running of IRS3B (0.725W), 1W assumed here
- Higher power OPA 847 (90mW ea) assumed [OP 846 is 60mW ea.]

Carrier02 Thermal Studies



Carrier02 Thermal Studies



Includes all power plane stitching vias, but not edge plating

IRS3B Testing/Next Steps

• Modify version 2 firmware: IRS2 → IRS3B (becomes version 3 once fully incorporated)

• Evaluating timing performance with pi-Las laser & SL-10 for RCO-locked feedback (Carrier 02 very helpful)

• Optimizing biases/timing settings for 4GSa/s operation, direct evaluation of timing/addressing strobes (not properly aligned yet)