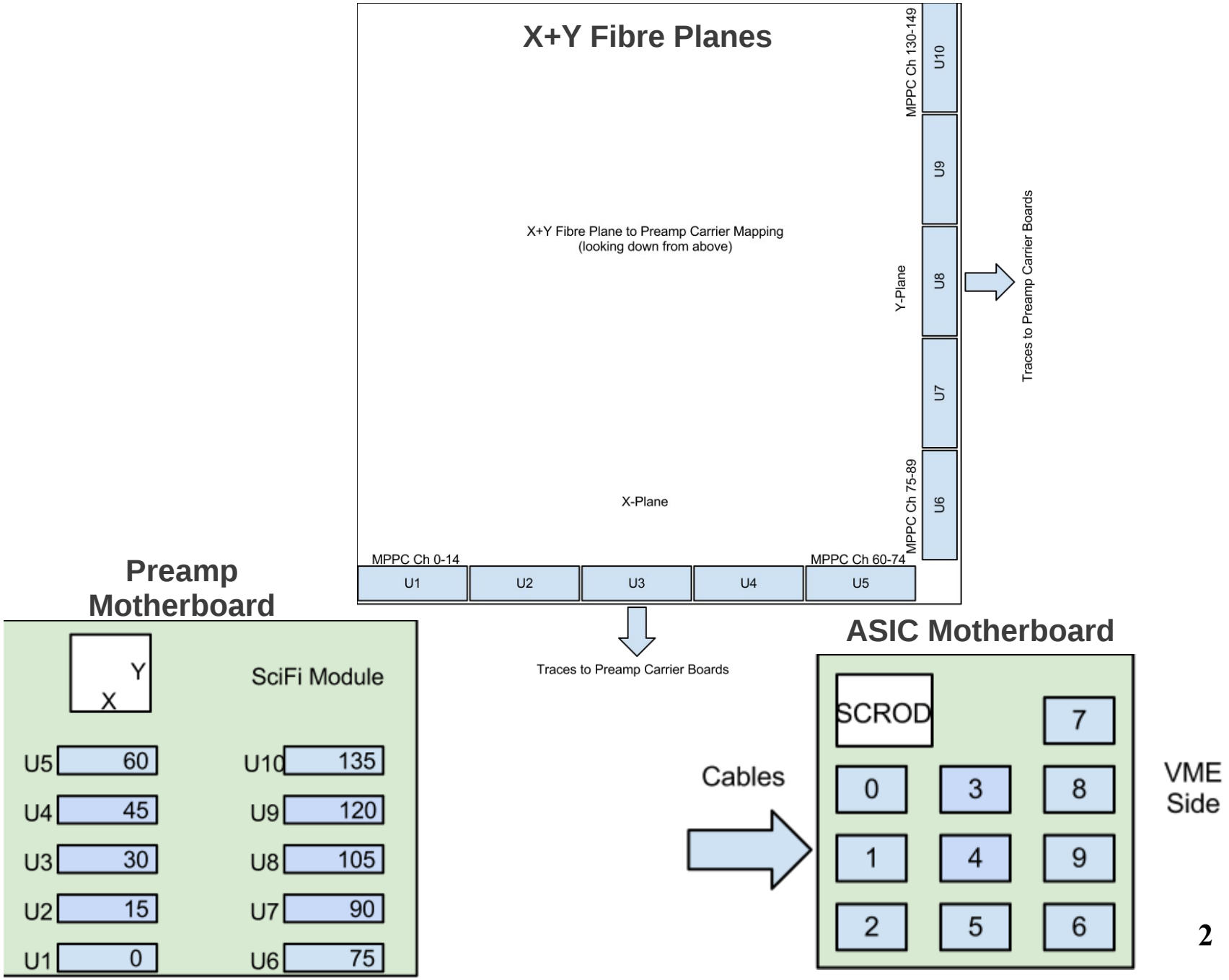
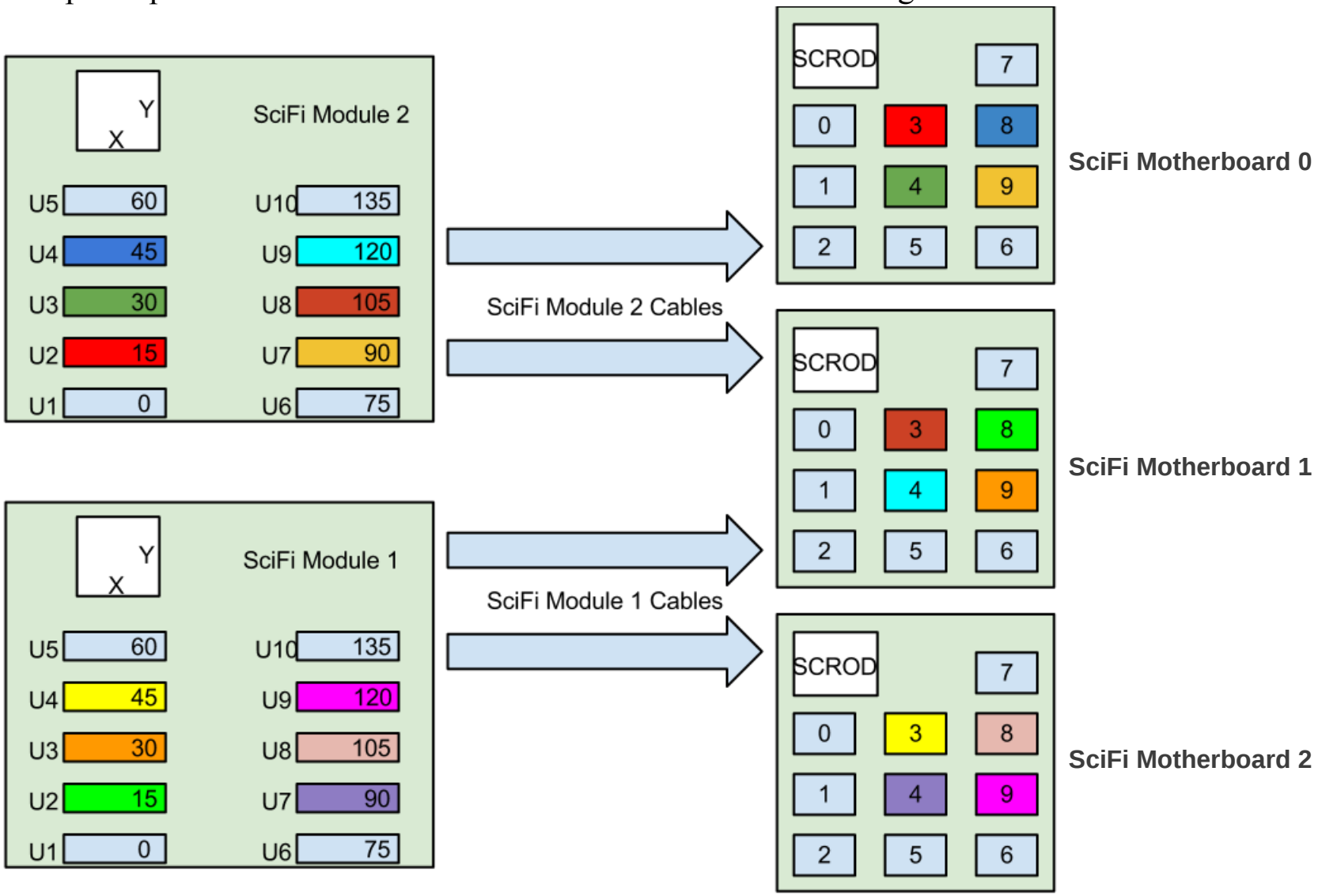
Sci-Fi Tracker Update

Feb. 28th, 2013

- Numbering schemes for various boards



- Propose only 12 ASIC carriers in system initially
  - Gets around “ASIC-DAC writing” problem
  - Connect preamps such that central region of each fibre plane are instrumented
  - Basic cabling diagram shown below, also shows numbering of preamp and ASIC carriers on motherboard
  - 12-preamp carriers are connected to 3 SciFi motherboards holding 4 ASIC carriers each

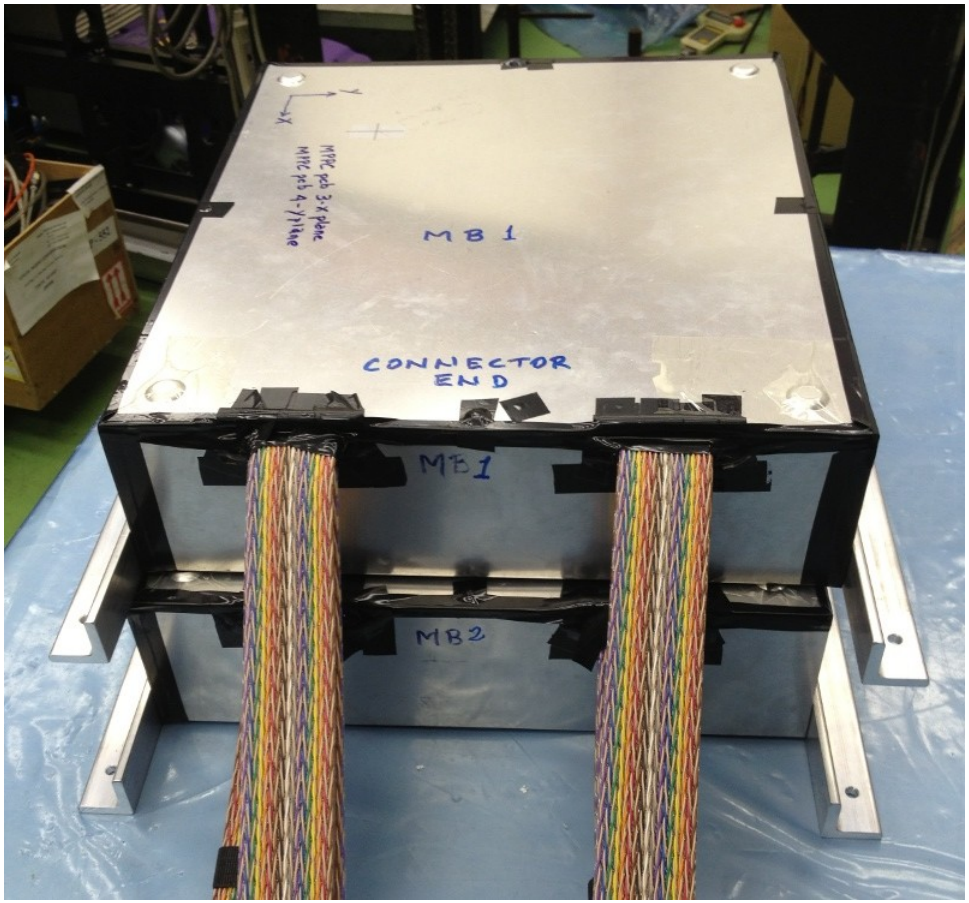


- Table summarizing 12 ASIC configuration cable mappings

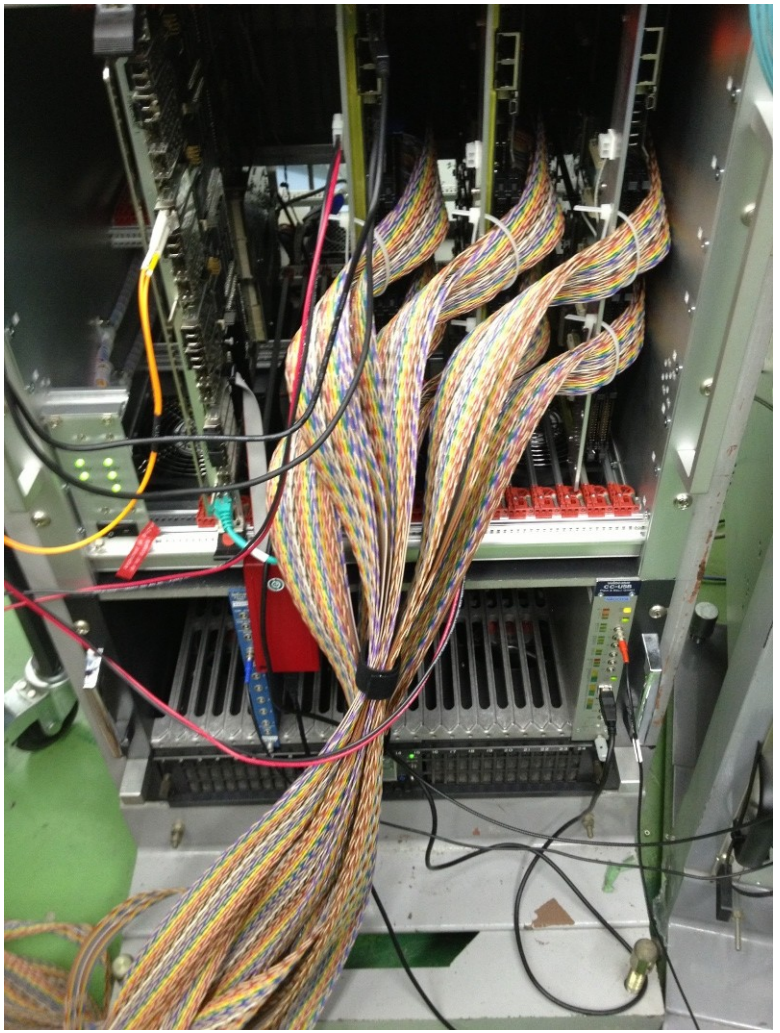
SciFi Module # (1 or 2)	Preamp Carrier # (U1-U10)	MPPC Plane (x or y)	MPPC Ch. Range (0-149)	Ribbon Cable #	SciFi Motherboard # (0,1,2)	SciFi ASIC Position # (0-9)
2	U2	x	15-29	1	0	3
2	U3	x	30-44	2	0	4
2	U4	x	45-59	5	0	8
2	U7	y	90-104	7	0	9
2	U8	y	105-119	3	1	3
2	U9	y	120-134	8	1	4
1	U2	x	15-29	6	1	8
1	U3	x	30-44	17	1	9
1	U4	x	45-59	10	2	3
1	U7	y	90-104	9	2	4
1	U8	y	105-119	13	2	8
1	U9	y	120-134	14	2	9

- Pictures of completed detectors, cabling
- We confirmed that each ASIC in the system has MPPC pulse signals on RF inputs

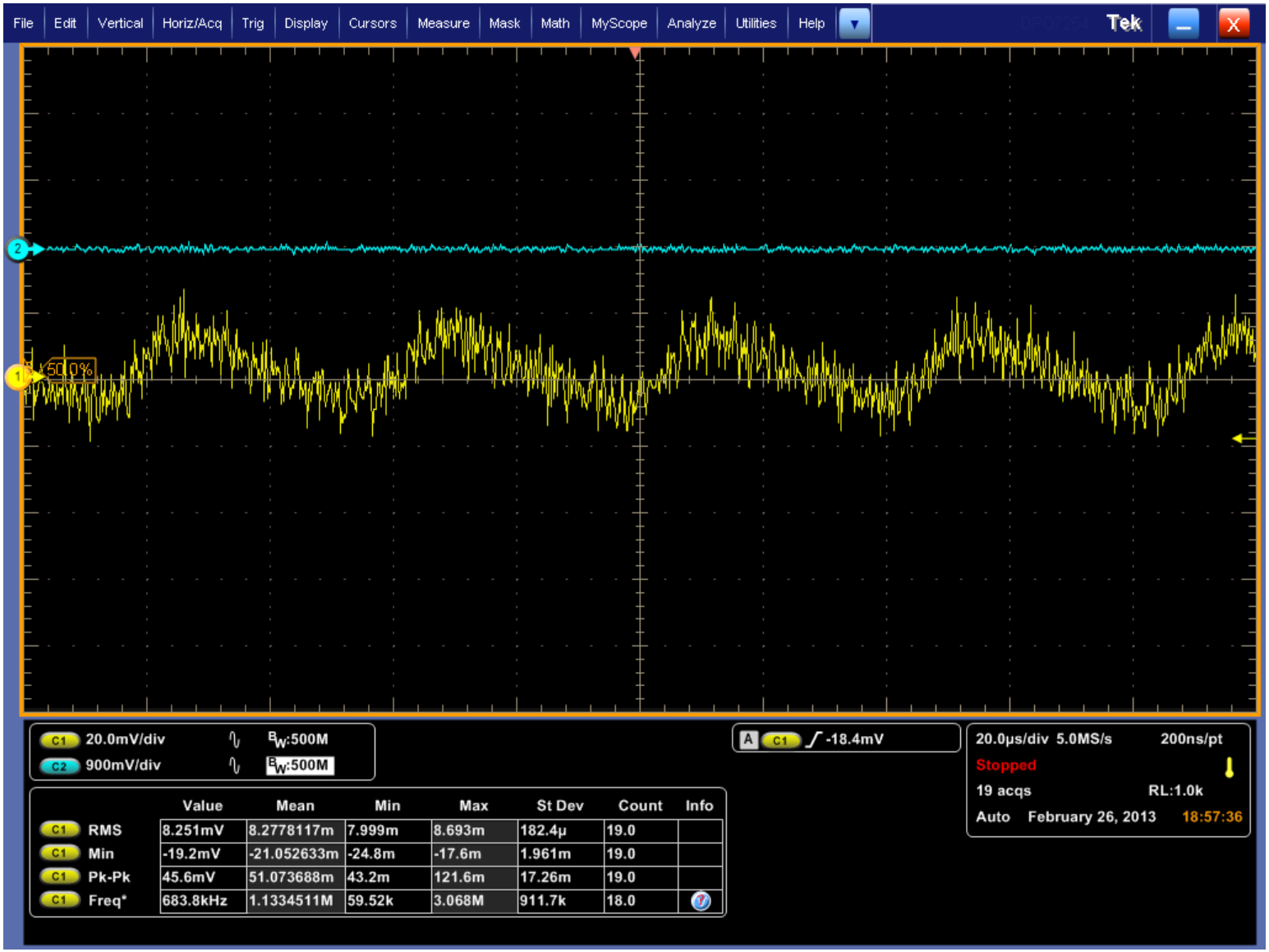
Completed, Light Tight SciFi Modules



3 SciFi Motherboards in VME Crate with Ribbon Cables

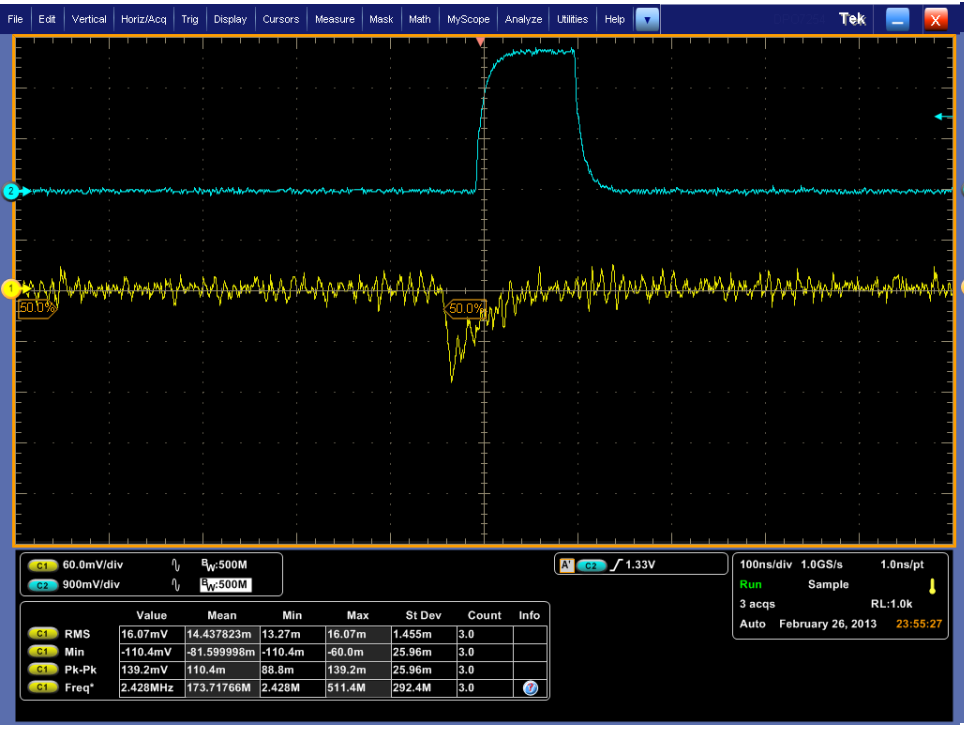


- Noisy 25kHz 40mVpp signal is still present, tests at Fuji Hall suggest it originates from preamplifiers under certain conditions, or certain preamps

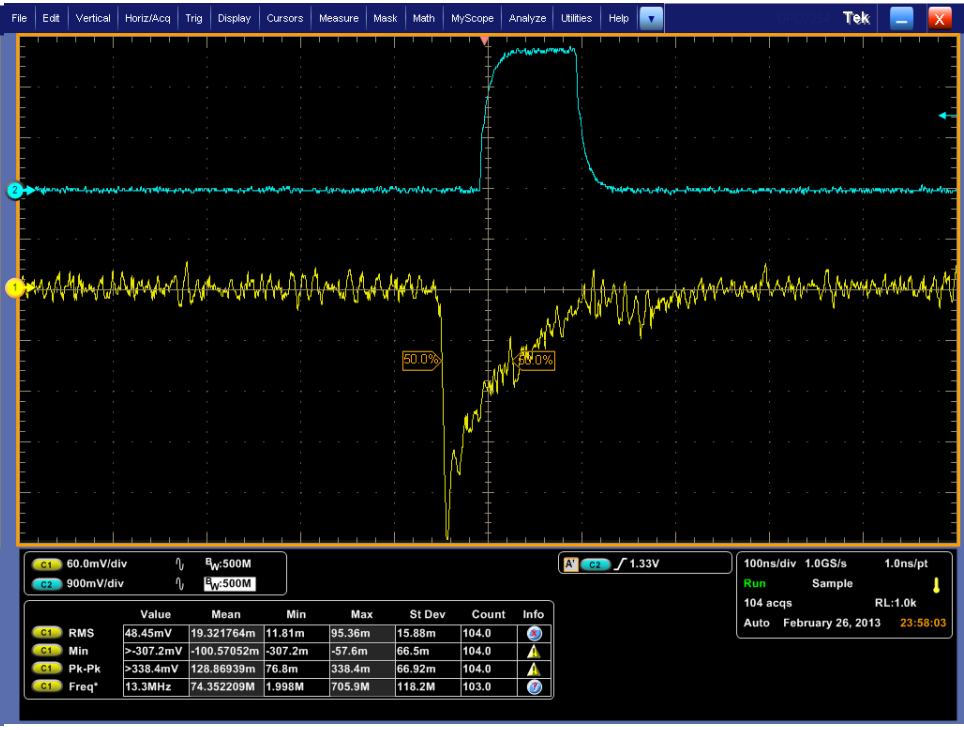


- Identified two usable DAC ranges for use with trigger thresholds
  - 0x700 – 0x7FF (~1.09V-1.24V): trigger on >60mV MPPC pulses
  - 0x600 – 0x6FF (~0.94V-1.09V): trigger on >280mV MPPC pulses
    - -note discontinuity between pulses selected by 0x6FF and 0x700 threshold DAC values is due to ASIC DAC word corruption
    - Sample of pulses obtained using 0x6FF threshold is very pure, 25kHz noise signal does not contribute
    - Propose running system at 0x6FF threshold, turn up MPPC bias such that cosmic pulses are >280mV

Typical Pulse Selected Using Trigger Threshold of 0x700

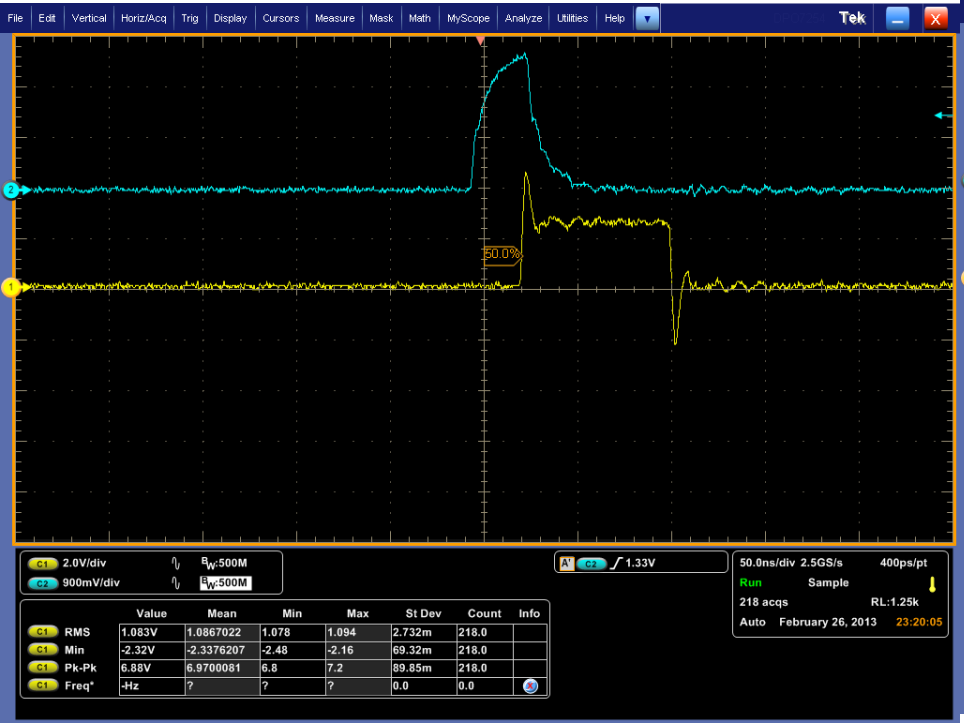


Typical Pulse Selected Using Trigger Threshold of 0x6FF



- Wbias DAC adjusted so that width of trigger pulse overlaps with period that trigger bits are being latched for both values of “TRIG_TYPE”
- Wbias = 0x3BF nicely extends through latching period, 0x600 does not

Trigger Pulse (Blue) at Wbias = 0x600 and Latching Period (Yellow)



Trigger Pulse (Blue) at Wbias = 0x3BF and Latching Period (Yellow)