Confirming Event T0
27-JAN-2013

- Verification of event Time 0
  - To be confirmed as part of any data taking
  - Verify during initial check-out
- Set-up can be used to check ROI and other preliminary performance

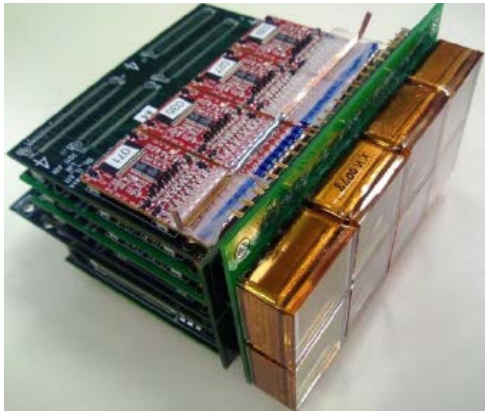
System Synchronization

While dealing with HV, firmware problems, focused on System Timing issues

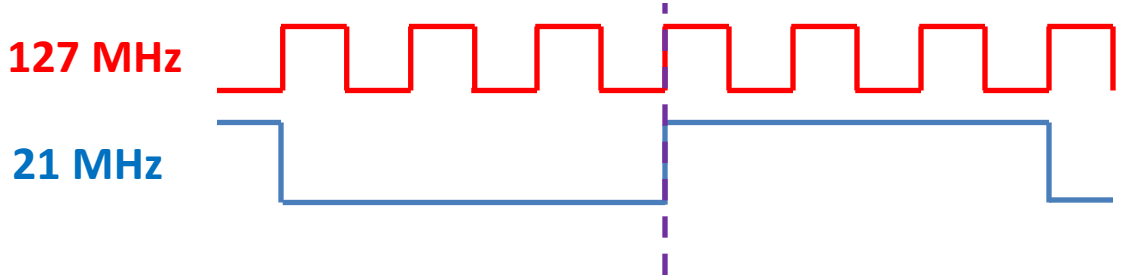
FTSW (Timing & Trigger Distribution board)

127 MHz clock

Serial data (trigger & synchronization)

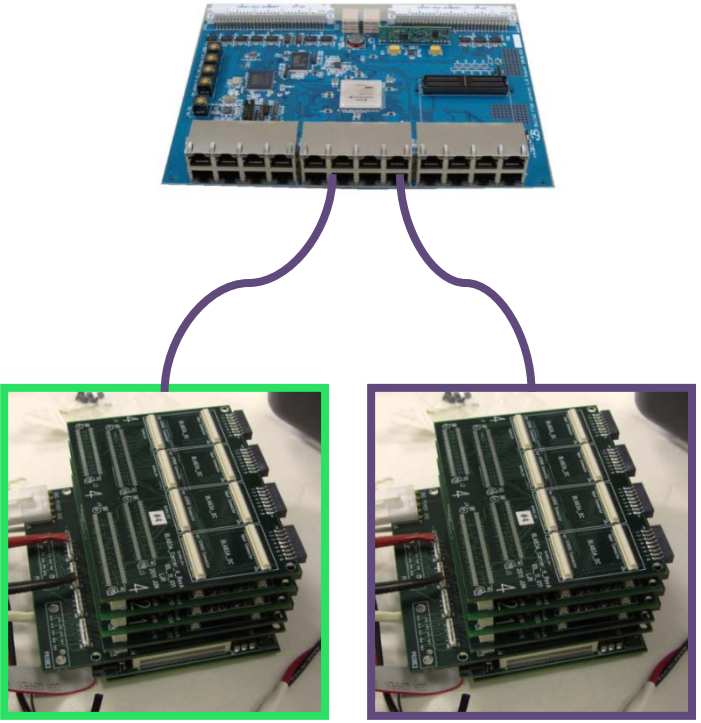


- **127 MHz clock is divided by 6 on front-end module to ~21 MHz**
  - **This corresponds to sampling rate of ~2.7 GSa/s**
  - **FPGA uses serial data stream to determine clock phase**

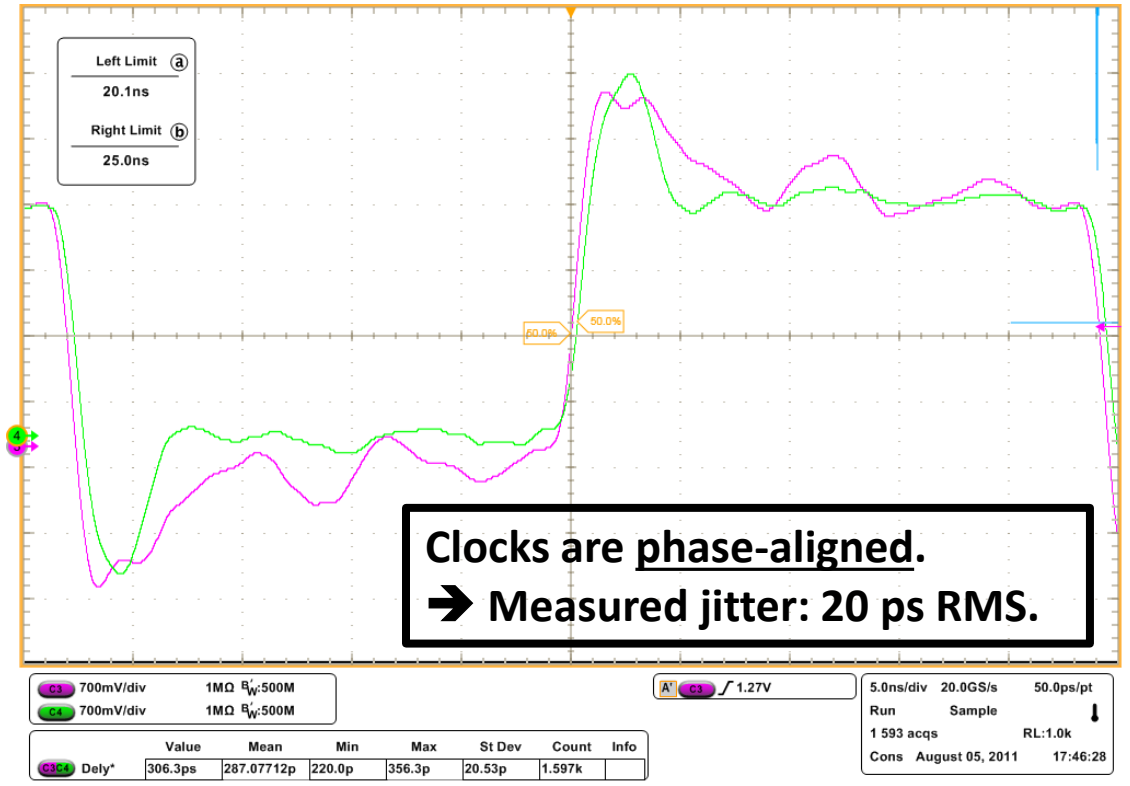


Clock Distribution Performance

- Test results performed as part of the cosmic ray test stand integration at Nagoya Univ in August 2011:

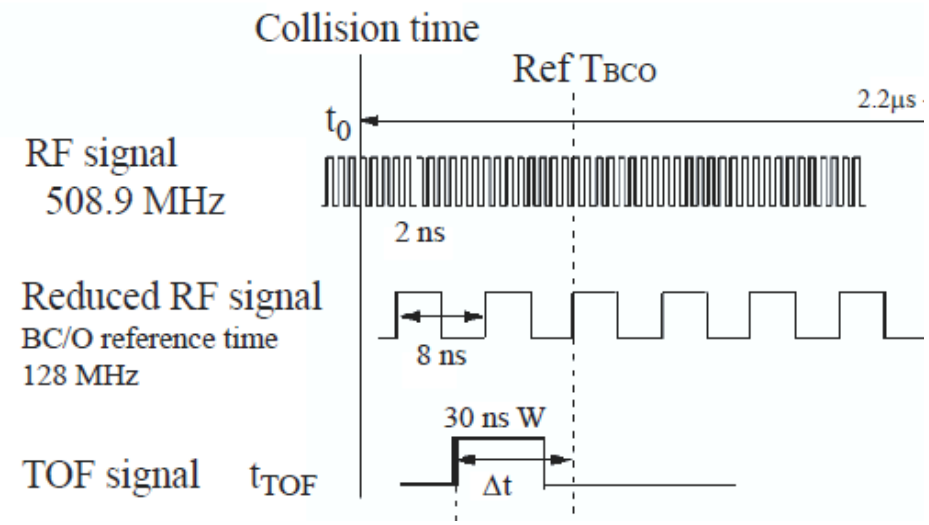


Measured phase and jitter of 21.2 MHz clock from two modules (on oscilloscope)

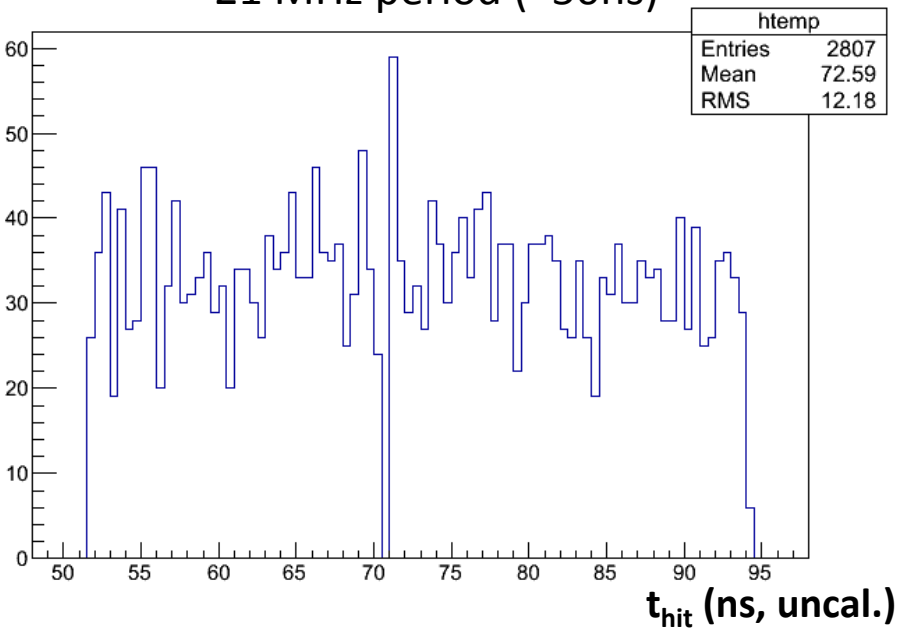


Event Timing

- At Super-KEKB the timing of signals should be **fixed** relative to trigger (system clock)
  - But it is random with respect to 21 MHz derived (Super-KEKB RF clock).
  - t_{hit} from waveform must be combined with t_{FTSW} from CAMAC TDC to align events.
  - $t_{global} = t_{hit} + t_{ftsw}$

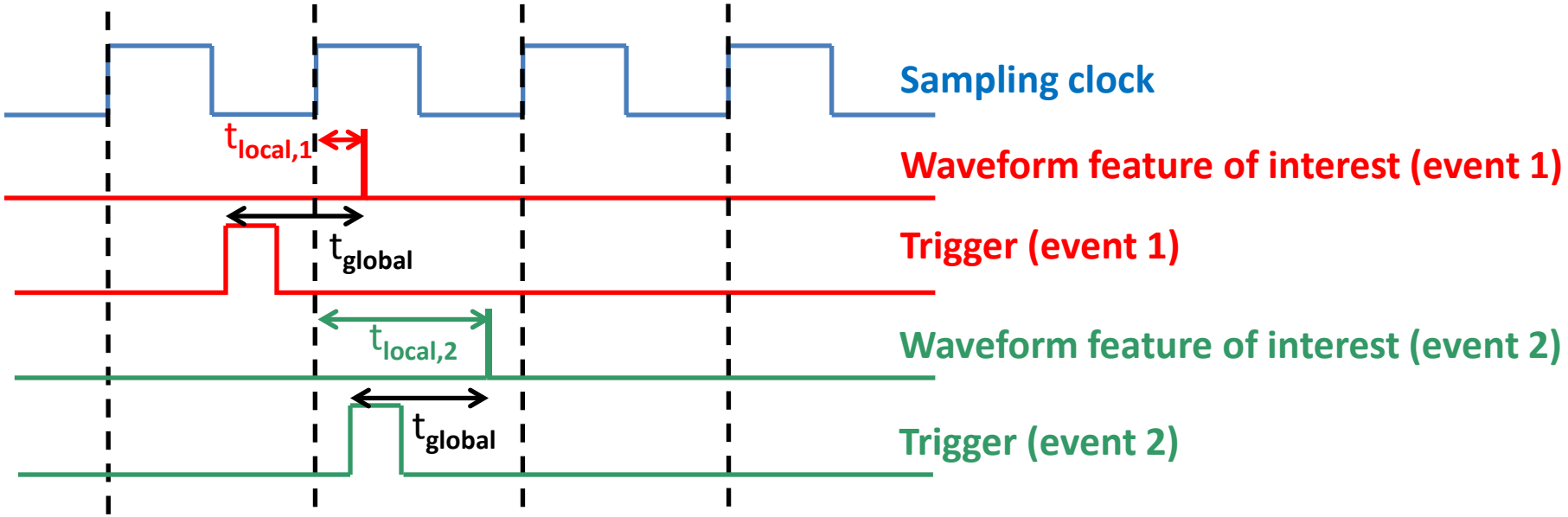


21 MHz period (~50ns)



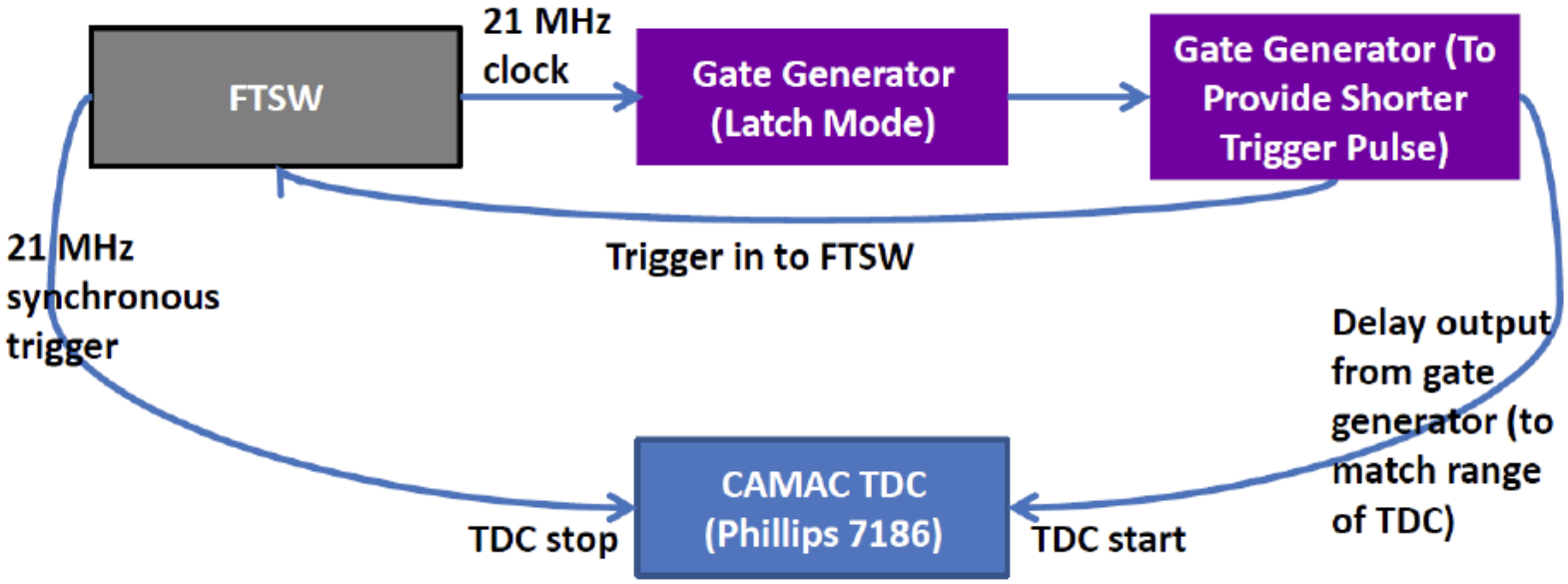
Clock Alignment w.r.t. Trigger

- Final Belle-II system:
  - The distributed clock is derived from accelerator clock ➔ waveforms are already synchronized to bunch crossings.
- Bench/cosmic/beam test systems:
  - Triggers are random relative to distributed clock ➔ we need a way to align waveforms to a global timebase.



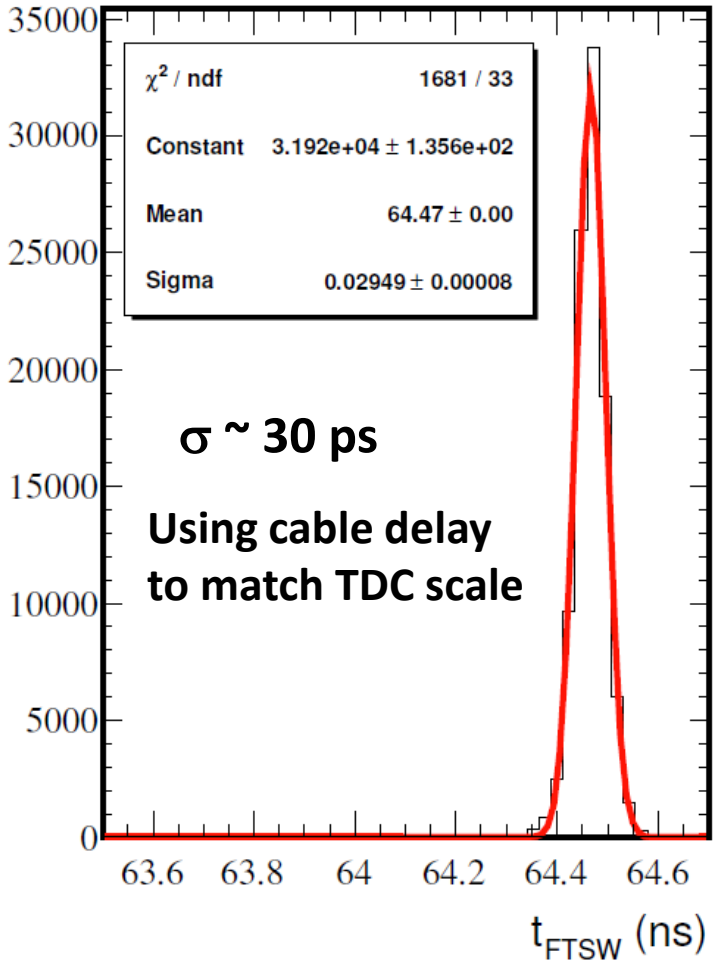
➔ **Two events with same time relative to trigger (t_{global}) have different timing within a waveform (t_{local}).**

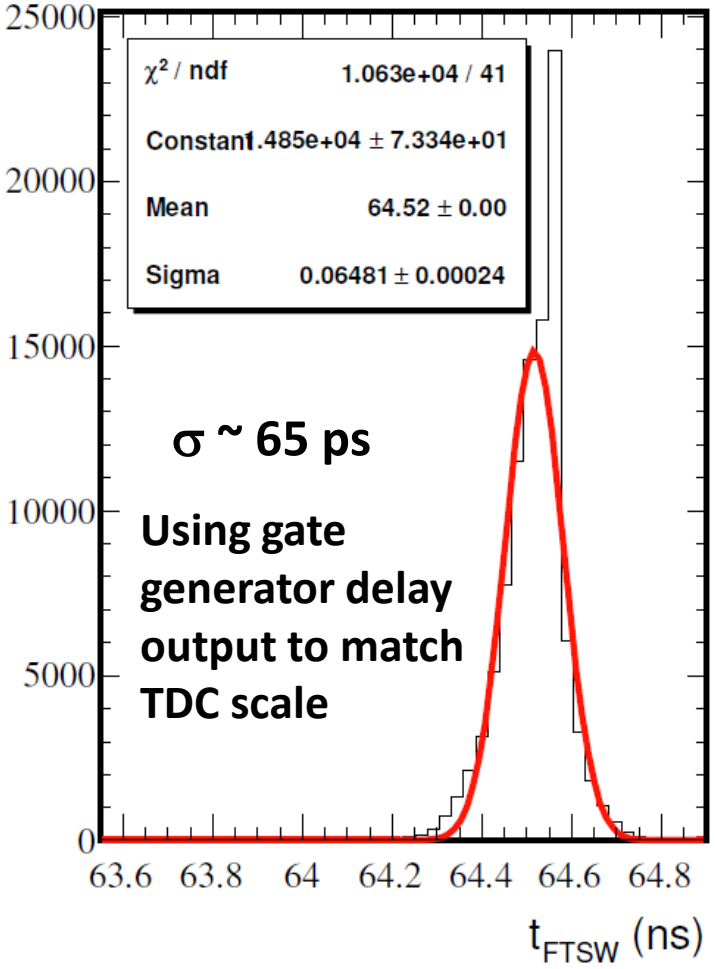
Clock/Trigger Phase Resolution



- Resolution of phase measurements directly impacts all bench/cosmic/beam results, so it is important to know limitations.
- Evaluated clock/trigger phase resolution by triggering based on 21 MHz clock (February 2012).
  - ➔ Clock phase should always be the same relative to the trigger in this configuration.

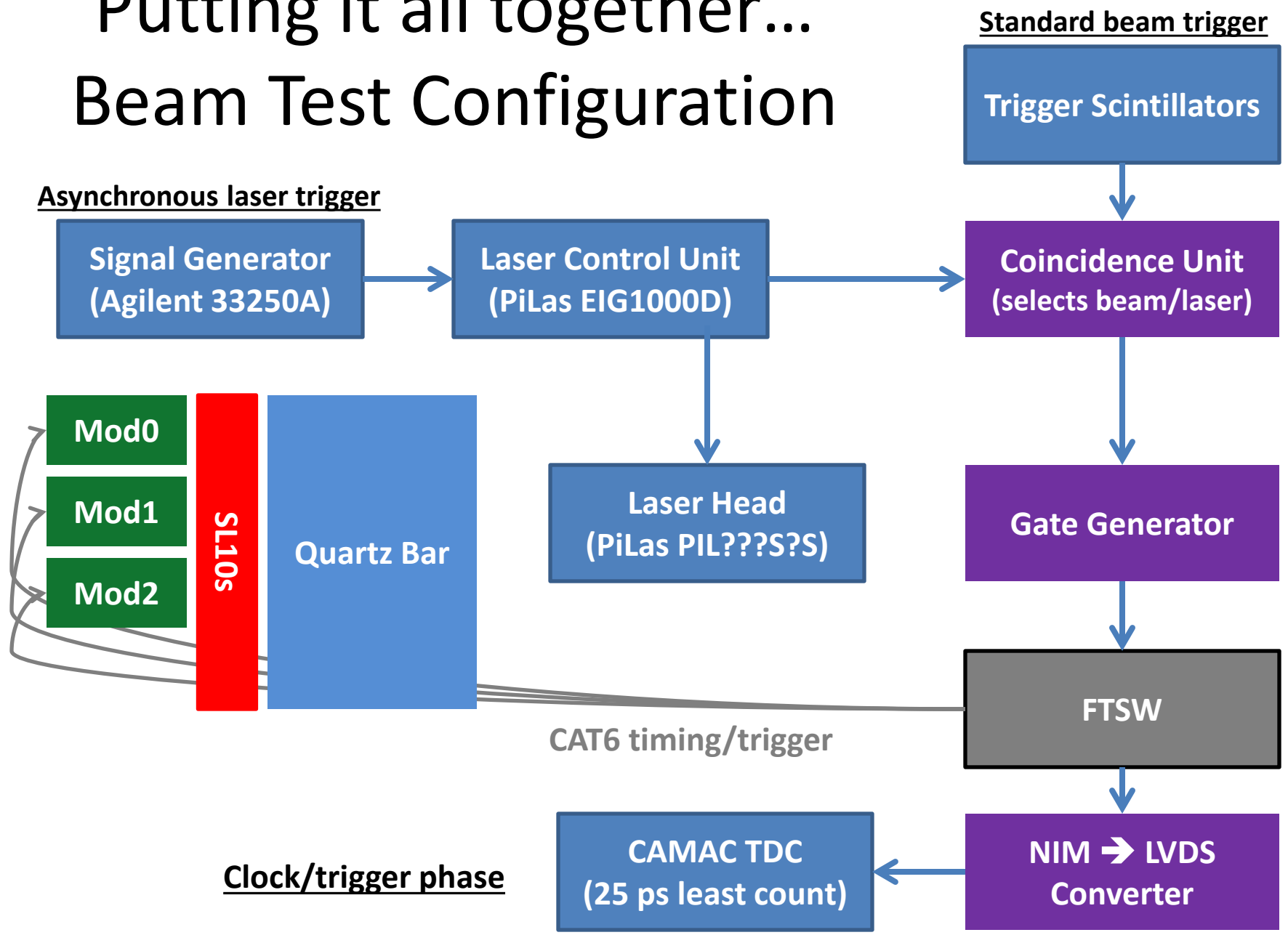
Clock/Trigger Phase Resolution





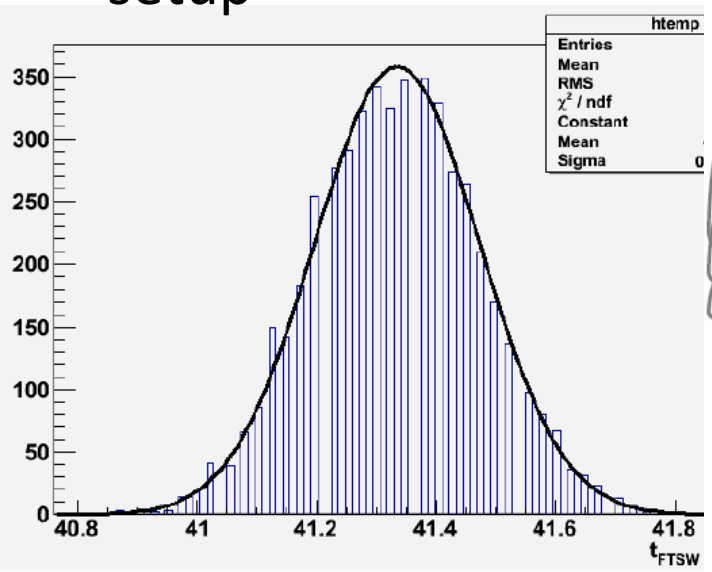
- Measurements indicate adequate performance:
  - But very sensitive to conditions.
  - Unfortunately, this was not evaluated at the 2011 Beam Test.

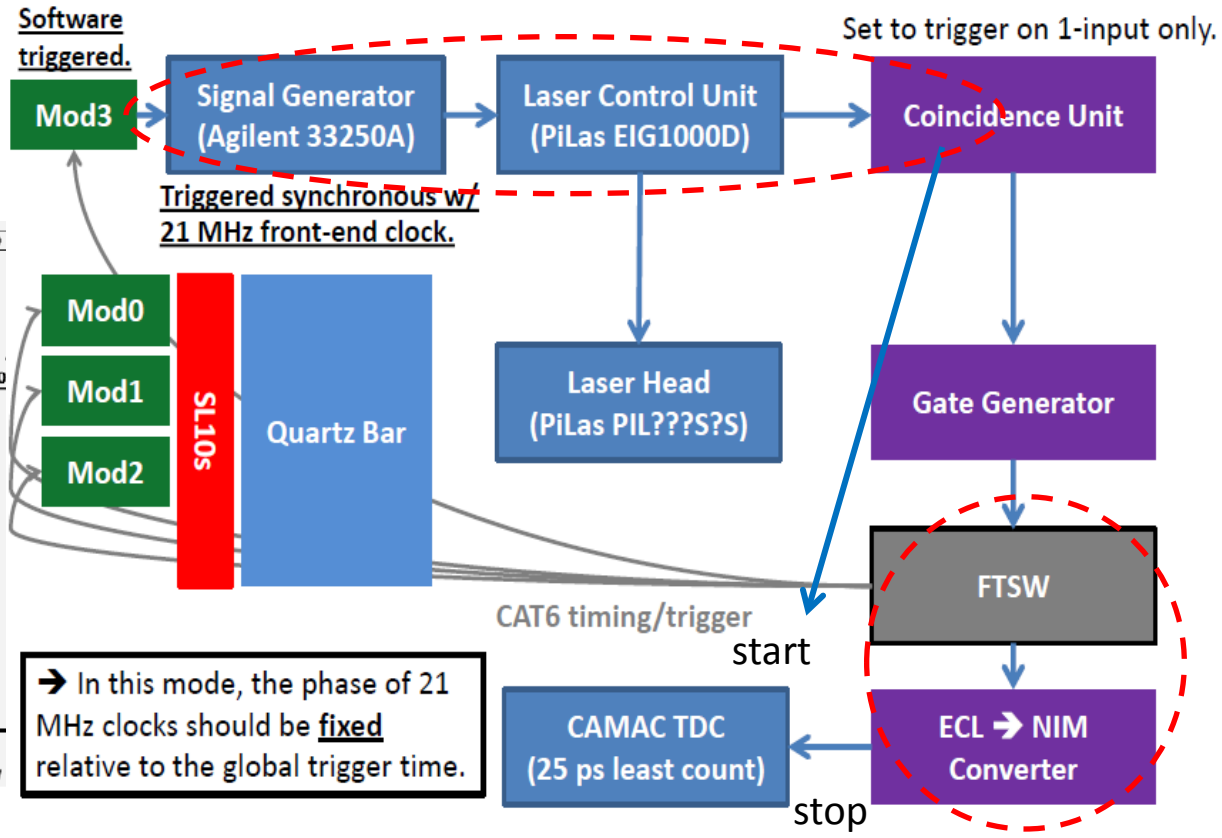
Putting it all together… Beam Test Configuration



Event time broadening

- Checked readout jitter with special laser run setup

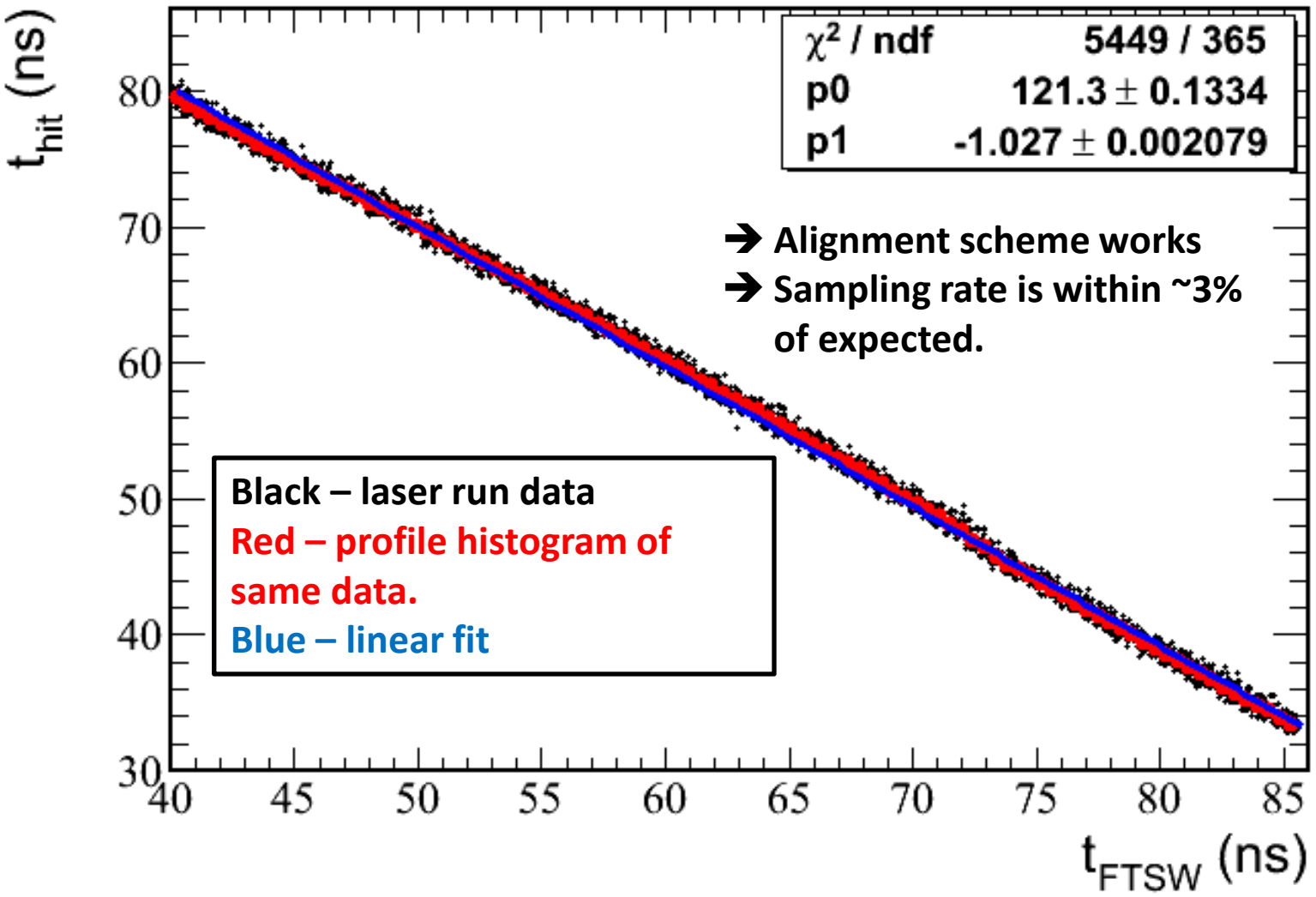




- Jitter is σ~140ps.
  - Intrinsic jitter in timing distribution? or jitter in measurement system?

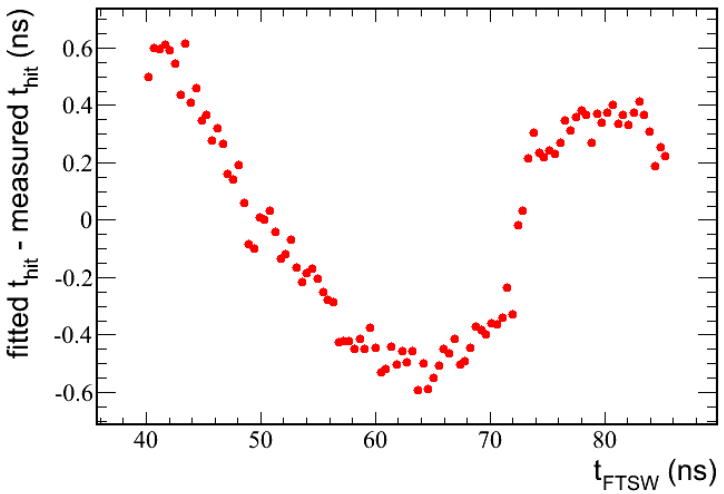
➔ Further calibration bench testing

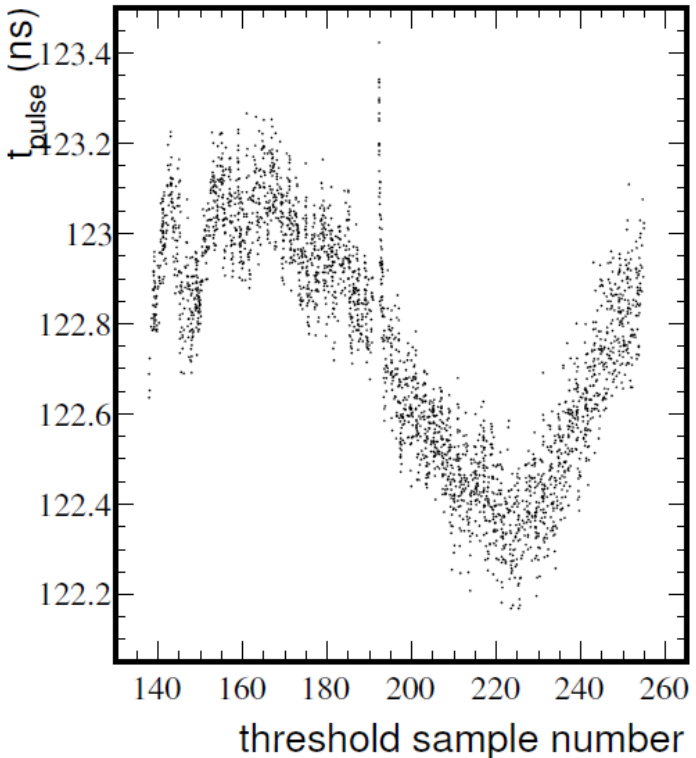
2012 Beam Test - Laser Run Results



No fine calibration applied: assumed 2.7 GSa/s for all samples; 25 ps / count for CAMAC TDC. Time extracted by software fixed threshold discrimination on waveforms.

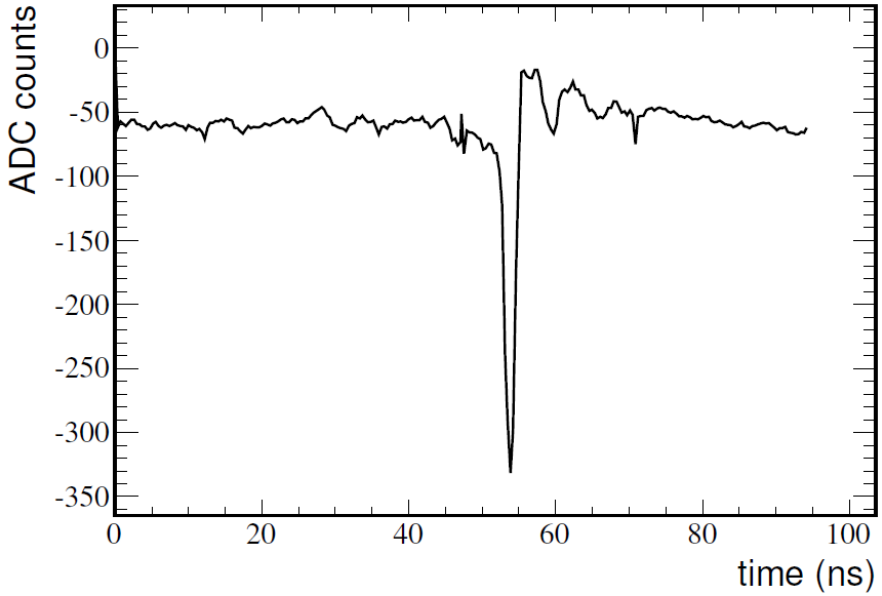
Timing Nonlinearity & Calibration





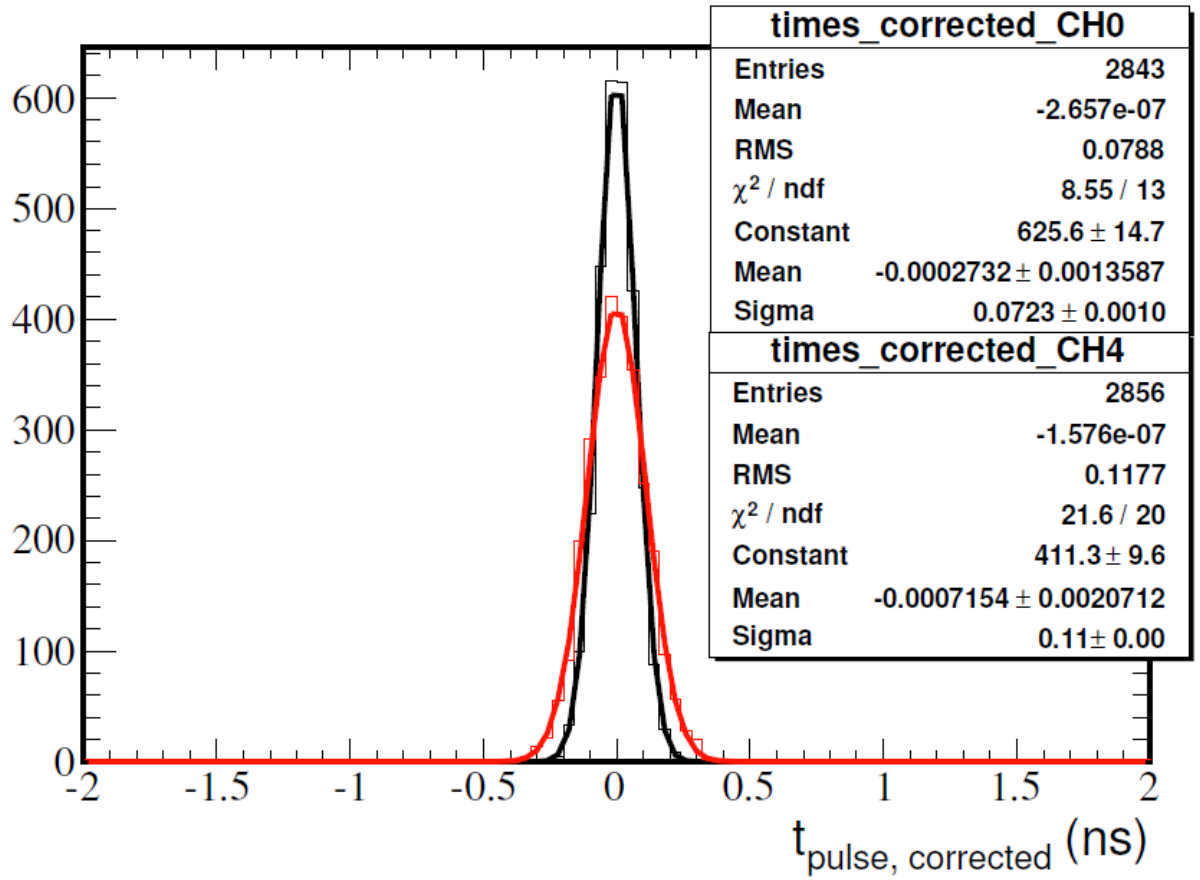
(Left) Residuals of linear fit to laser data on previous slide.

- **This type of nonlinearity is expected for our waveform sampling architecture.**
- **Laser data itself is not ideal for calibrating this effect out.**
- **Instead, we use fixed-amplitude "MCP-PMT-like" pulses (example below).**
- **Use measured nonlinearity vs. sample number (lower left) to calibrate.**



11

Resolution after Timing Correction



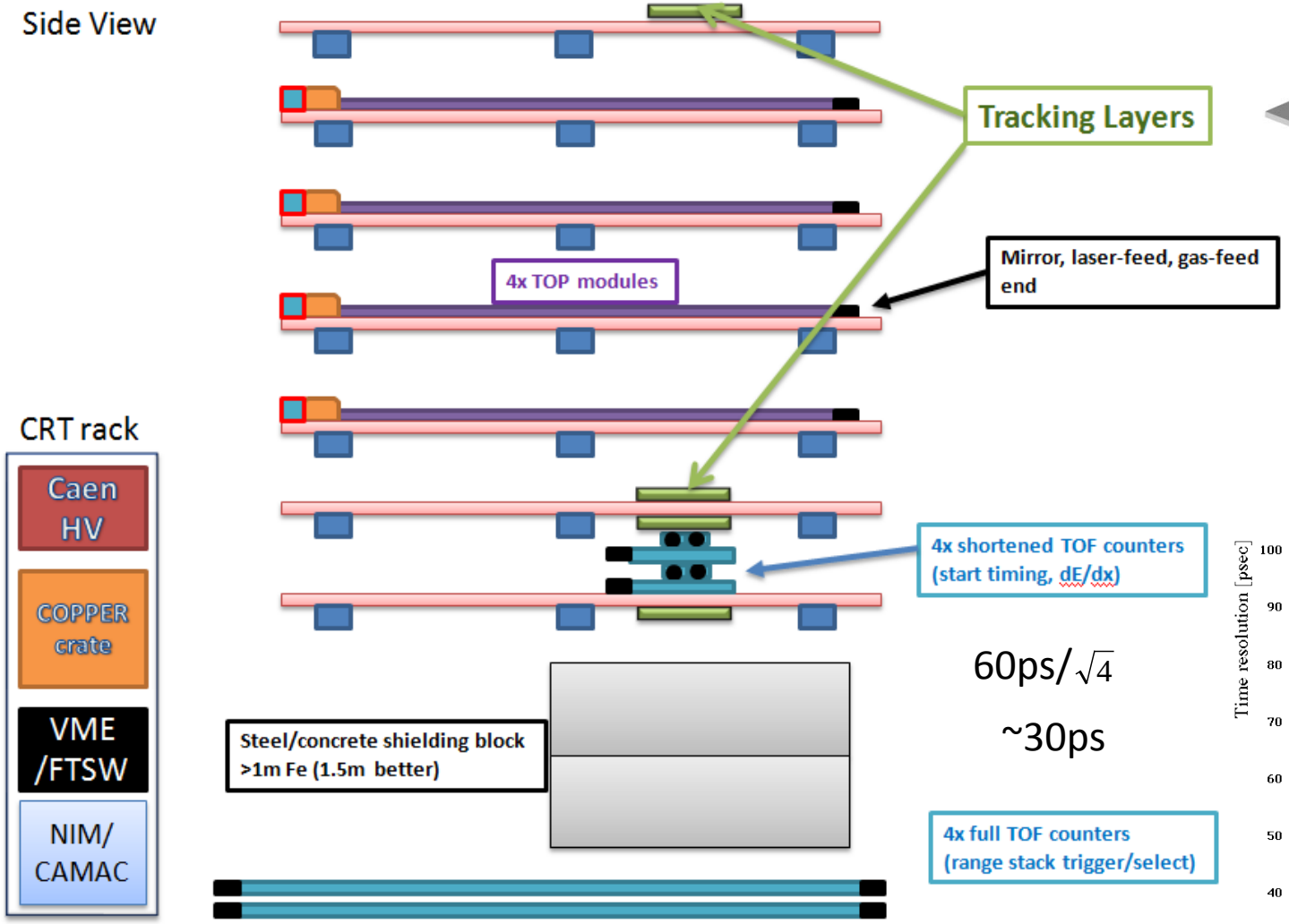
- **Example corrected timing resolutions for one ASIC: ~70 ps (best) to 110 ps (worst).**
- **Resolution generally worse in higher channels.**
- **This resolution includes all known pure-electronics effects.**

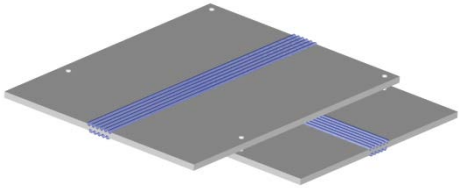
Resolution is probably sufficient to try applying calibrations to beam test data

This is not necessarily the limiting case, only the current status

Further analysis may allow improvements on this…

Cosmic Ray Telescope (Fuji Hall, KEK)

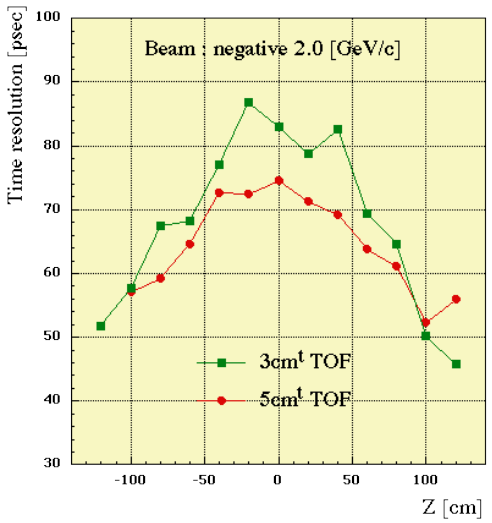




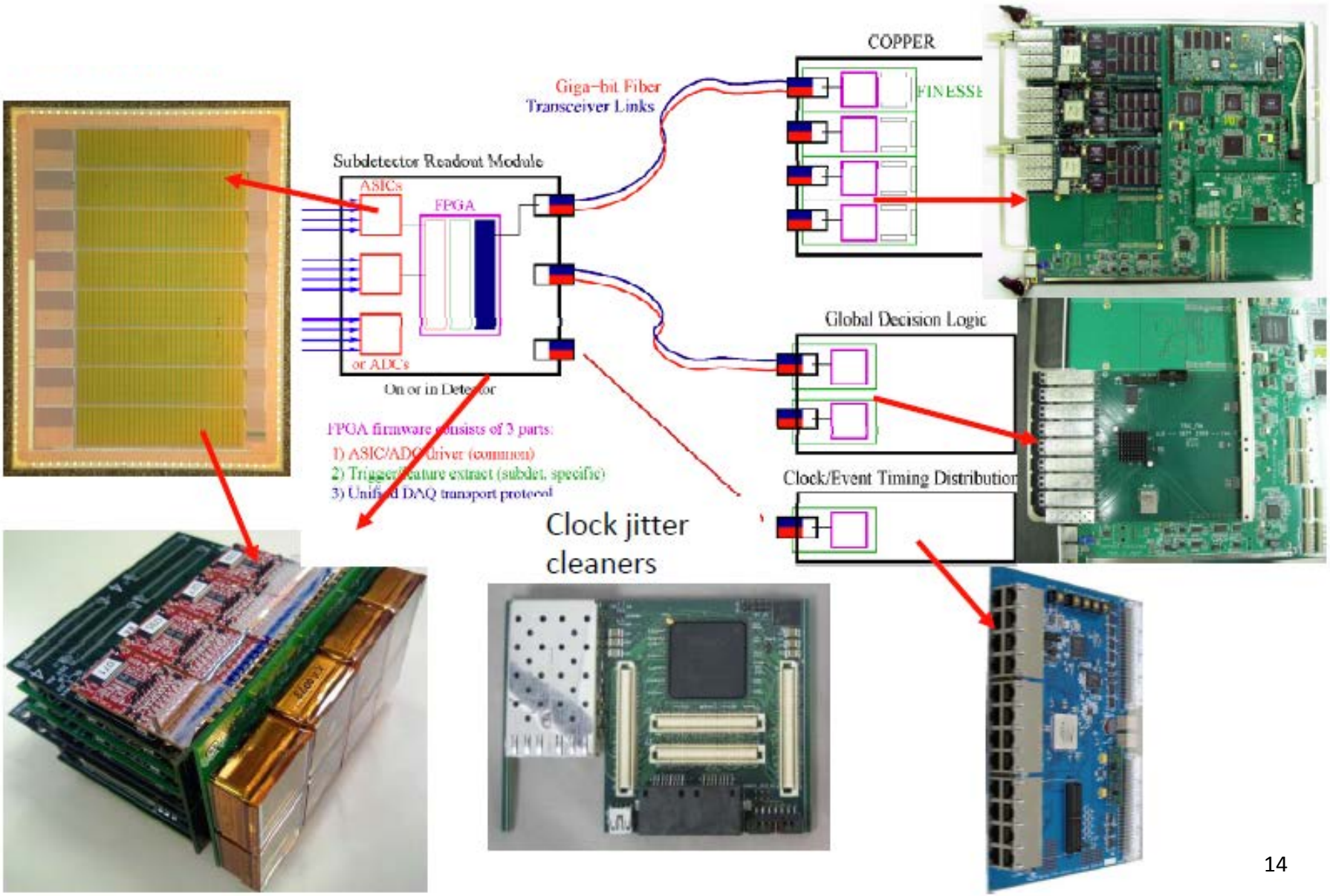
~1mm resolution
Sci Fi tracker over
~2 meters
< ~1mrad

60ps/$\sqrt{4}$

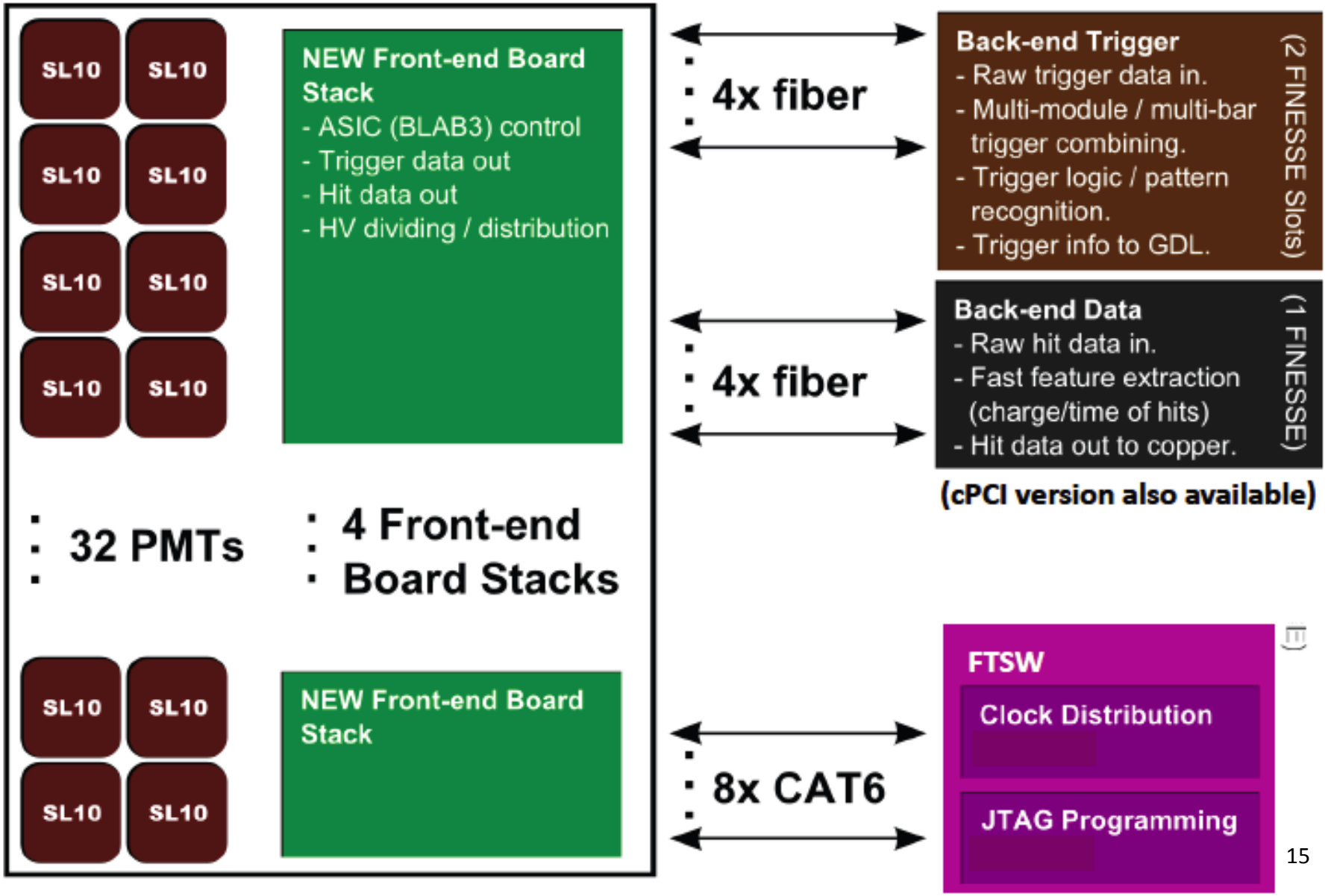
~30ps



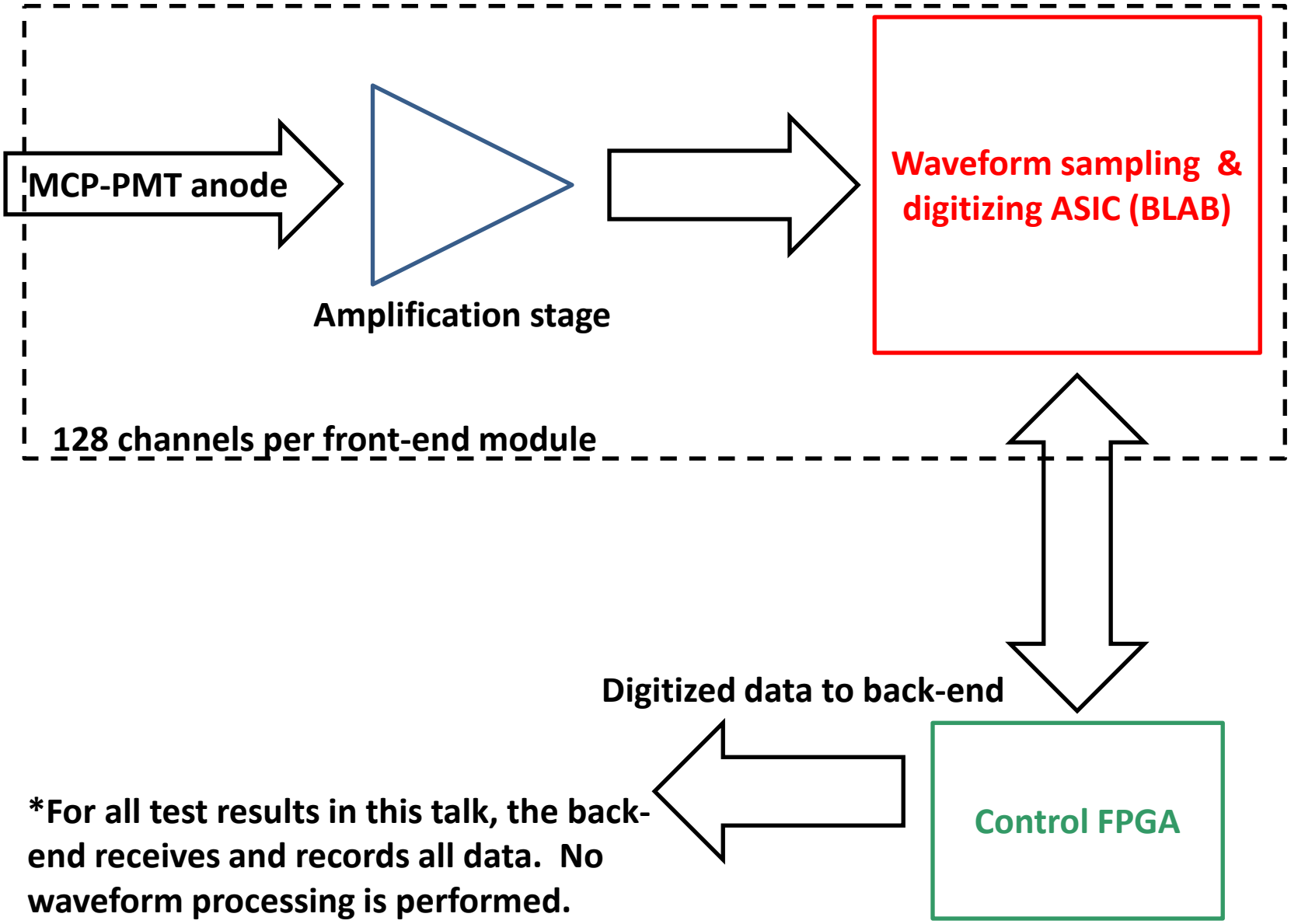
Back-up Slides



Electronics of an iTOP Module

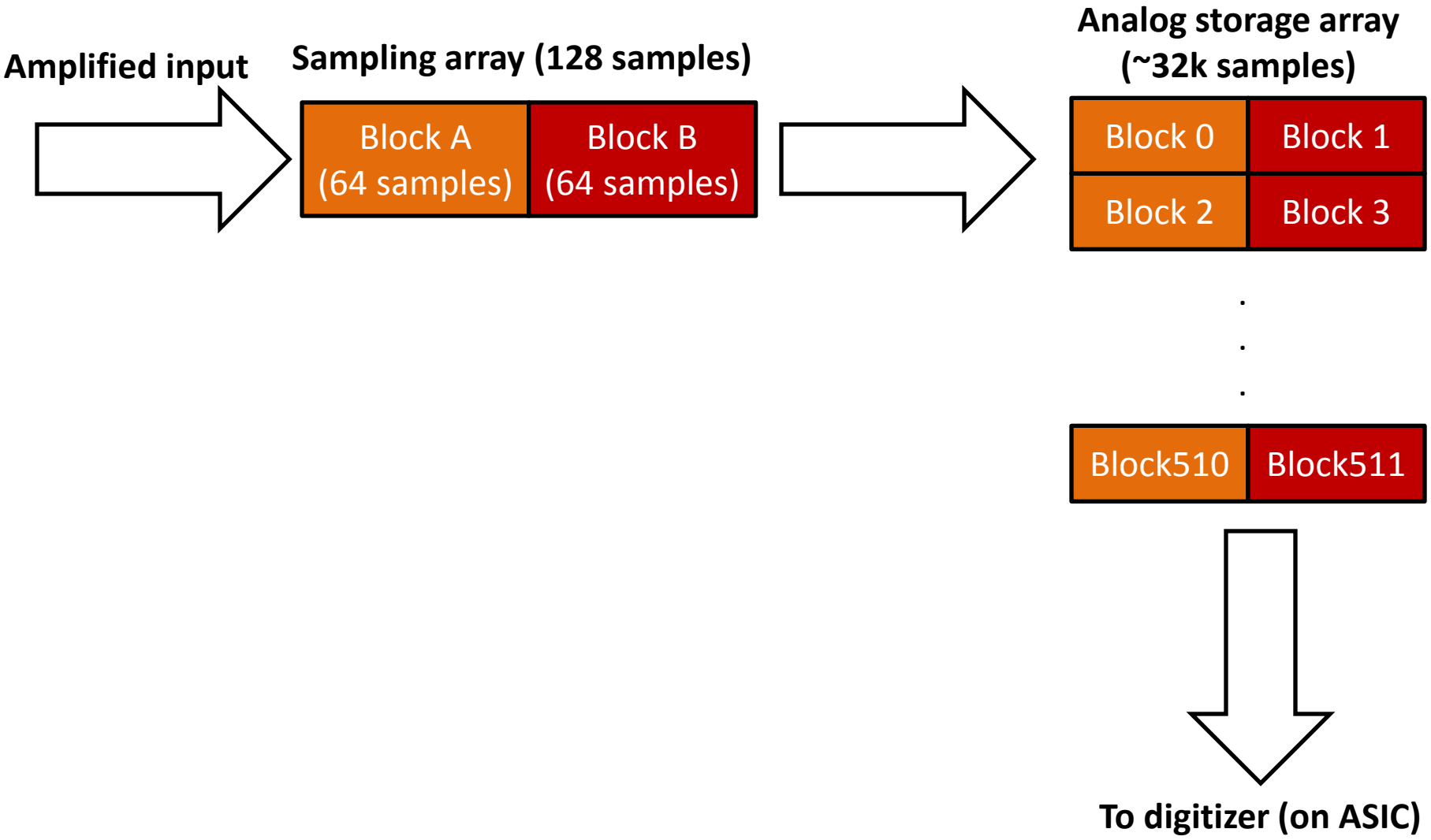


System Operation (Front-end)

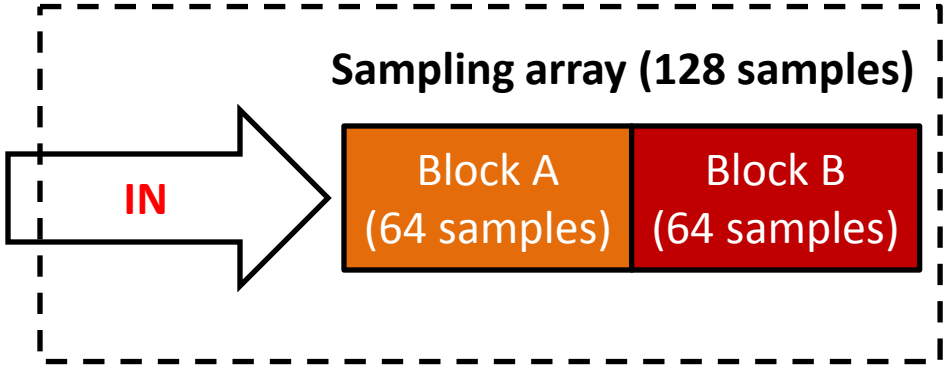


*For all test results in this talk, the back-end receives and records all data. No waveform processing is performed.

System Operation (ASIC)

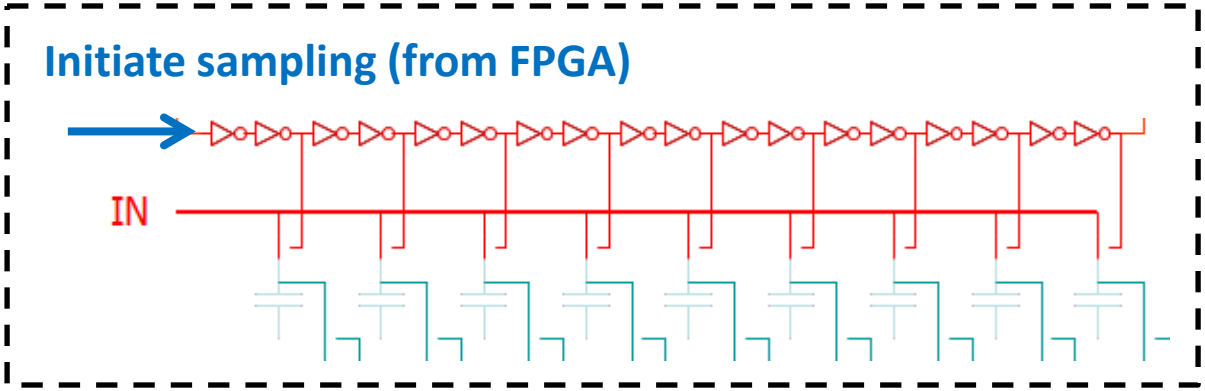


System Operation (ASIC)



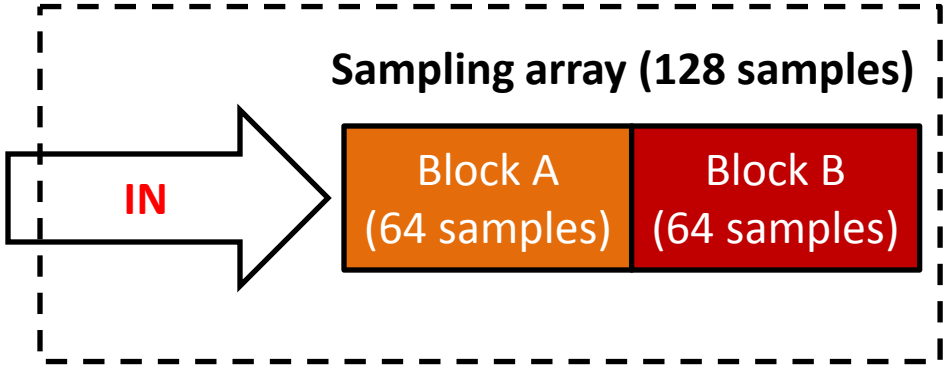
Each capacitor represents a single waveform point

The signal into the inverter chain defines the "start" of a 128-sample waveform.



Huge power savings by not actually performing A->D conversion at GHz rates

System Operation (ASIC)



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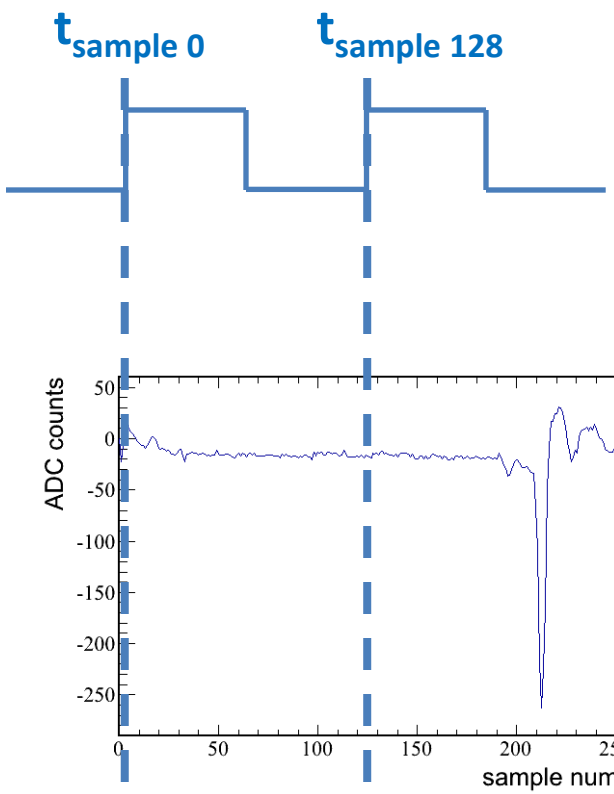
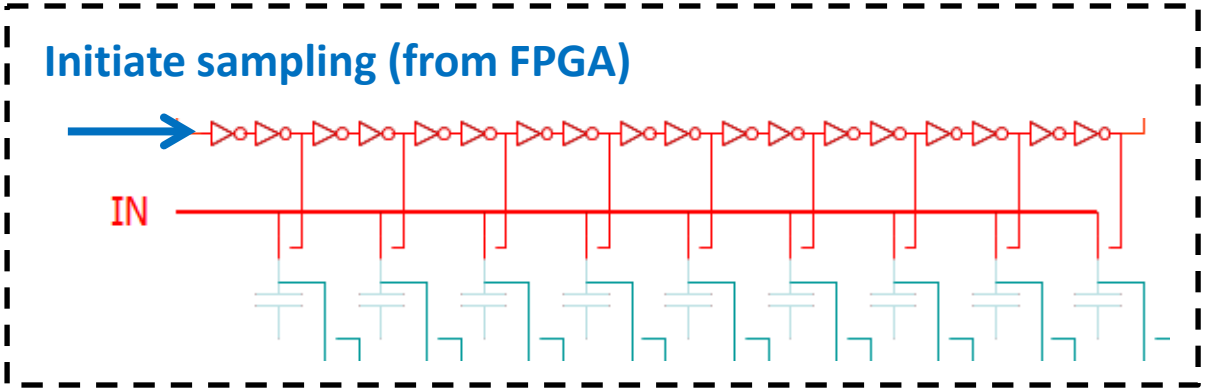


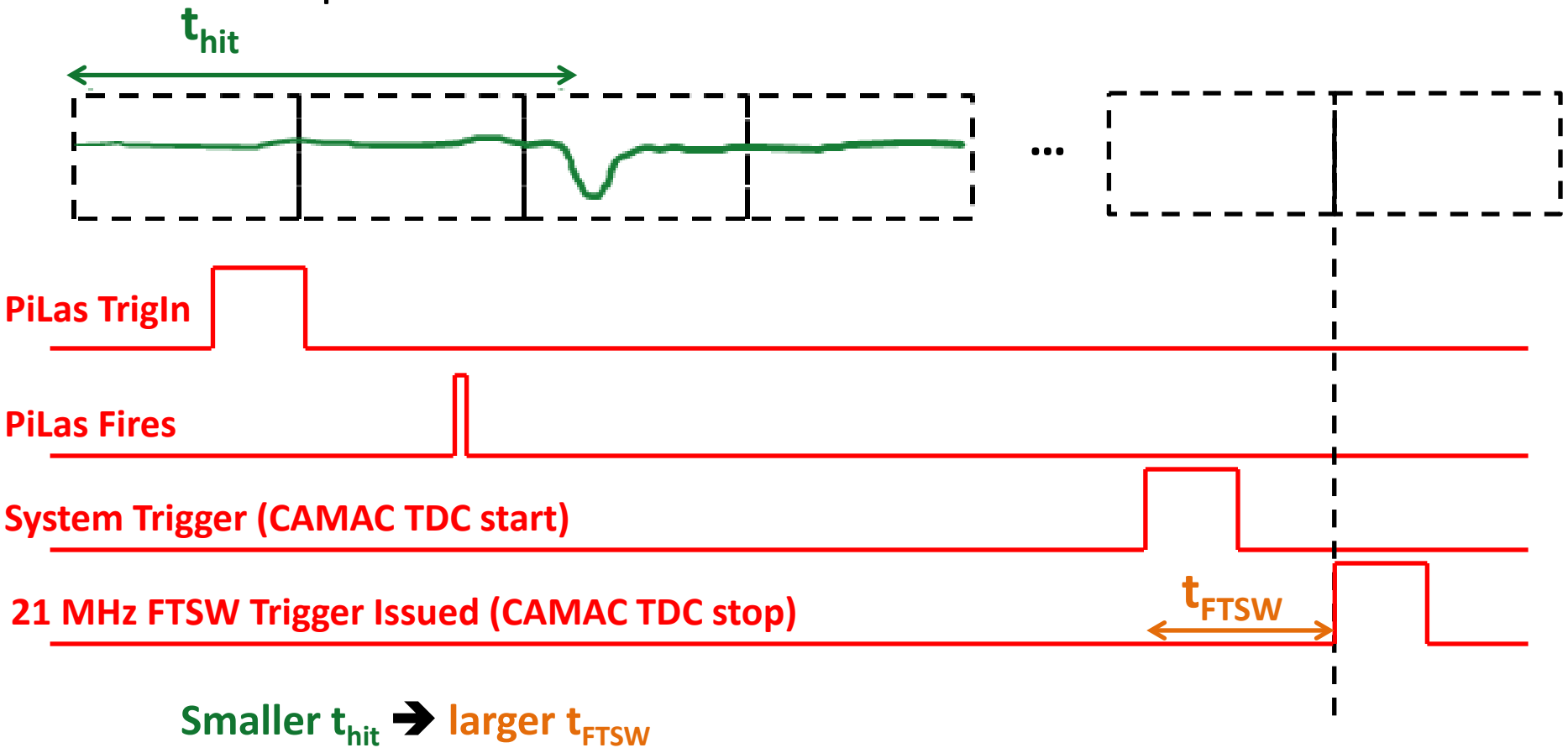


<u>This system imposes two requirements</u>:

- **Jitter on this sampling clock will directly contribute to timing resolution.**
- **This sampling clock must be synchronized between modules.**

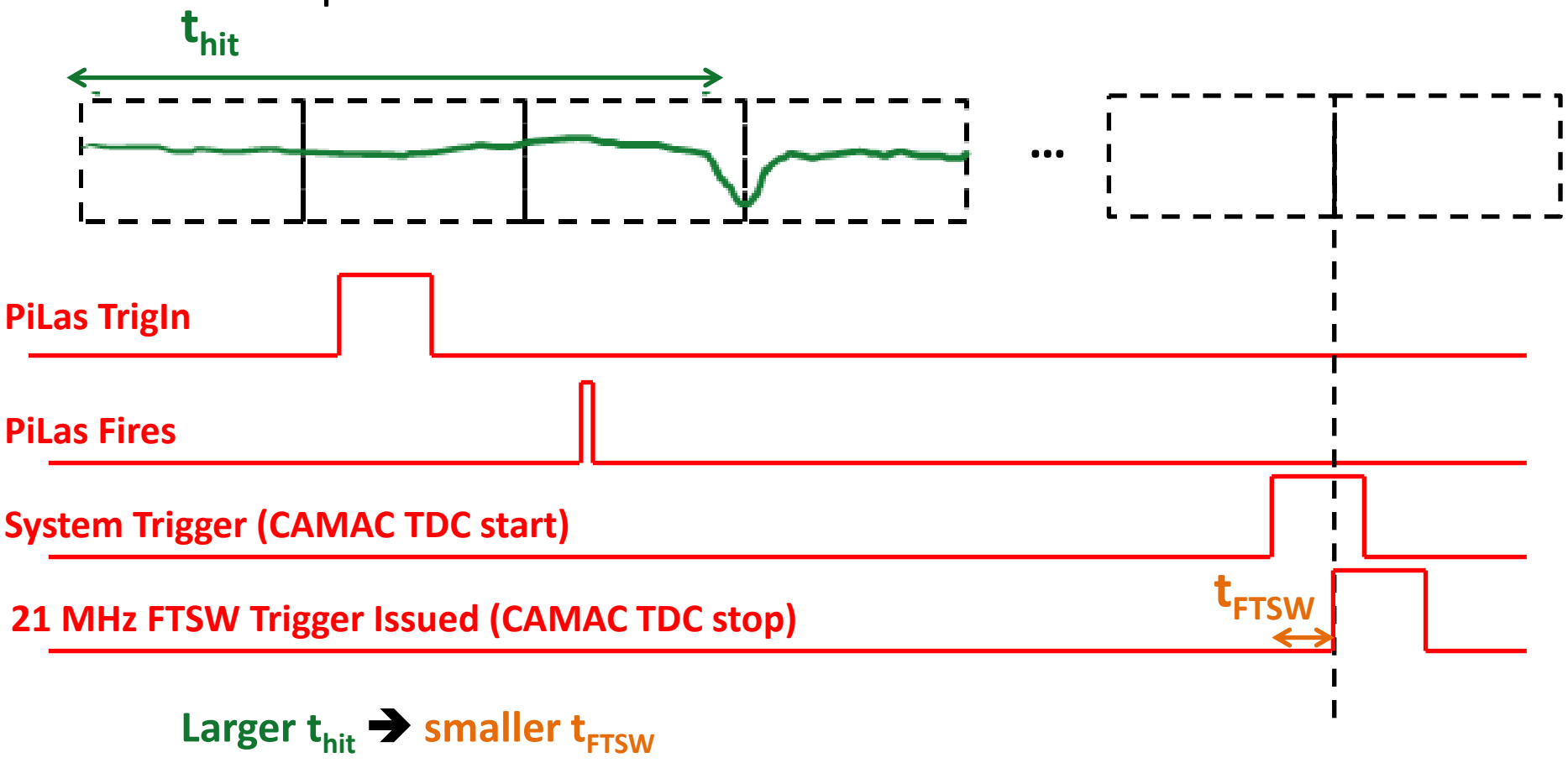
Beam Test Laser Runs

- Laser fired randomly with respect to FTSW clock…
  - …but at a fixed time relative to the global trigger.
  - Example 1:



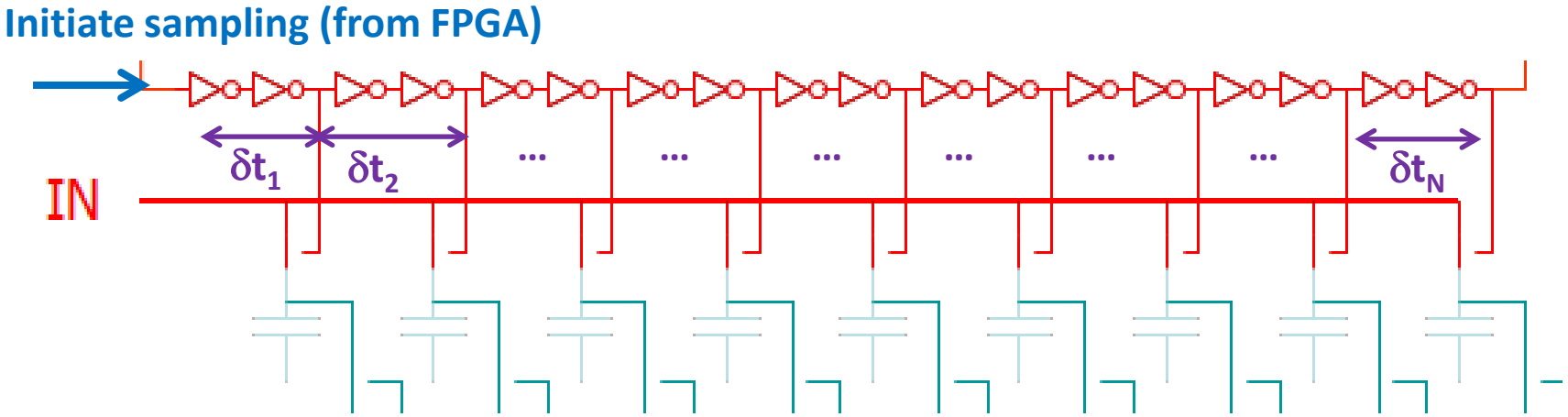
Beam Test Laser Runs

- Laser fired randomly with respect to FTSW clock…
  - …but at a fixed time relative to the global trigger.
  - Example 2:



Source of Timing Nonlinearity

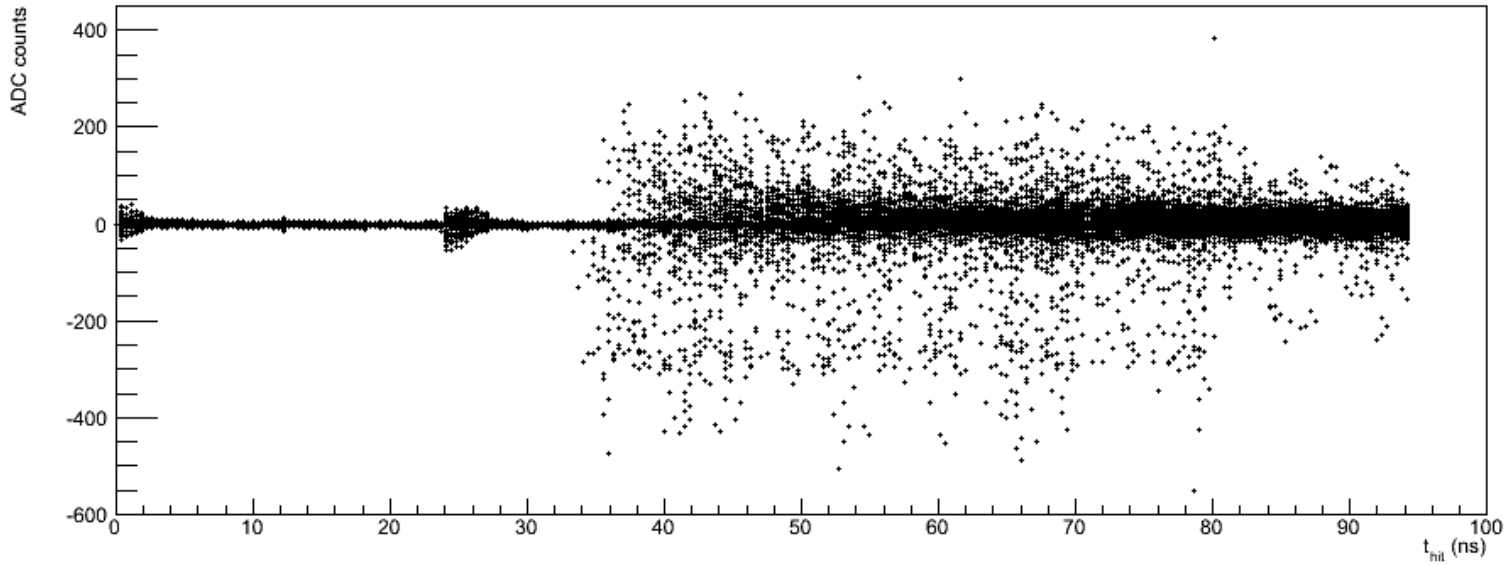
- Delay between individual sample cells is generated by inverter pairs.
  - Process variations make this delay vary from cell-to-cell.



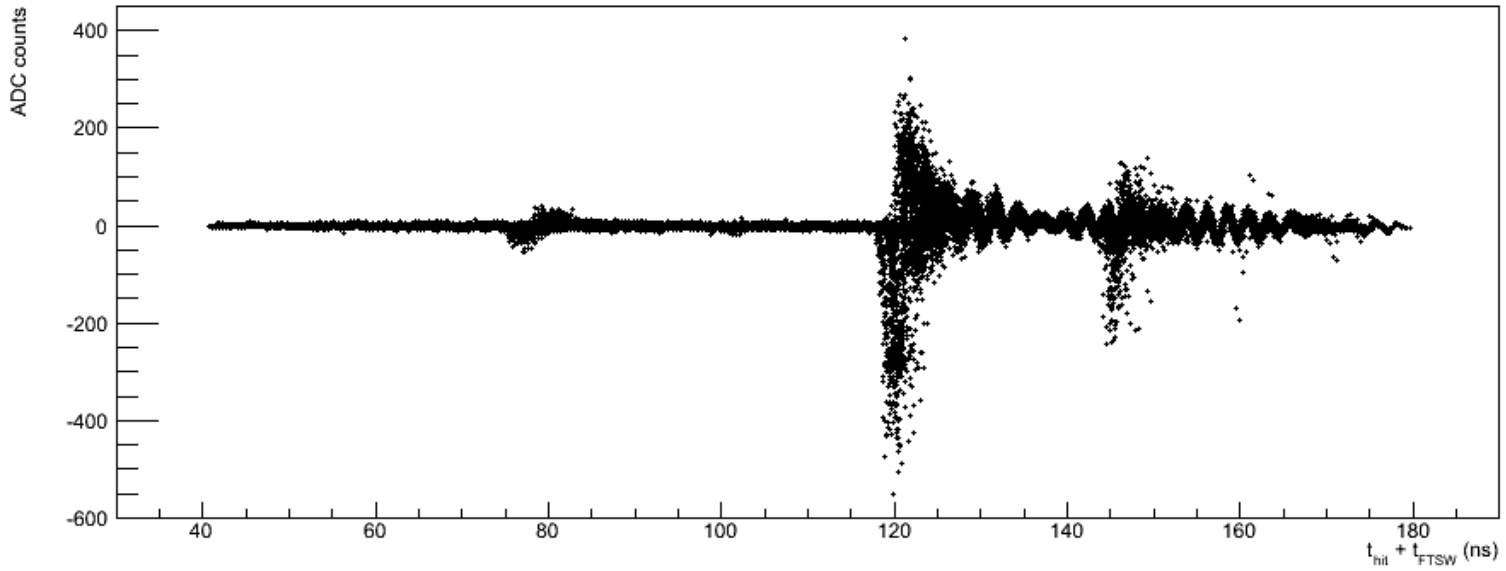
Spread in δt values is typically (15%-30%) – consists of "fixed" and "random" components.

Proper calibration should account for this "fixed" component.

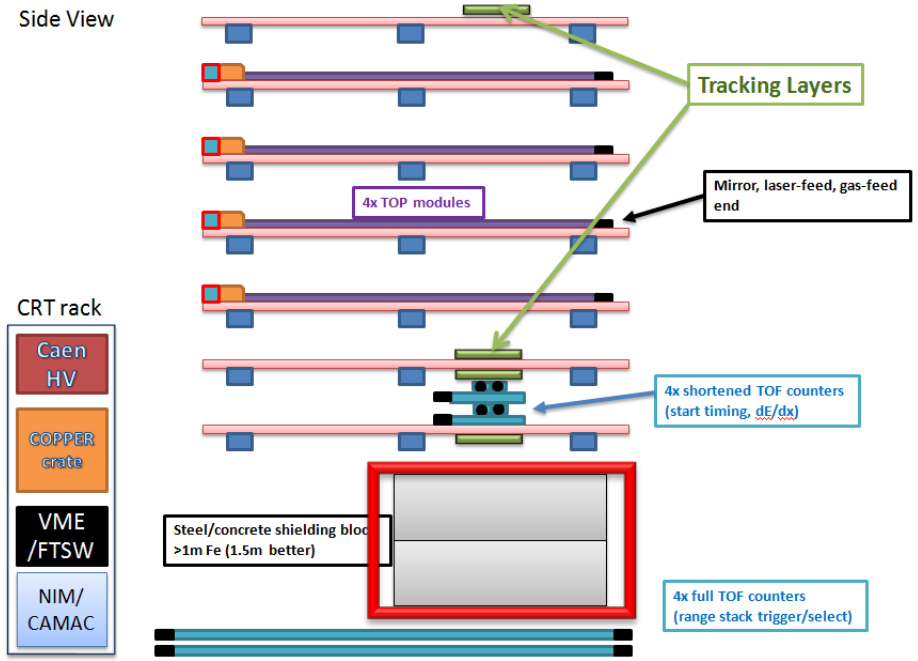
Ensemble of waveforms **before** applying clock/trigger phase offset:



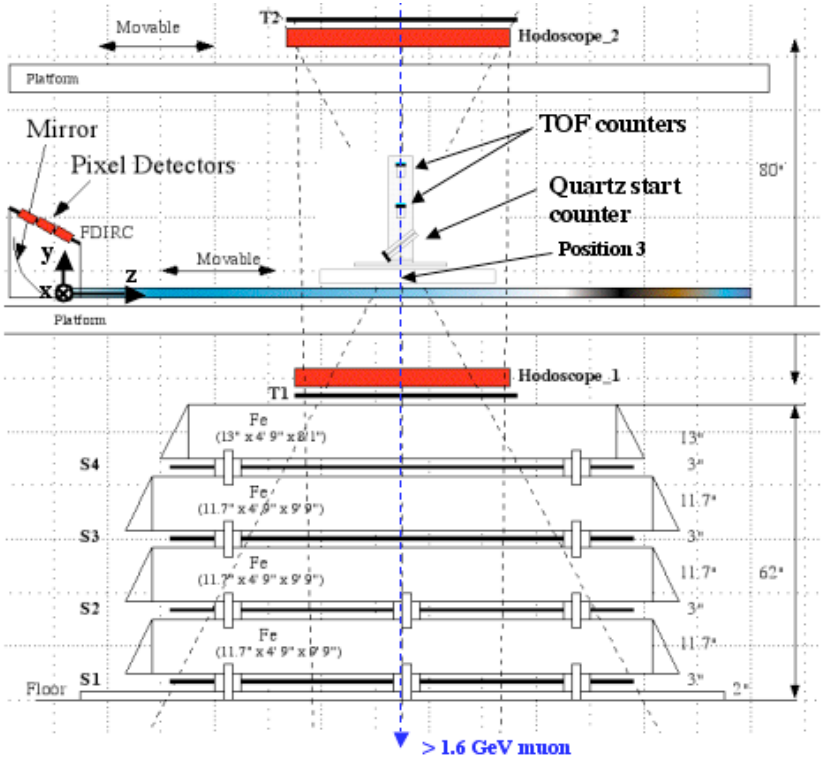
<u>Same</u> ensemble of waveforms **after** applying clock/trigger phase offset:

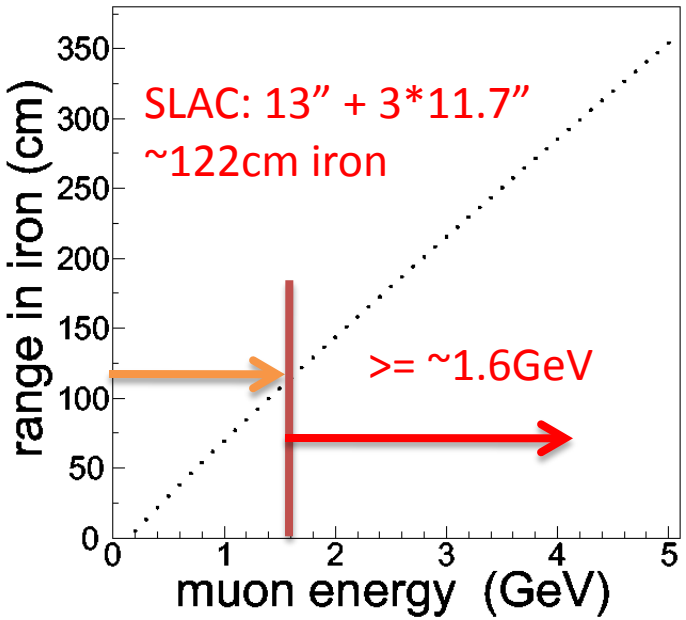


Muon Range stack



SLAC fDIRC CRT





The main stack: