



# CRT Electronics Preparations

- Short Updates:
  - > Further IRS3B testing
  - ➤ Amplifier Performance
  - > HV update
- Posted/presented separately:
  - > PNNL "back end" update
  - Schedule updates
  - > Equipment list follow-up

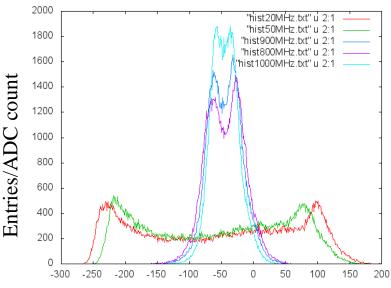
31-OCT-2012 (Hawaii) edition

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### Analog Bandwidth

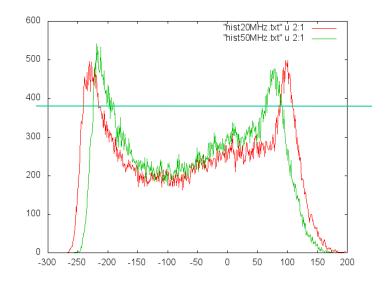




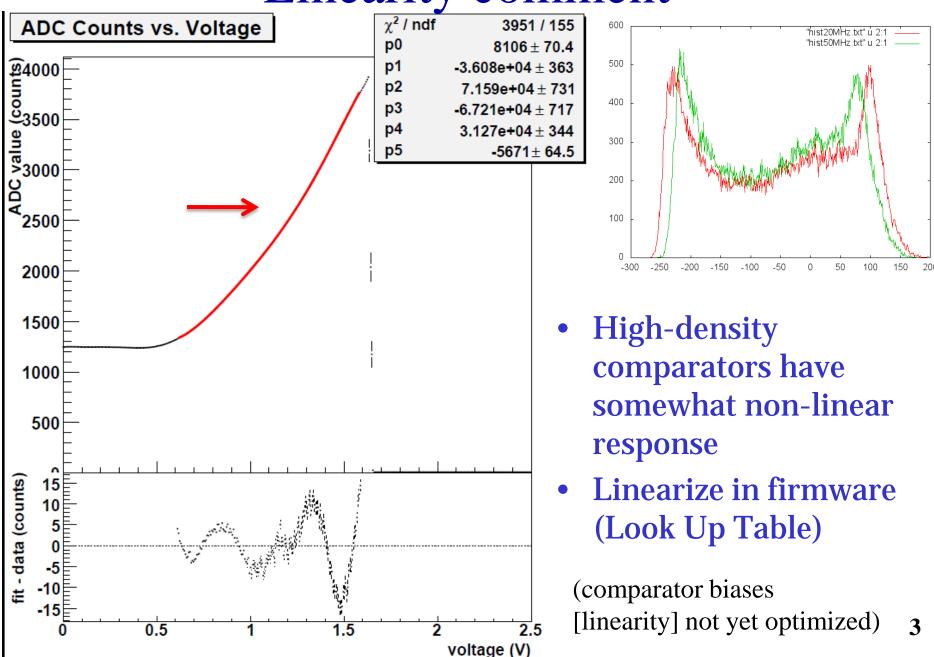


Pedestal subtracted data [ADC counts]

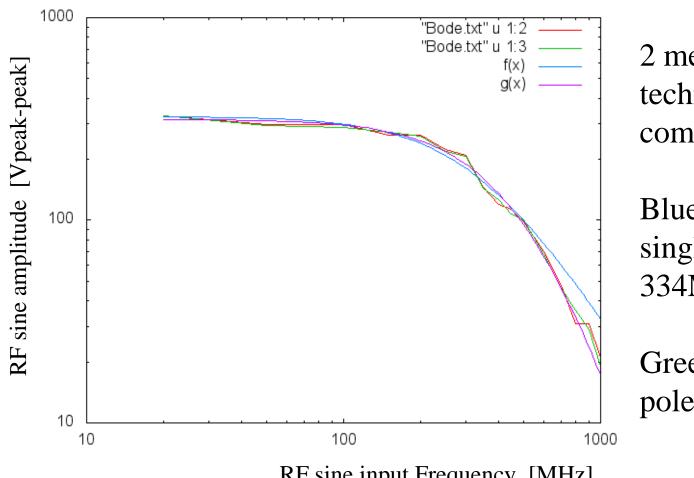
- Data logging coming along
- 2x estimators (sine peak):
  - 1. 90% of maximum
  - 2. Highest entry



Linearity comment



# Analog Bandwidth



2 measurement techniques give comparable results

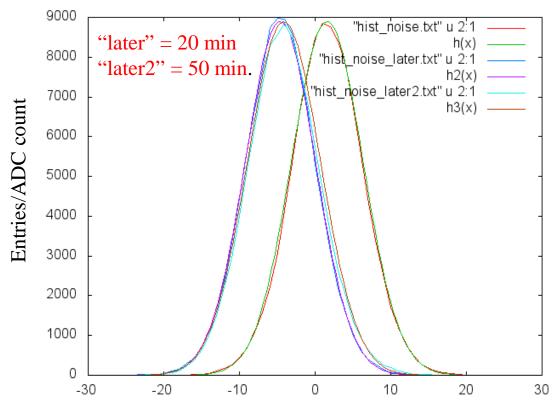
Blue fit is for a single pole at 334MHz

Green is a doublepole

RF sine input Frequency [MHz]

Best fit (green) for a double pole at 554 MHz

#### Noise measurement



No signal input, pedestal subtracted [ADC counts]

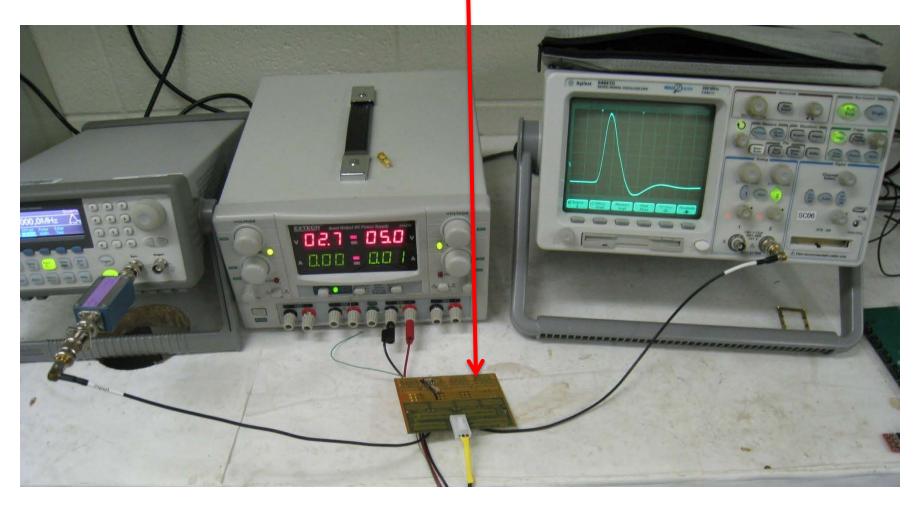


Sets limit on overall noise and baseline jitter

- 100 events, 16x 64-sample windows
- RMS  $\sim 4.6 4.8$  ADC counts
- Gain needs calibration (~mV level)

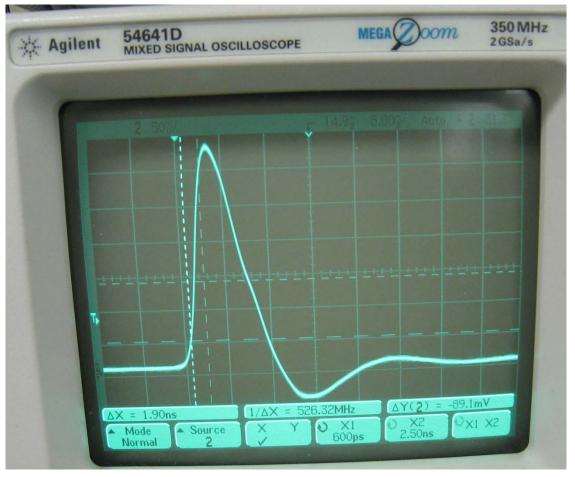
- Distributions very much match the Gaussian fits (h<sub>i</sub>(x))
- Vdly servo-locking off, so drift in mean position due to temperature change, but no "blow-up" as saw with IRS2 pedestals (need to check with Vdly feedback on)

# New Carrier + Amp test



• OP846 (lower-power) amp installed

#### New Carrier + Amp test



Sync signal differentiated to give fast input

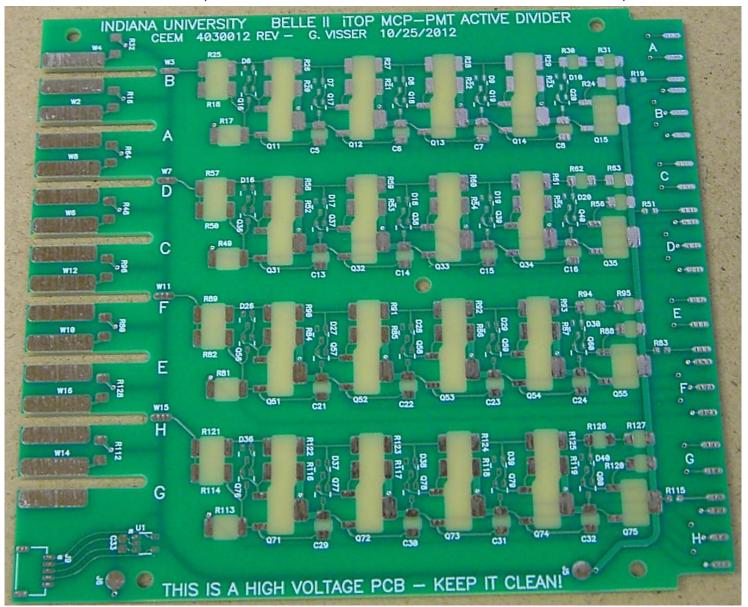
1.9ns risetime

Modest amount of overshoot (width matches simulation)

5ns per division

• At least 5-6 samples on leading edge

#### New HV (Gerard – board received)



#### Summary

• High voltage cable: RG-316 for testing -- long term stability?? (Gerard is proposing burn-in test)

• Schedule updated, very tight

A lot of progress, but a long way to go