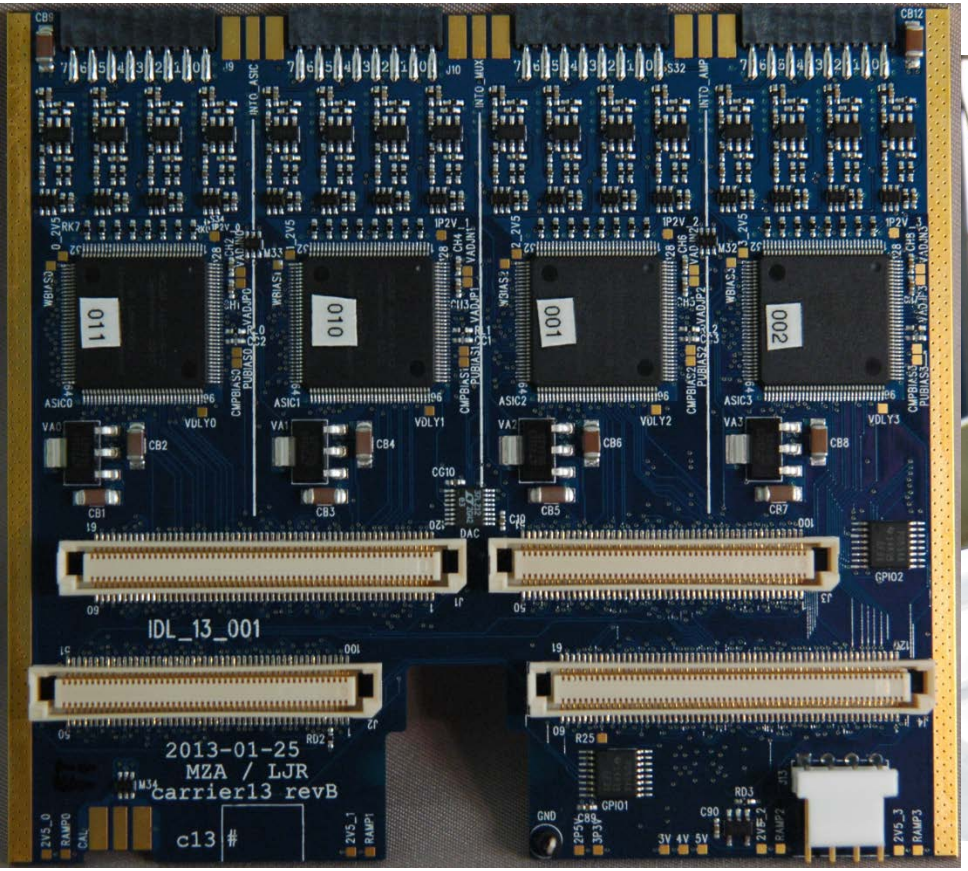
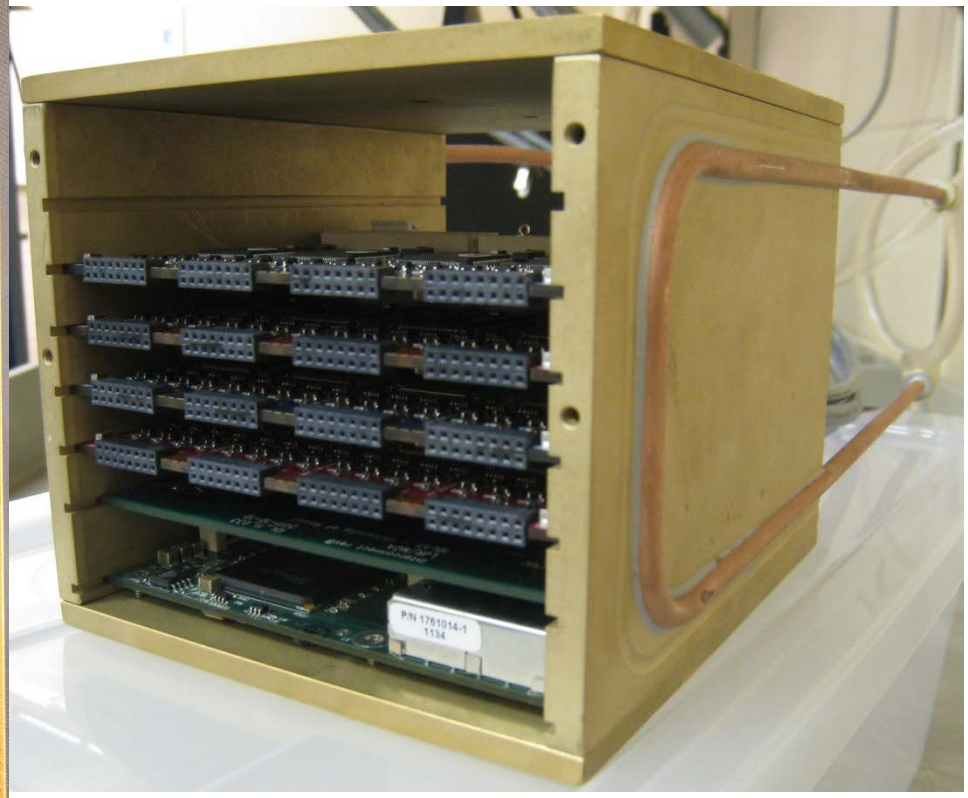
TOP Electro-mechanical Update

(Fuji Hall/back-end update separate)

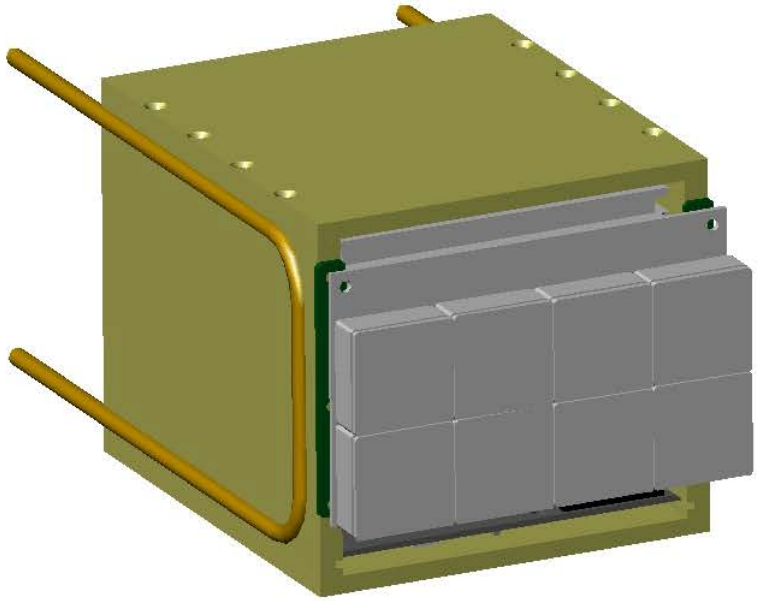


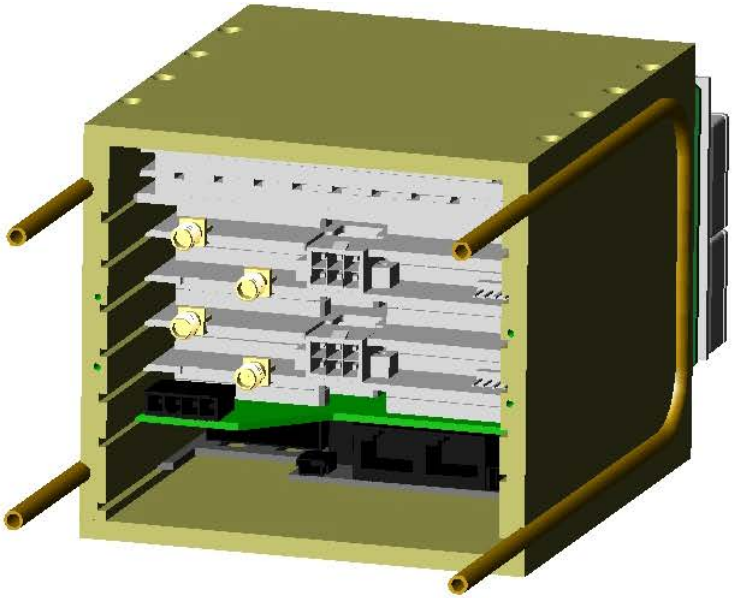


4-MAR-2013

M. Andrew, K. Le, G. Jung, B. Kirby, L. Macchiarulo, B. Macek,
M. Rosen, X. Shi, G. Varner, C. Yee

Improved packaging/thermal

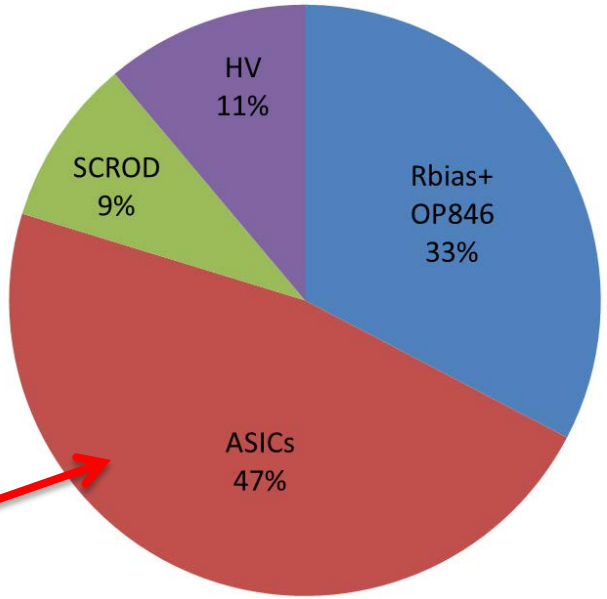




About 31W per board-stack module

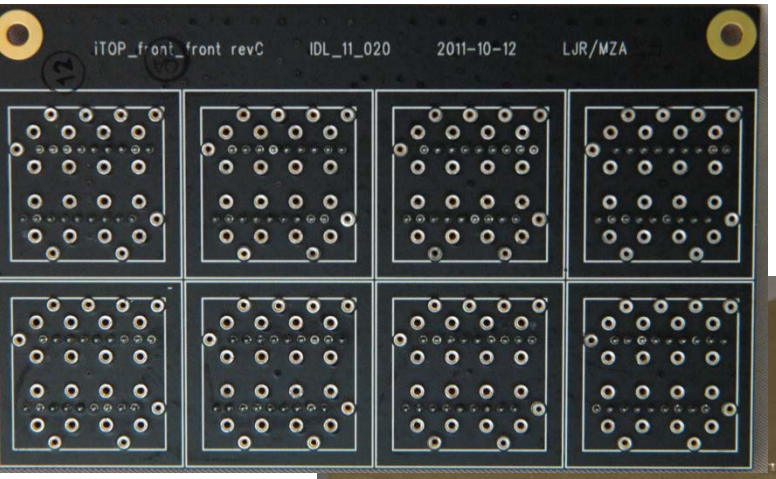
Full TOP, measured numbers

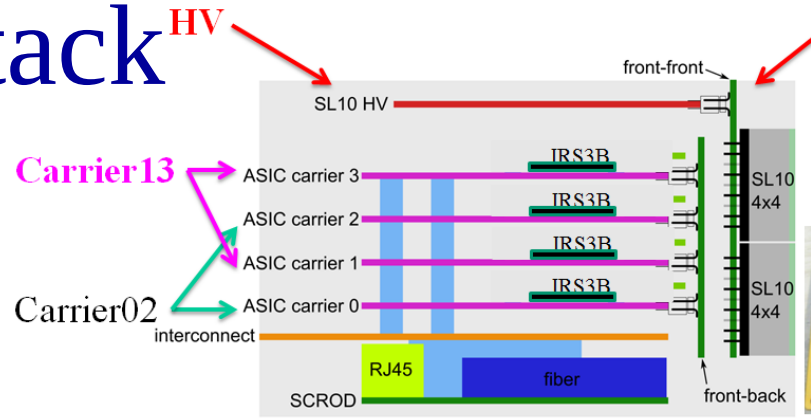
Rbias+OP846	40	W
ASICs	57.6	W
SCRODs	11.2	W
HV	13.6	W
Total	122.4	W

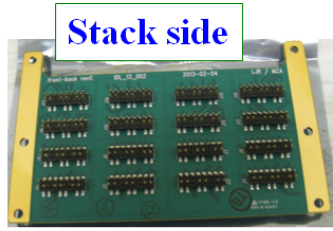


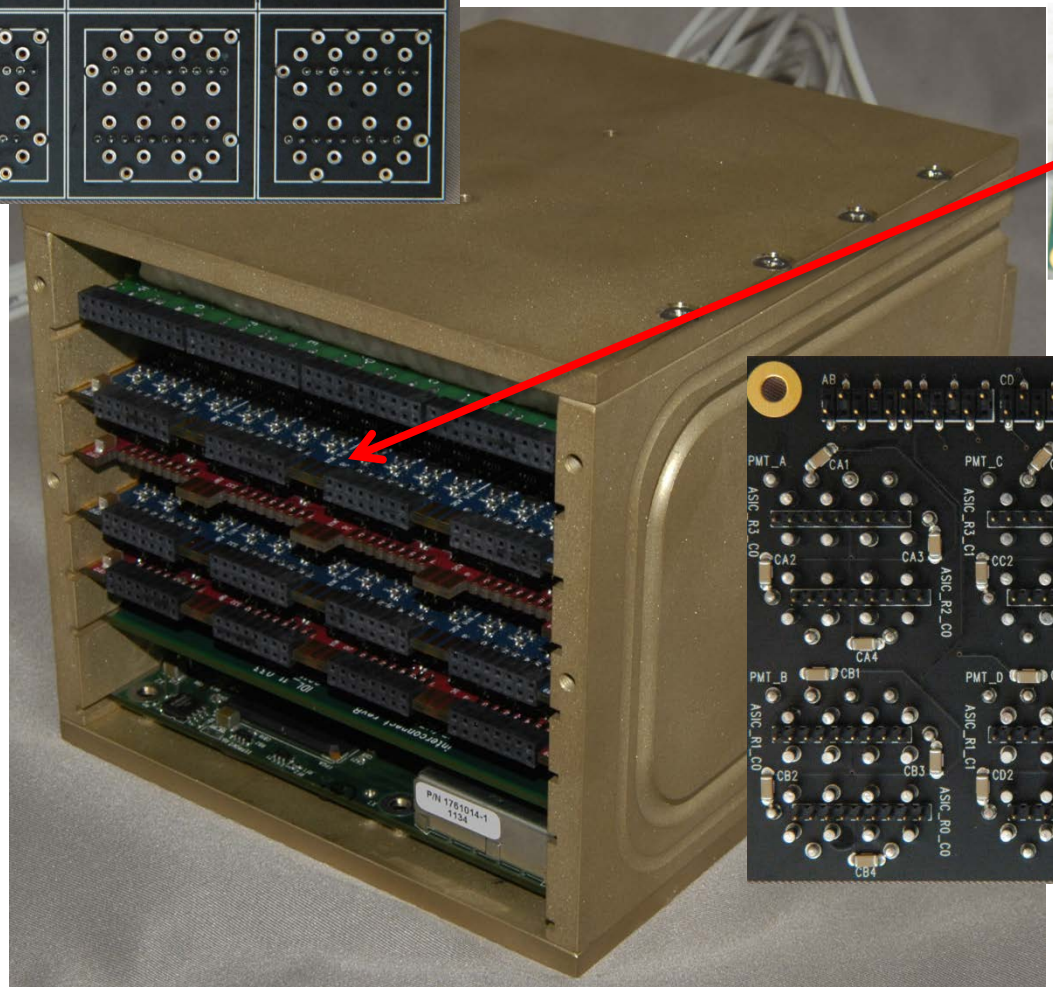
May be possible to tune biases lower

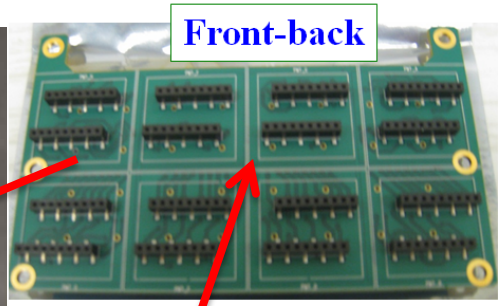
Rev. A2 board stack

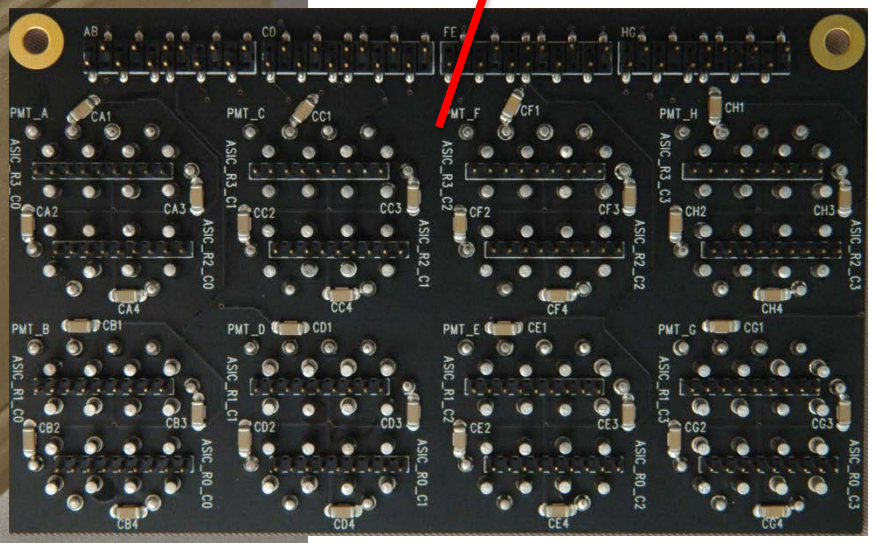






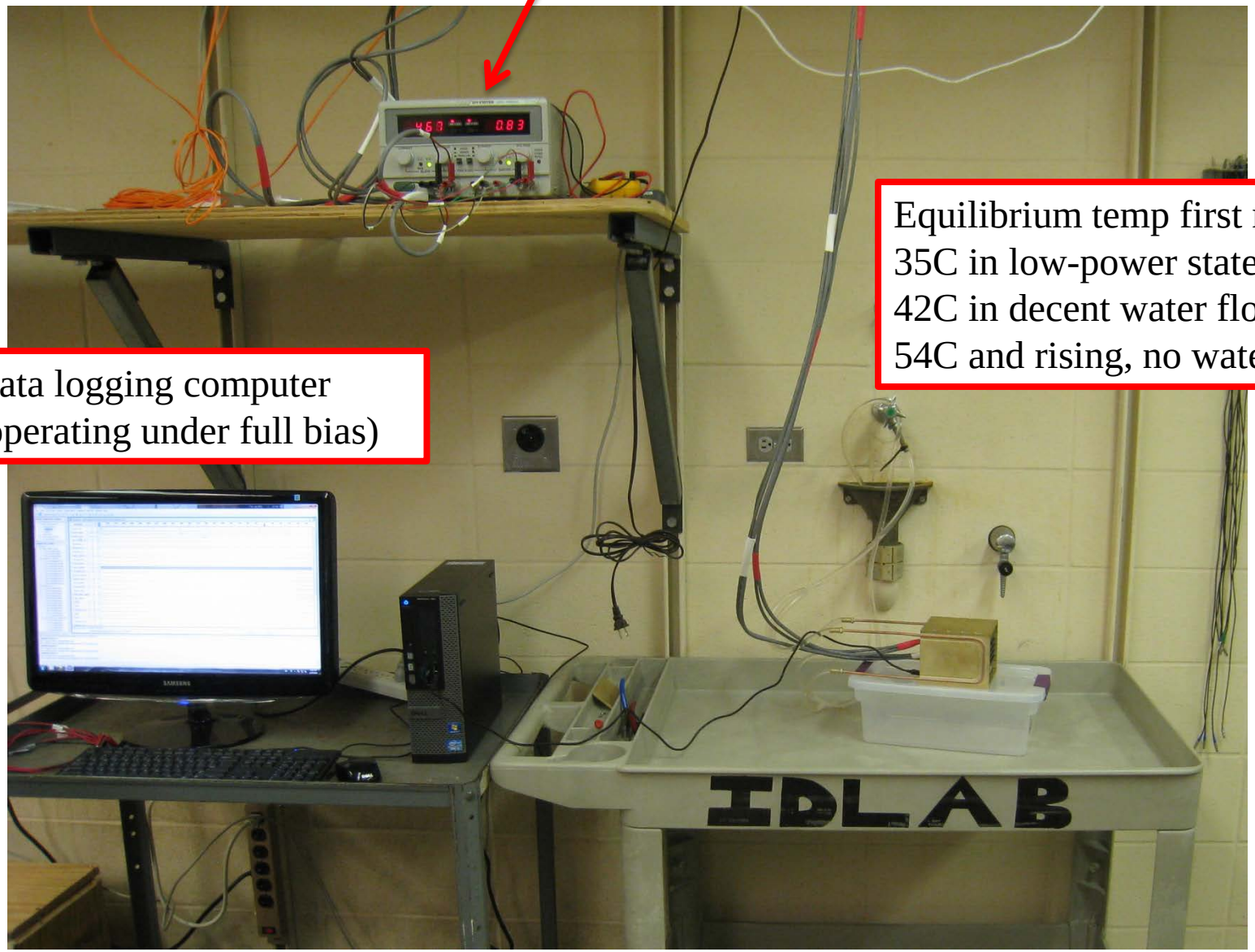






Thermal test bench – Run 1

Module Power: 4.6A @ 3V, 0.8A @ 4V, 2A @ 5V



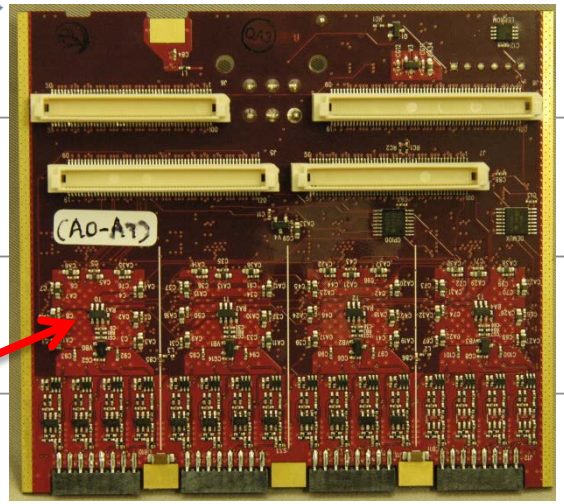
Equilibrium temp first run:
35C in low-power state
42C in decent water flow
54C and rising, no water flow

Data logging computer
(operating under full bias)

Summary of Run 4

Nominal Biases: 4.6A @ 3V, 0.86A @ 4V, 2A @ 5V

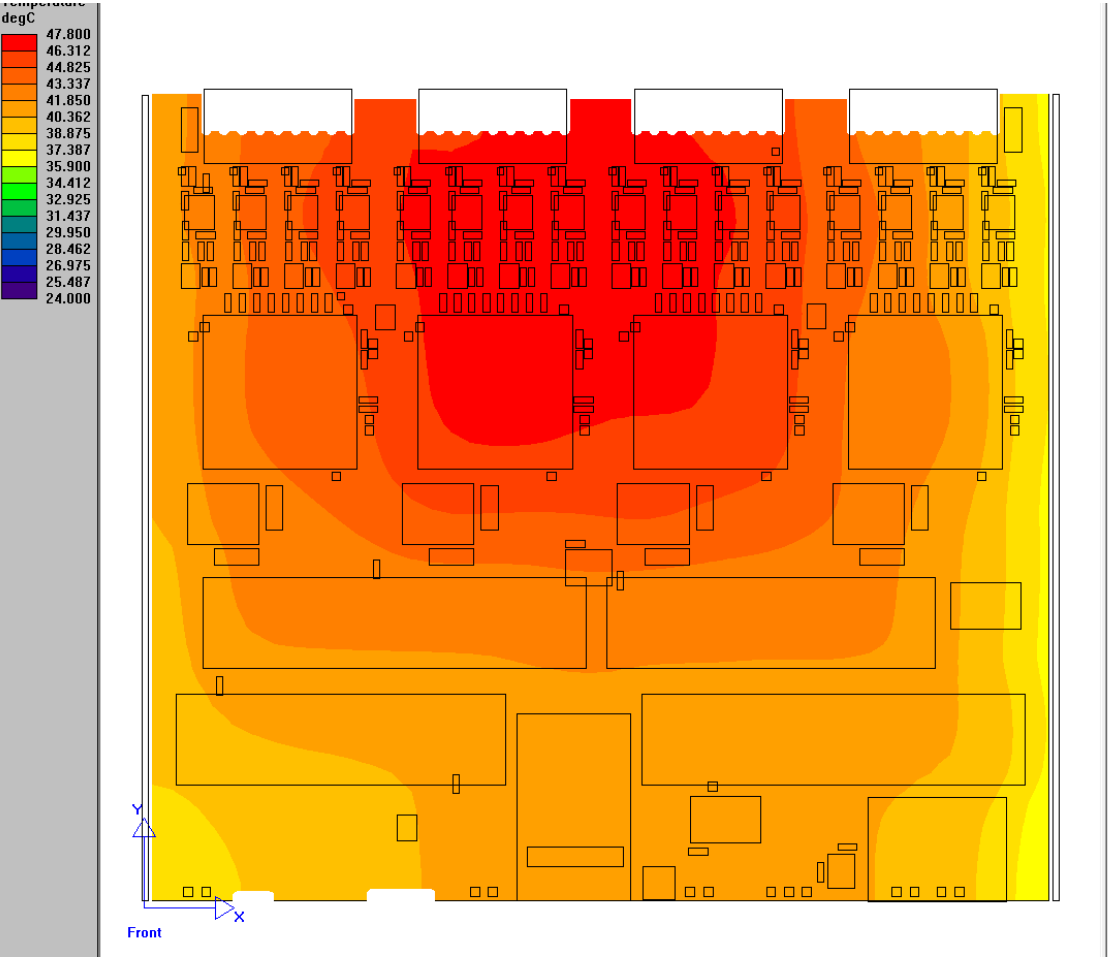
IRS3B "Vbias" = 0x000

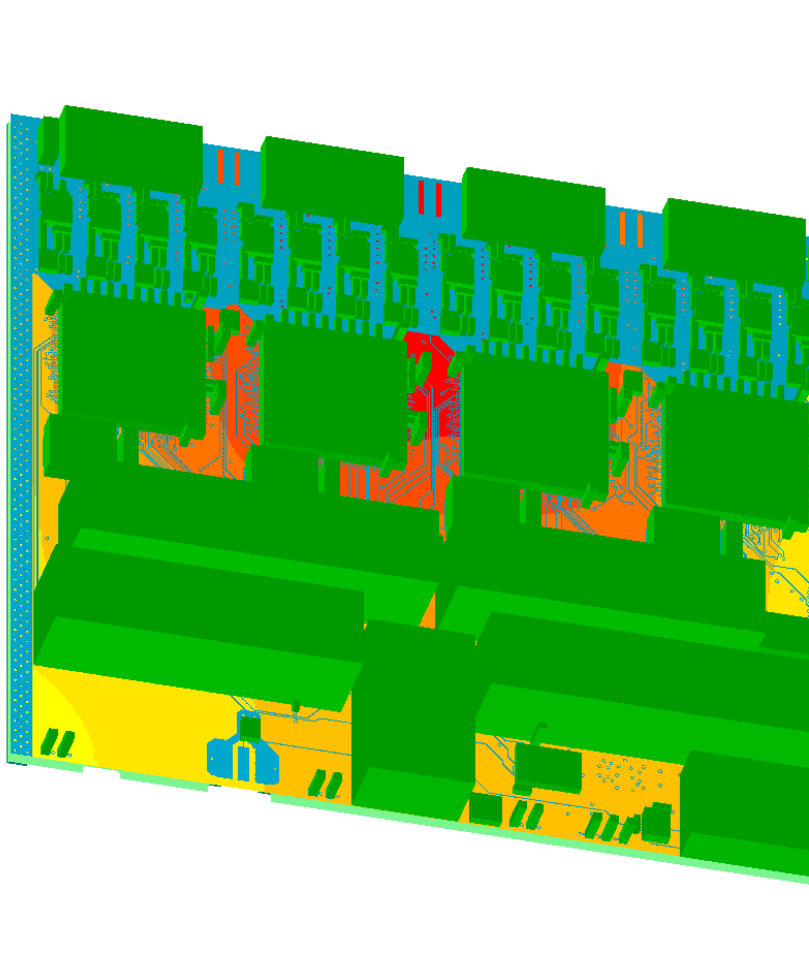


Ch. 1

OP846 unpowered

Revised Thermal Model





Clearly need to do a better job of coupling
To sidewalls (with water flow cool to touch)

Consider compression/
Wedge lock mechanism

Initial Testing

• 62 of 64 IRS3B ASICs verified, all channel 1 see calibration input signal (1 AMUX problem? other is likely configuration debug). Packaged up in thermal housings and 512 channels of readout being delivered to Fuji Hall

• Having programmable control over fine timing adjusts permits automated scans of parameters

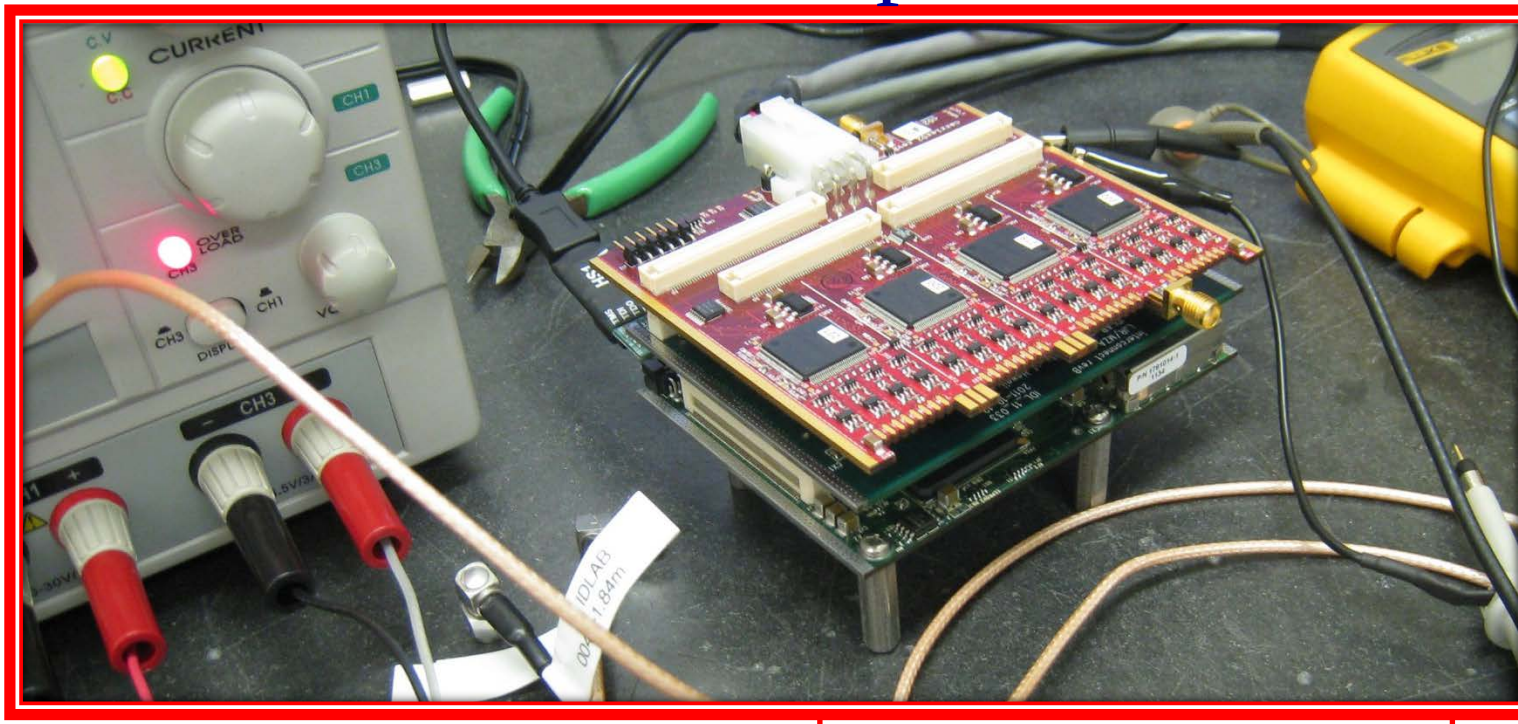
• A few minor issues with I^2C addressing and external DAC bypassing – all have straightforward, though firmware-tedious work-arounds

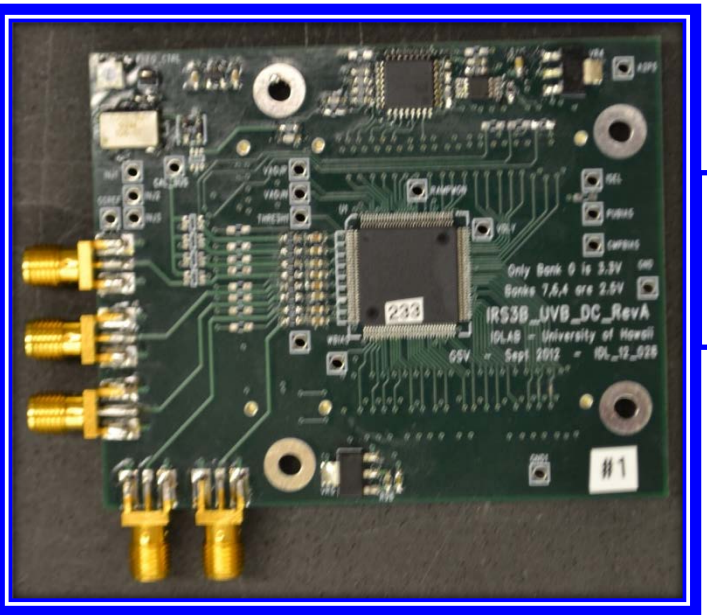
Firmware Development Status

Carrier 02 (top)

Interconnect Rev. A (mid)

SCROD A2 (bottom)





IRS3B firmware (Eval Board)

Firmware v.2 (ROI, full board-stack)

Firmware v.3 (IRS3B, ROI, full board-stack)

Fuji Hall Integration

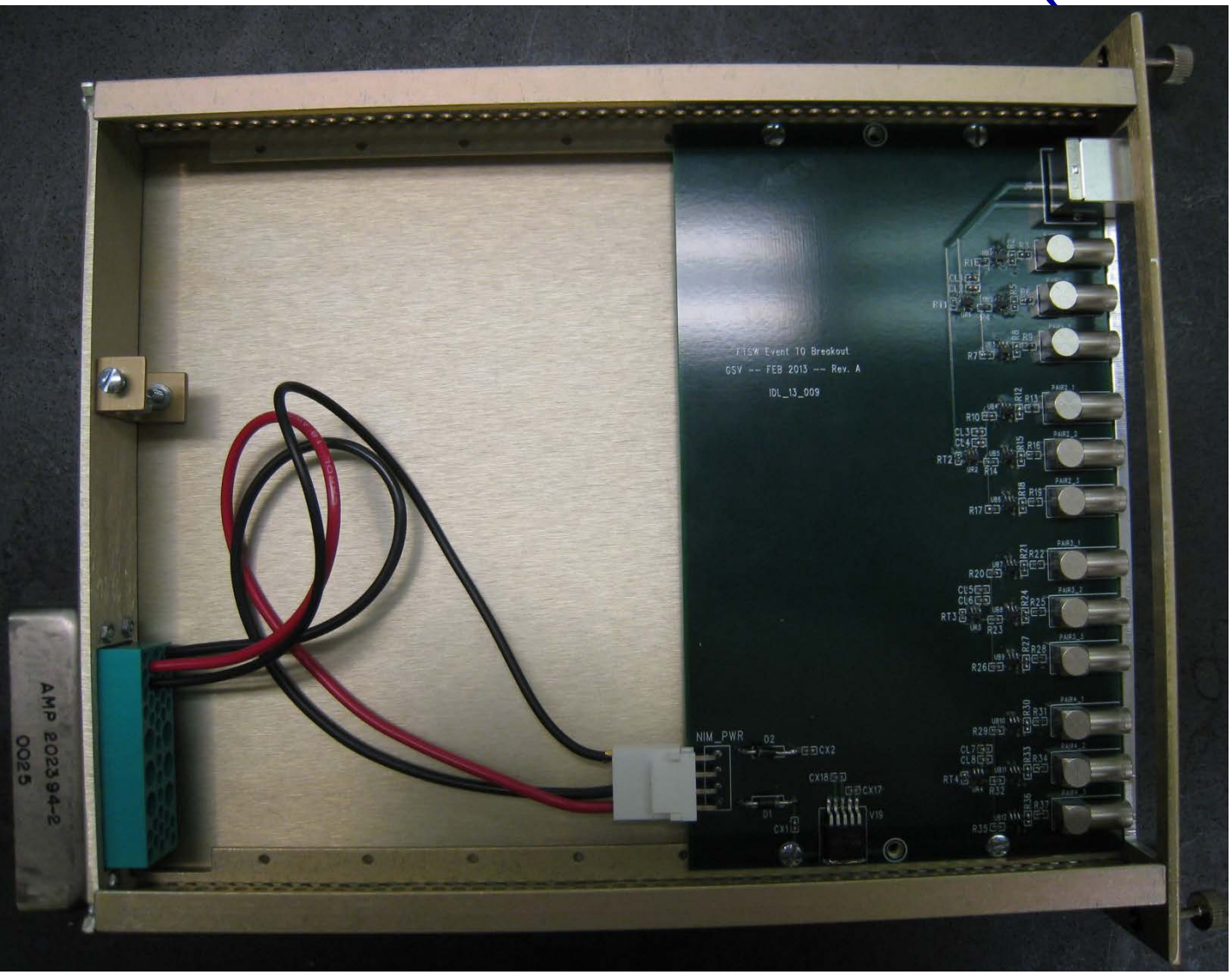
- Integrated power supplies not ready; short term solution (should be ready for CRT(?) or LEPS)

- Next 2 weeks critical for commissioning and debugging data flow – FTSW timing verification crucial (new FTSW LVDS – NIM module)

- Interconnect board Rev. C delayed (has built-in cal source features – for now use ext sig gen); new chassis still to be machined (slide 11)

- **Can do voltage, timing, alignment scans "on demand" on all 512 readout channels in situ**

FTSW Aux Monitor (Event T0)

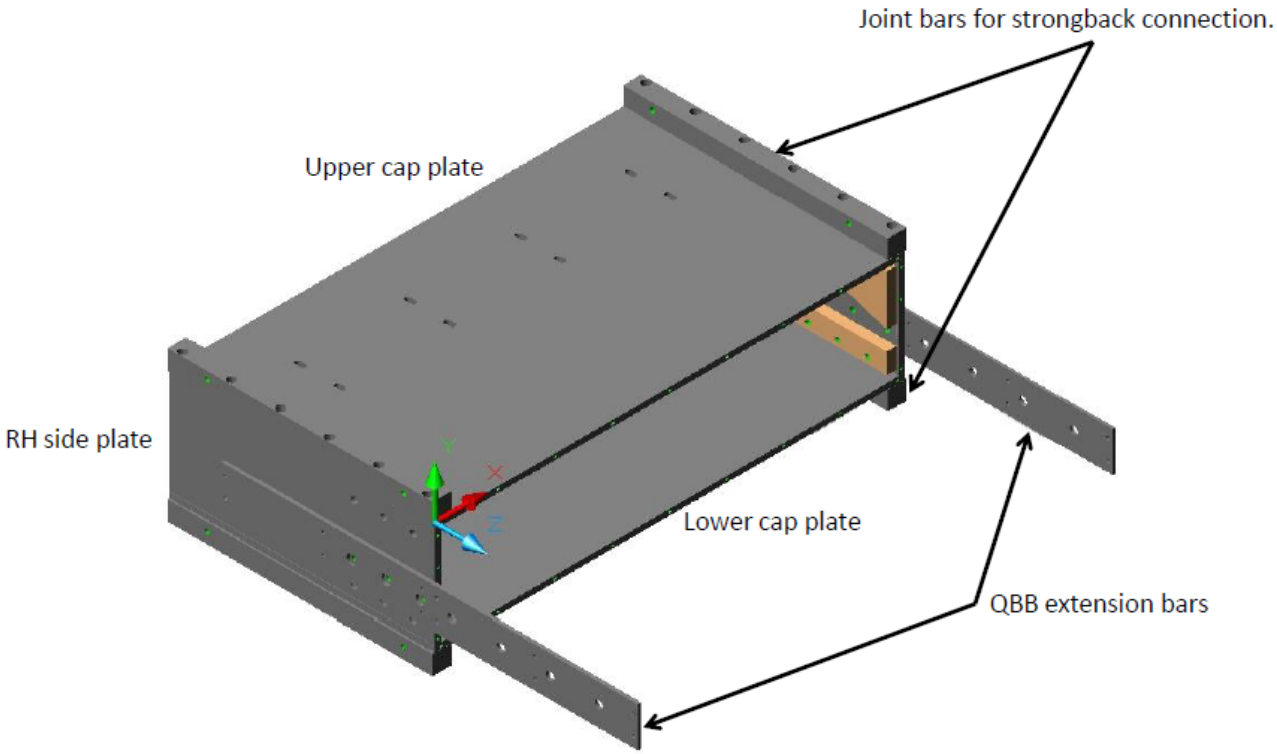


Each AUX LVDS monitor pair has 3x NIM output copies

Tested with FTSW – outer channels Work (network cross-over cable)

New Readout Chassis

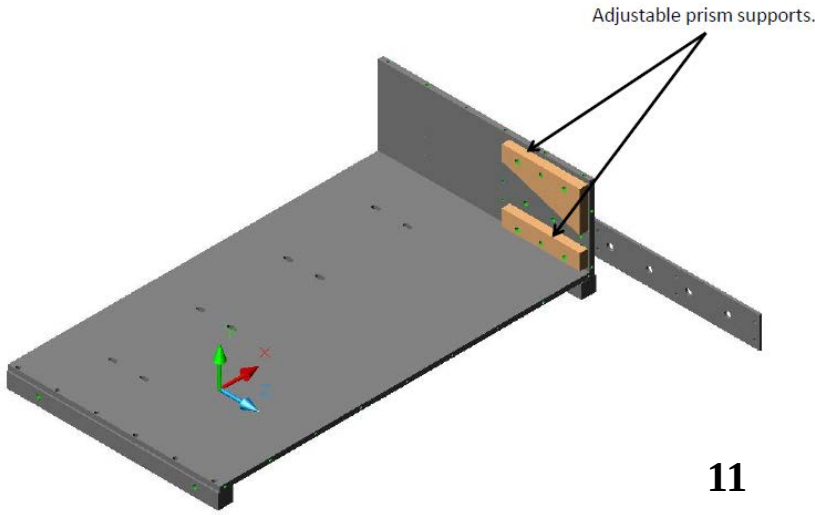
Readout chassis with all components displayed.



Rosen: March 2, 2013

Design complete; to be machined

Material rough-cut, to be finished next few days



Electro-mechanical Summary

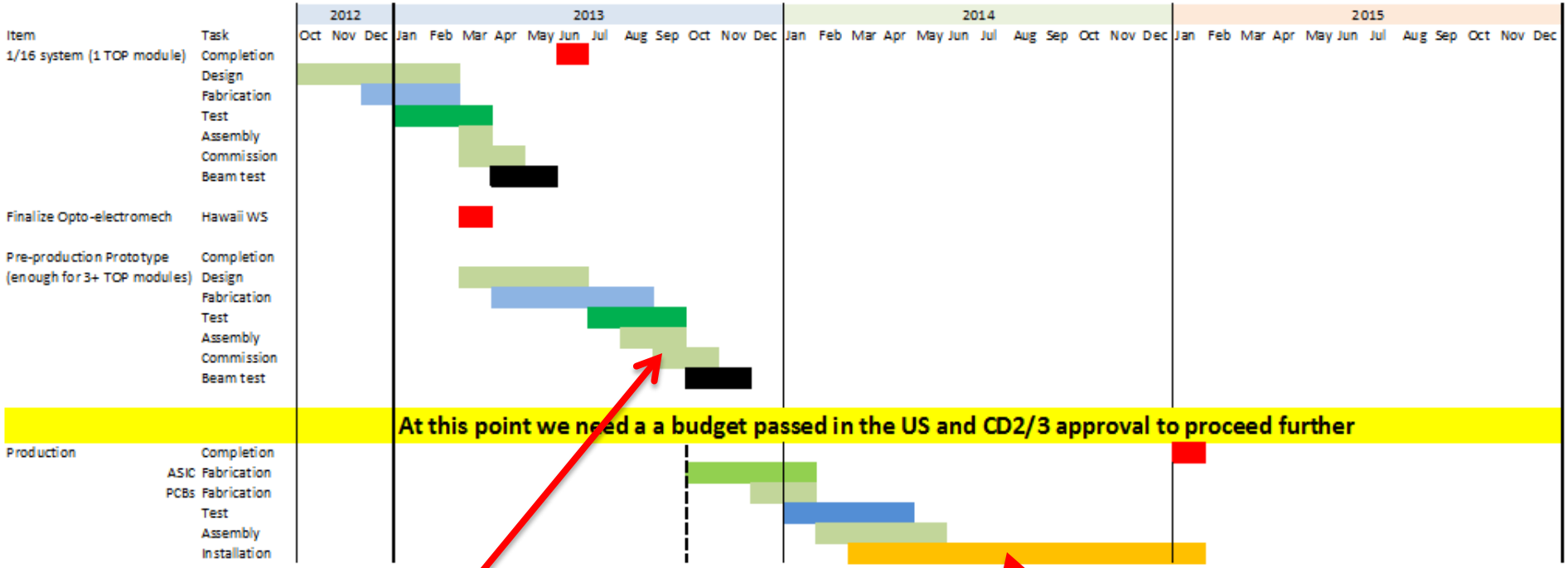
• IRS3B working very well (only change being considered is a method to reduce power-on current surge). No major problems Rev A2 boards

• Full TOP bar “1/16 prototype” E-M readout delivered for installation in Fuji Hall this week; integration with COPPER-based readout

• Firmware works in pieces – needs to be integrated, debugged and commissioned (March)

• **On schedule for April Cosmic Campaign and <u>pre-qualified</u> May LEPS beam test**

Schedule



3+ TOP modules of readout

Install and operate completed modules in Fuji CRT

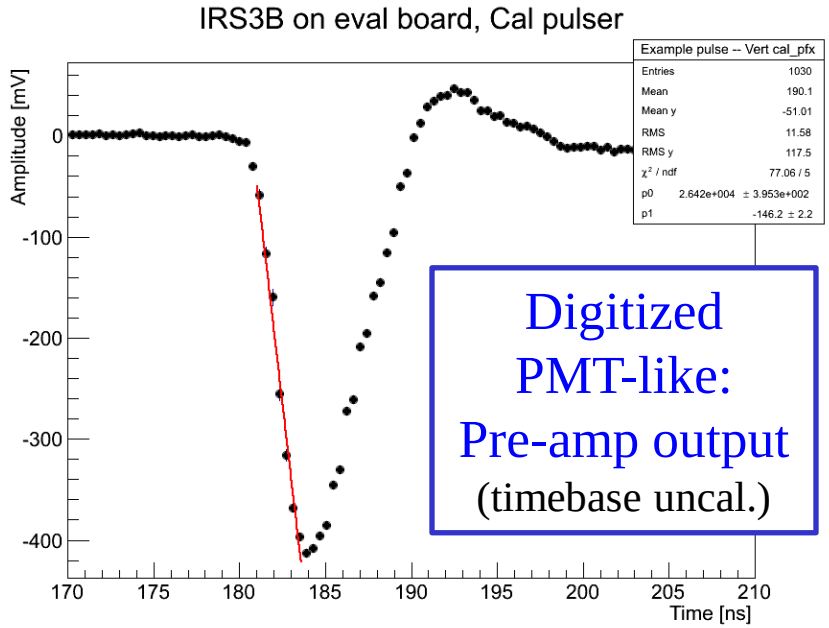
Items Prior to Production

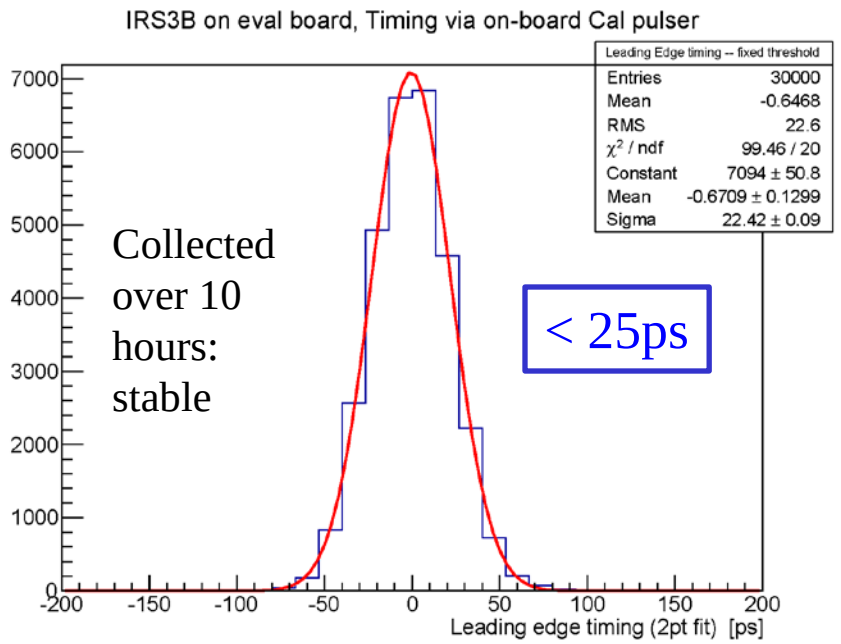
1. ASIC configuration, sampling issues
2. Timebase stabilization (servo-loop)
    1. Firmware needed to be re-written
    2. Improved phase control
3. SCROD module (“final” form factor)
4. Better thermal management (85C redline ops)
5. HV divider redesign
6. Improved SL-10 electro-mech interface
7. Demonstrate DSP (real time) data reduction
8. In-situ (on demand) calibration

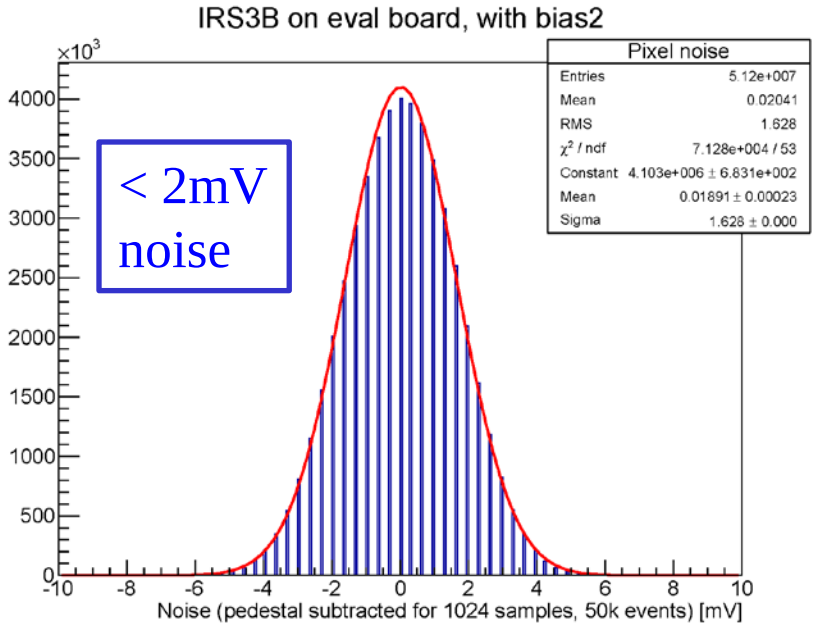
= Demonstrated

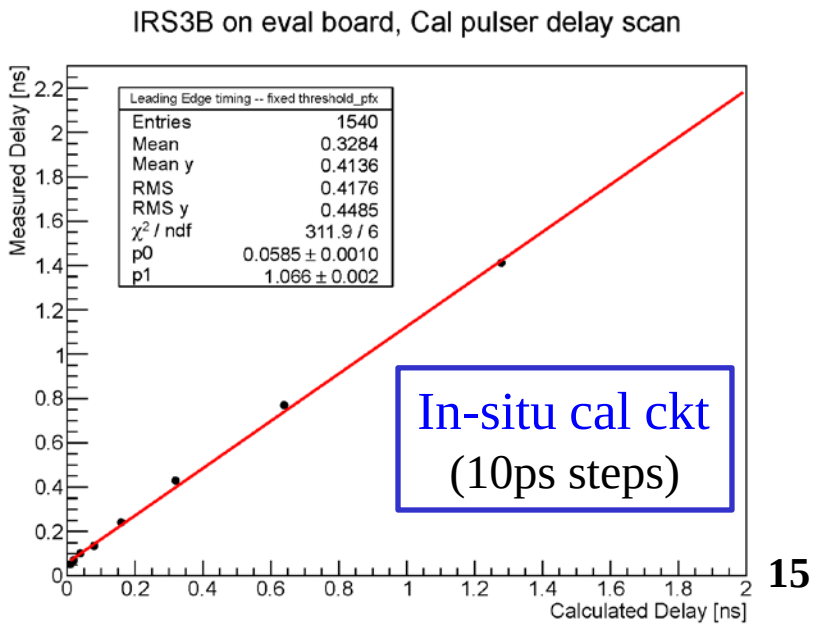
= to be done “pre-production”

IRS3B and Readout working well



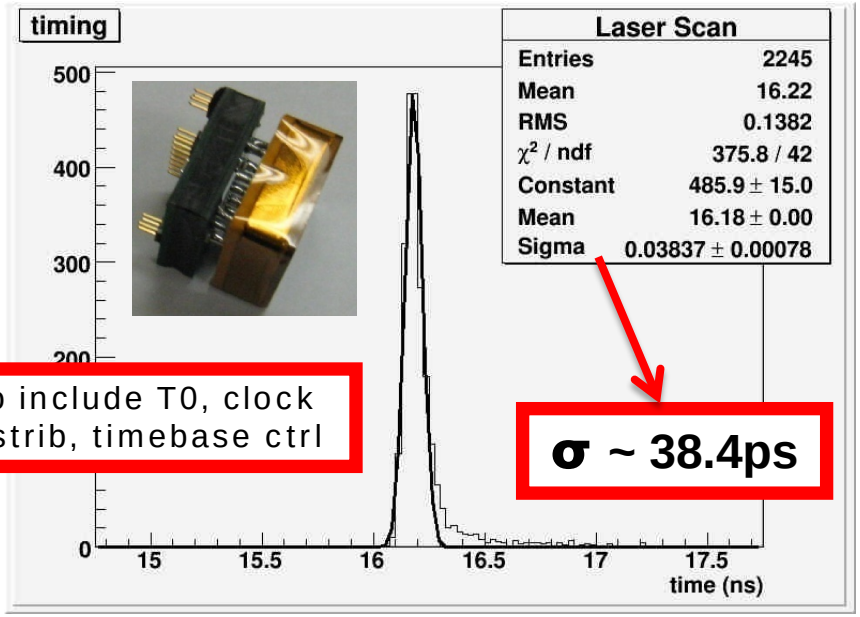


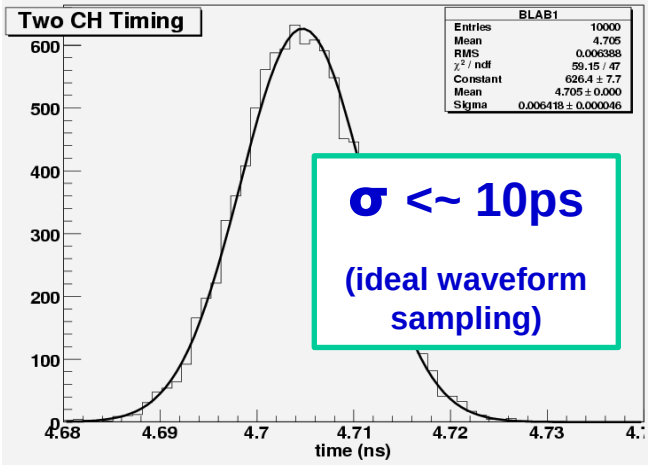




Performance Requirements (TOP)

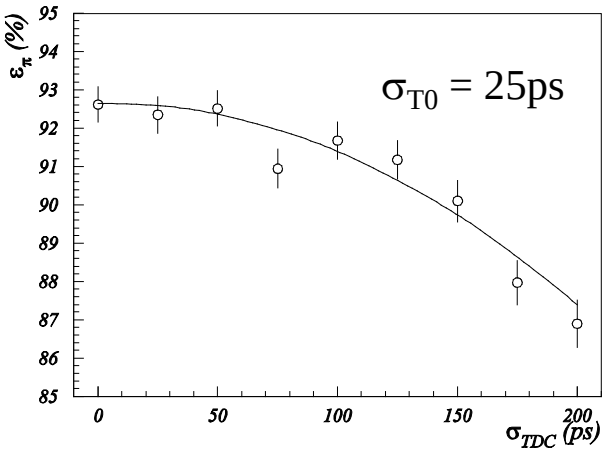
- Single photon timing for MCP-PMTs

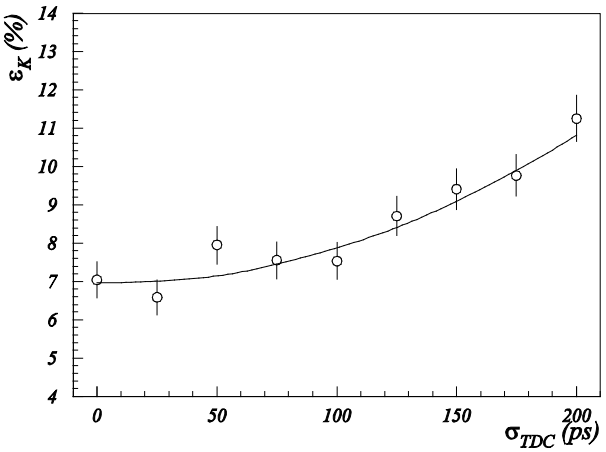




NIM **A602** (2009) 438

σ <= 100ps ➔ 1% impact





σ <~ 50ps target

NOTE: this is single-photon timing, **not** event start-time "T_0"