Integration Report

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Firmware Status

- Clock/trigger distribution and control:
  - FTSW clock/trigger receiver
  - Clock multiplexing to use distributed or local clock
- DAC control.
- ASIC control:
  - Sampling control
  - Digitizing and readout
- ASIC triggering:
  - Scalers for all ASIC channels
  - Trigger bit stream recording
- ASIC feedback:
  - ADC count-rate feedback
  - Sampling rate feedback
  - Trigger width feedback
- Fiberoptic:
  - Basic communication
  - Packet receiver (for commands ➔ board stack)
  - Packet sender (for data ➔ cPCI)
- Auxiliary
  - Temperature readout
  - EEPROM readout (for board-stack ID)

Key:
Green – Integrated and verified functional, may require minor debugging.
Orange – Integrated but still needs features added.
Red – Not integrated or not yet written.

➔ **For initial cosmic ray running, N_{hit} and very coarse timing will be easiest comparisons to MC.**

➔ **Yesterday, first confirmation of real ASIC data readout from front-end through fiberoptic to cPCI crate!**

Still need to integrate command receiver and proper packetizing/formatting of data.

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→ **Lynn working on this now.**

→ **Basic data path now exists, but these will need to be finalized to take any meaningful data.**

Hardware (original plan)

- No significant problems have been found in the low voltage boards.
- Need another version of front-front board.
  - Matt is preparing this.
- Will attempt to leave 3 full board stacks in Nagoya for now, taking some back to Hawaii to assist in debugging.
  - Enough for up to 16 MCP-PMTs, should be adequate for initial running.

Board	# for beam test	# for initial cosmic test	# to remain in Nagoya
SCROD	4	2	3
Interconnect	4	2	3
Carrier0/1/2/3	16	8	12
IRS2_DC revB	64	32	39
front-front	4	2	2
front-back	4	2	2
SL10_HV revA2	4	2	4

Hardware (amended)

- No significant design problems have been found in the low voltage boards.
- Before leaving, tested the following on all boards:
  - (Major) FTSW clock and trigger receiving.
  - (Major) Plausible ASIC data out.
  - (Minor) Trigger bits on each channel of each daughter card responsive.
- A number were found to have issues:
  - Brought back all boards with major faults, left some with minor faults.

Board	# for beam test	# for initial cosmic test	# to remain in Nagoya
SCROD	4	2	3
Interconnect	4	2	3
Carrier0/1/2/3	16 (4,4,4,4)	8 (2,2,2,2)	12 (3,2,2,2)
IRS2_DC revB	64	32	~~39~~ 35*
front-front	4	2	2
front-back	4	2	~~2~~ 4 (1w/bad PMT slot)
SL10_HV revA2	4	2	4

*"wrong" DAC addresses on some…

Documentation / etc.

- As part of moving toward complete system, code-base and documentation is growing:
  - To check out current code:

svn checkout *http*://idlab-scrod.googlecode.com/svn/iTOP-BLAB3A-boardstack/branches/beam_test_or_bust idlab-scrod-read-only
svn checkout *http*://idlab-scrod.googlecode.com/svn/iTOP-BLAB3A-boardstack/branches/pseudo-data_by_fiber idlab-scrod-read-only

  - Documentation is available on wiki:

    http://code.google.com/p/idlab-scrod/w/list

    - Including preliminary hardware setup guide at:

      http://idlab-scrod.googlecode.com/files/bPID_Electronics_Setup.pdf

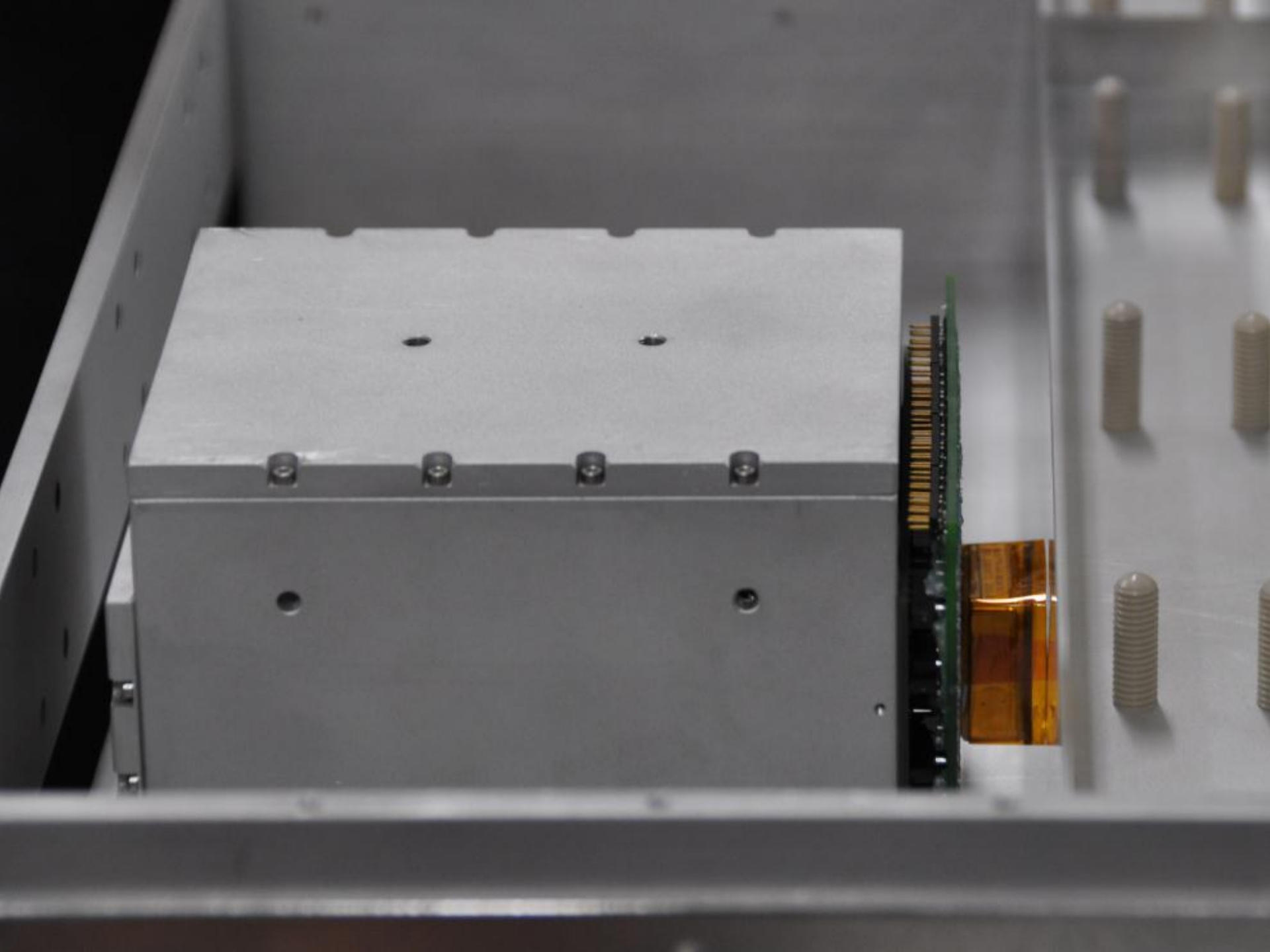
***Matsuoka-san is now trained in hardware setup and minimal data collection. Need to add some more information to this guide (or a separate guide) on operating the DAQ system.**

Mechanics

- (Hours) Before leaving, Nagoya group did a run-through of assembly procedure.
  - Bar <-> Expansion <-> 1 PMT <-> 1 Elec. Module

***Some concerns about this interface…**


Ext-Bwd



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