

6

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E

E

differences between revA and revB
 removed 3 debugging headers and cut board to allow for cat7 cables to click in place
 removed all 4 mounting holes
 added 6 test points to probe DC voltages
 added copper pours to top and bottom layers connected to ground on the sides of the board to allow for maximal thermal contact with aluminum frame (included soldermask keepout there)
 moved power connector closer so board extent could be reduced
 re-routed several traces that were in the 2mm side-edge for the aluminum frame
 added note to SCROD schematic decal showing which nets were GCLK nets on SCROD's FPGA
 fixed typo in SCROD schematic decal
 added vias and thickened traces around voltage regulators
 added a few vias to power/ground nets feeding J2 on top of board
 added silkscreen to top of board so it's easier to know which connector on SCROD is which
 moved inner power planes away from edge of board
 added connector part number on schematic decal for SCROD
 renamed DAC1..DAC8 on SCROD schematic decal
 added many stitching vias to edge copper pours to promote thermal conductivity to aluminum frame
 renamed J1..J4 on SCROD schematic decal to reduce confusion when soldering

D

D

C

C

B

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A

A

institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	interconnect
revision:	B
IDLAB design #:	IDL_11_033
circuit design:	LJR, MZA, GSV
PCB design:	LJR, MZA
sheet #:	1 of 4
sheet description:	TOP Block
date last modified:	2011-10-09

notes updated 2011-10-09

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E

E

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D

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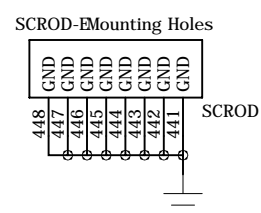
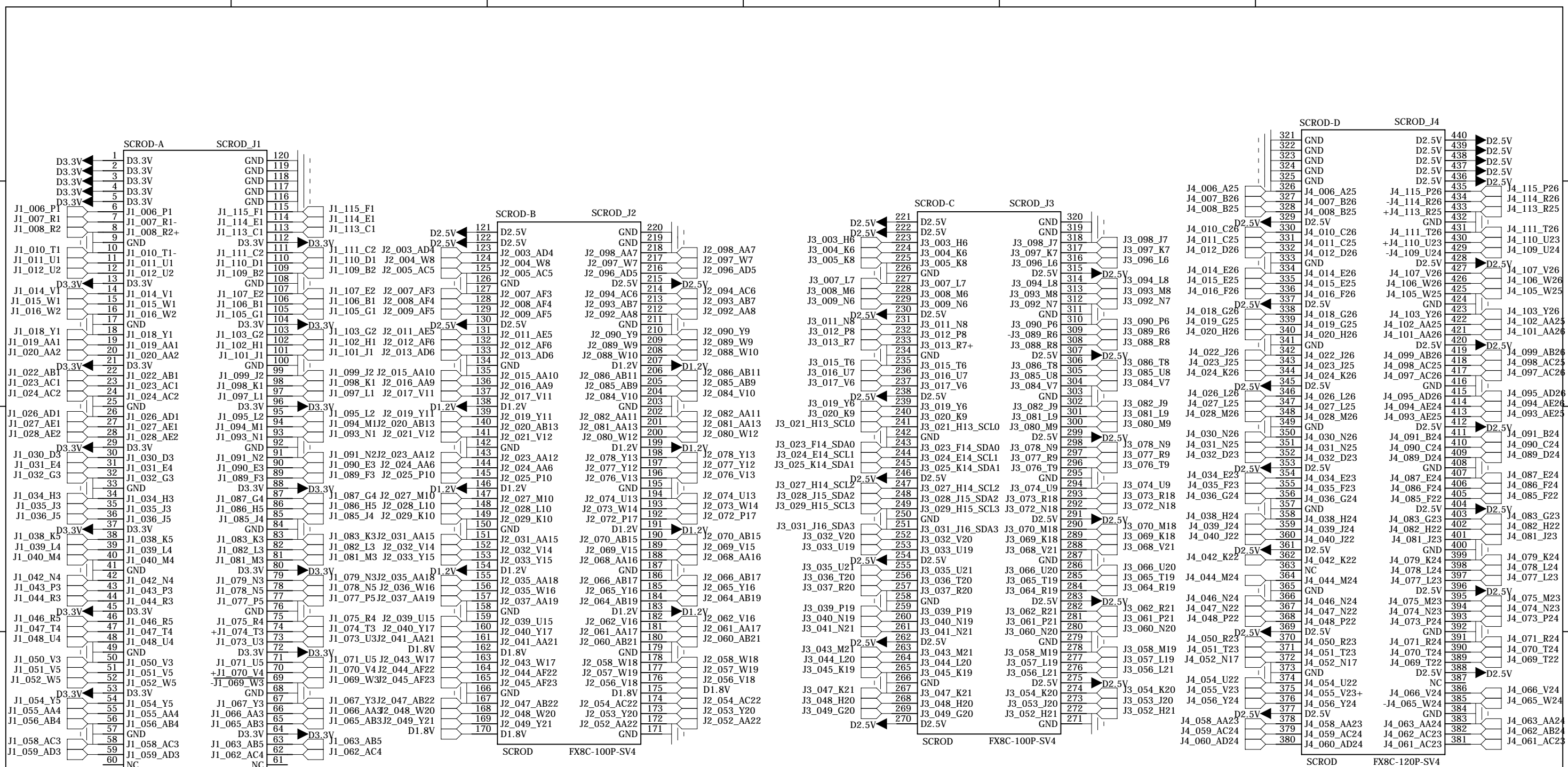
C

B

B

A

A



institution: University of Hawai'i at Manoa
 High Energy Physics Group
 Instrumentation Development Lab

title: interconnect
 revision: B
 IDLAB design #: IDL_11_033
 circuit design: LJR, MZA, GSV
 PCB design: LJR, MZA

sheet #: 2 of 4
 sheet description: SCROD Interface
 date last modified: 2011-10-09

E

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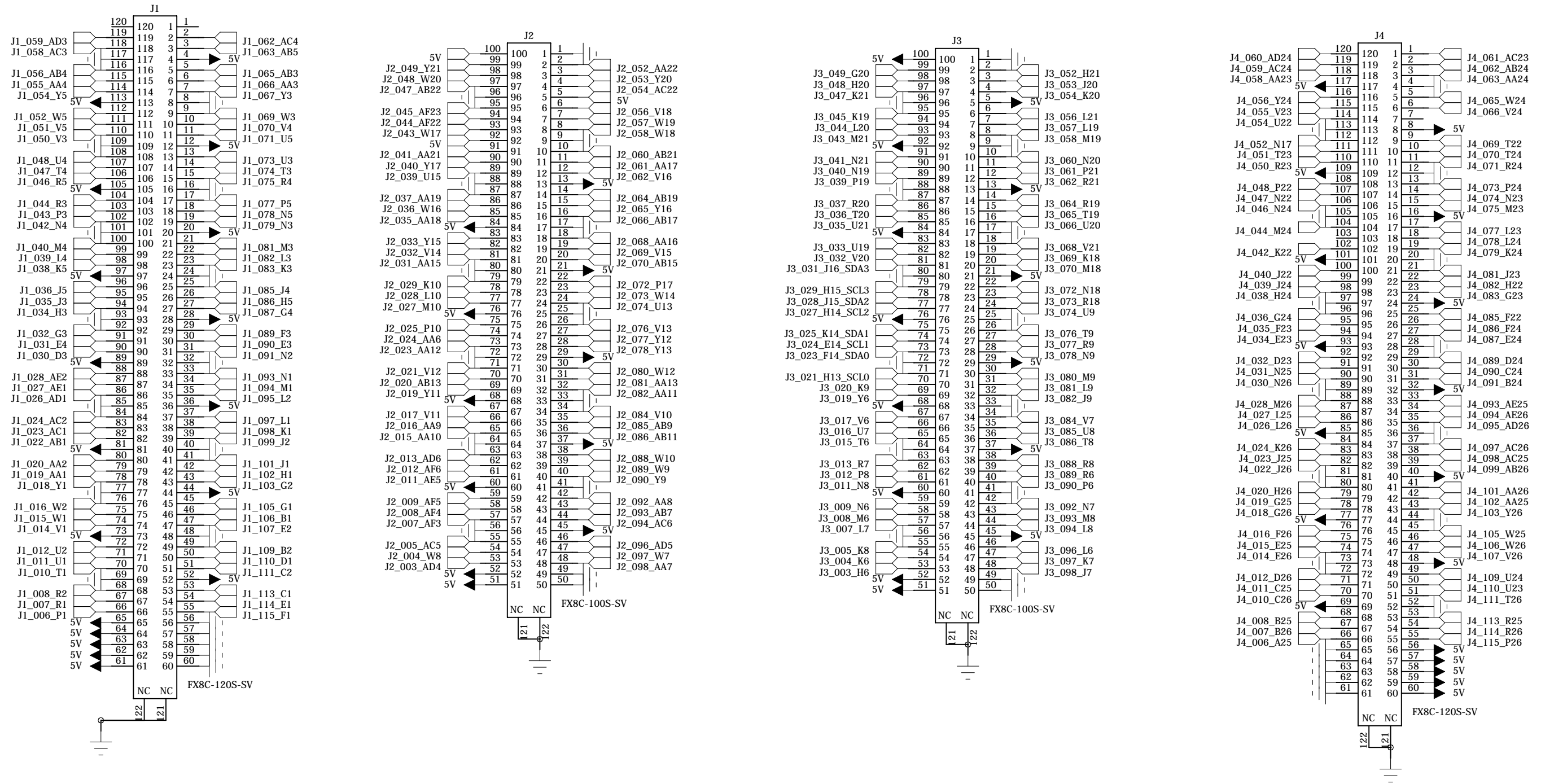
E

D

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B

A



institution: University of Hawai'i at Manoa
 High Energy Physics Group
 Instrumentation Development Lab

title: interconnect
 revision: B
 IDLAB design #: IDL_11_033
 circuit design: LJR, MZA, GSV
 PCB design: LJR, MZA

sheet #: 3 of 4
 sheet description: ASIC Interface
 date last modified: 2011-10-09

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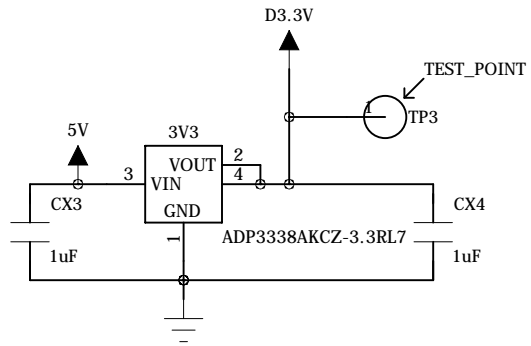
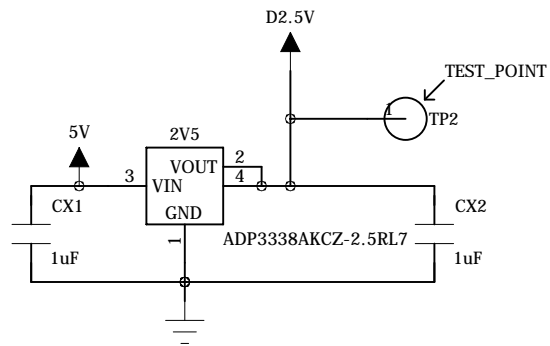
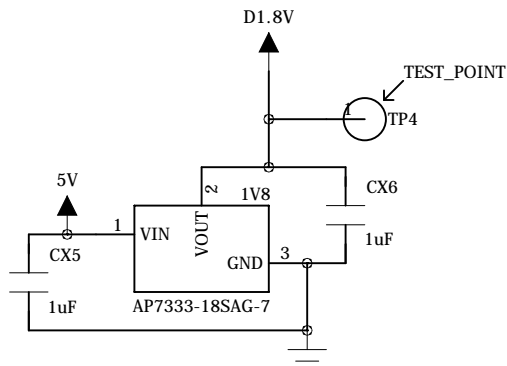
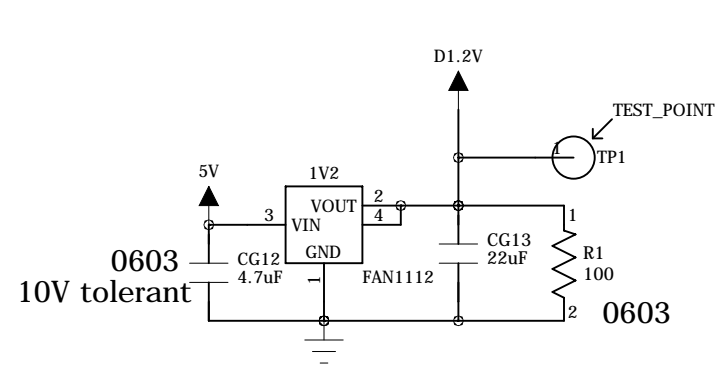
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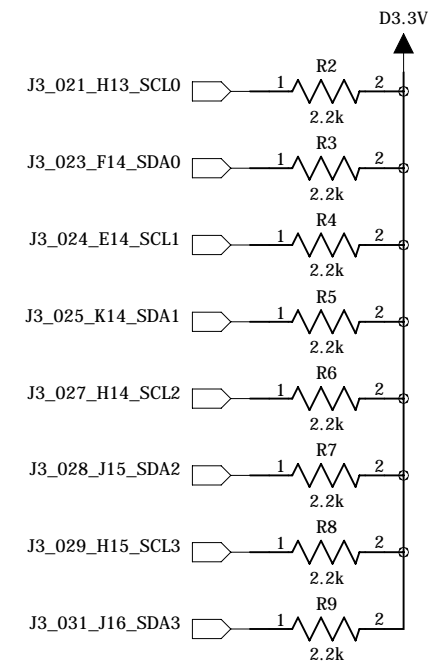
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D



I²C pull-ups for DACs



0402

C

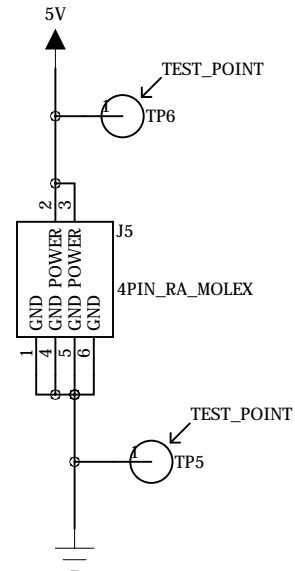
C

B

B

A

A



institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	interconnect
revision:	B
IDLAB design #:	IDL_11_033
circuit design:	LJR, MZA, GSV
PCB design:	LJR, MZA
sheet #:	4 of 4
sheet description:	Power
date last modified:	2011-10-09