1 SL10 'front board' HV Traces

First, I made a scaled drawing of eight SL10 PMTs (Figure 1), placed as they will be in iTOP.

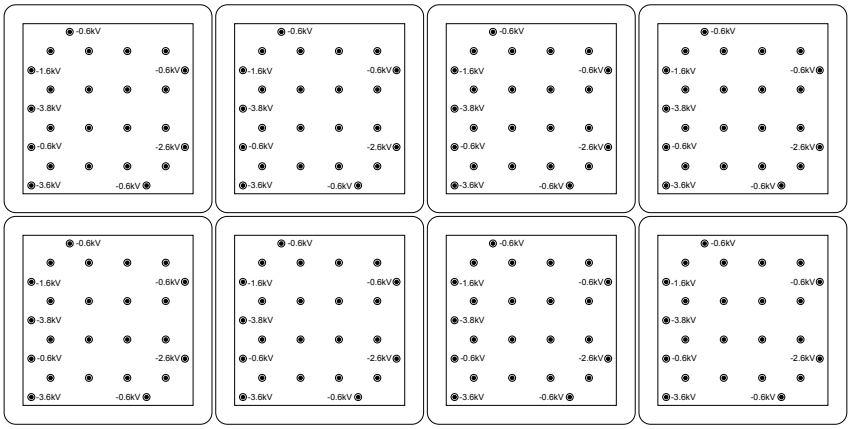

Figure 1: eight SL10s

Then, I overlaid keepout discs using the recommended $0.1"/kV$ of spacing for high-voltage traces (relative to ground potential). The result (Figure 2) is that routing the board would be nigh impossible.

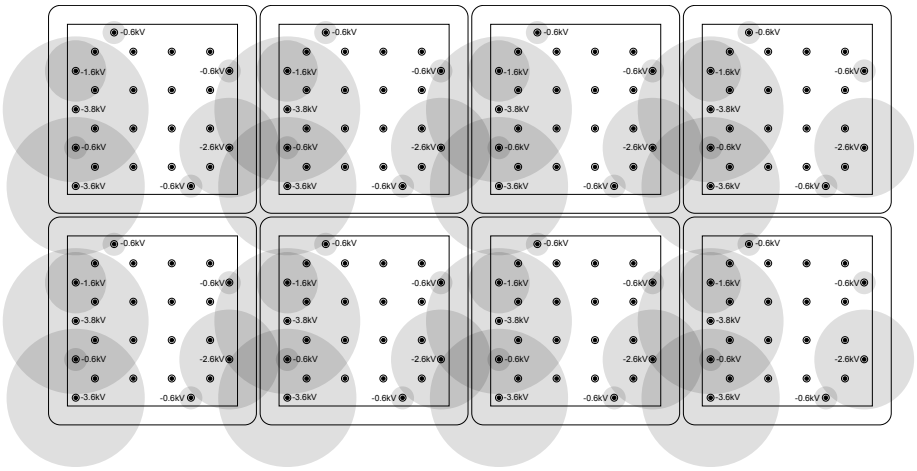

Figure 2: eight SL10s with $0.1"/kV$ HV trace spacing (relative to ground) on same layer

If we 'renormalize,' however, and take $0.033"/kV$ as the actual 'safe' HV keepout (as Hamamatsu's SL10 has $3.8kV$ on a pin that is .119" from an anode pin), the result (Figure 3) looks much more likely to be routable.

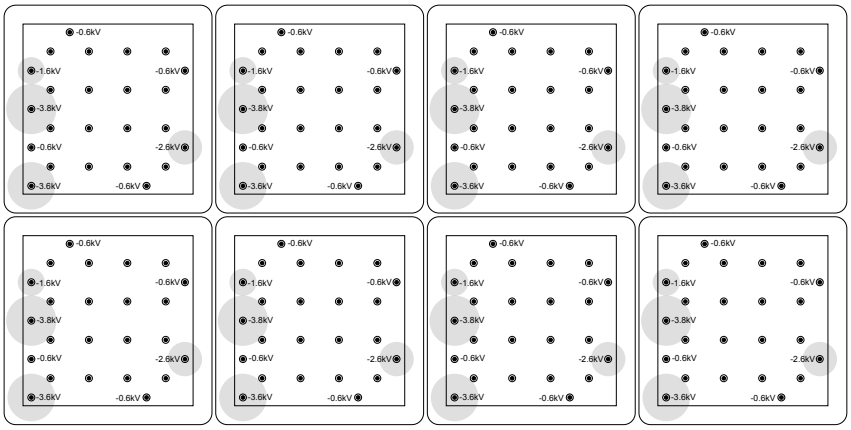

Figure 3: eight SL10s with 0.0345"/kV HV trace spacing on same layer

After getting this, I used the whiteboard to try to get some idea of how the routing would look and if the traces will violate this relaxed rule. Figure 4 shows a potential routing idea; the green circles are anode pins; the orange circles are HV pins; dimensions in blue show the closest point of approach of high voltage on a given layer (and the voltage difference); other lines are traces on different copper layers.

After a couple tries, I rotated the PMTs so most of the HV terminals were facing 'up,' which simplified the routing for the top row at least. The only remaining thing was to route the HV for the bottom row of PMTs in between the PMTs on the top row. The result (Figure 4) is that, if we have at least a 6 layer board, we can squeak the traces by the top PMTs. The multicolor traces in the drawing that bring the HV from bottom to top are supposed to overlap exactly, and depending on the required trace thickness, there will be a relatively generous HV trace spacing of 0.059"/kV (3.8kV twice over 0.451"). Gary, do you think this is acceptable?

2 SL10 'front board' Signal Traces

Next, planning for the signal traces on the 'front board' took place. Figure 5 shows two possible orientations of the SL10 and the possibilities of where the 16 pin 2mm connector can fit.

Using board-stack connectors with 6mm height (as was the plan) causes conflicts if we stick to the 2mm pitch connectors to get signals from the 'front board' (Figure 6).

Without significant (board redesign) effort, we can use different height board-stack connectors. Figure 7 shows that this does not resolve the conflicts.

All board-stack connectors don't have to be the same height. If we loosen that constraint, we find that there is no solution that fits inside the Belle detector

that does not cause conflicts between pins. Figure 8 shows that the only solution is if we let the connectors become available in half-millimeter sizes (which is not true). Also, there is no longer space for the high voltage components nor required space for cooling pipes on the HV board.

The only solution seems to be to go to a different connector to go between the 'ASIC carrier' and the 'front board'.

One such option is a 17 pin staggered $1mm$ pitch connector which would interdigitate ground with the signals on each connector (Figure 9). One benefit of this connector is that it will lay at a right angle to the 'front board,' whereas other single-row connectors would not. Another benefit is that with the interdigitization, the signal pins have the same pitch ($2mm$) as the existing 'ASIC carrier' boards, so some soldering magic could allow us to use the existing 'ASIC carrier' boards. A third benefit is that this is a surface-mount connector, so no extra holes need be drilled in the 'front board' that will complicate HV routing. One drawback is that the mating female connector will not necessarily come off the 'ASIC carrier' board at a right angle like the 'end-fire' $2mm$ connectors (sort-of) do.

If, however, we look at a different view of the same board-stack, we find that the situation is worse. Figure 10 shows that the $2mm$ connector pads on the 'ASIC carrier' / 'BLAB3A carrier' boards are not lined up with the PMTs, which causes pin conflicts in another dimension (also see Figure 11).

Alas, it seems that not even the 2011 beam test version of our iTOP electronics will be able to use the 'ASIC carrier' boards we have already designed (and in one case fabricated). Any ideas anyone has on how to correct this are welcome.

mTC might still be able to use the existing boards. Further study would have to be conducted to know for sure.

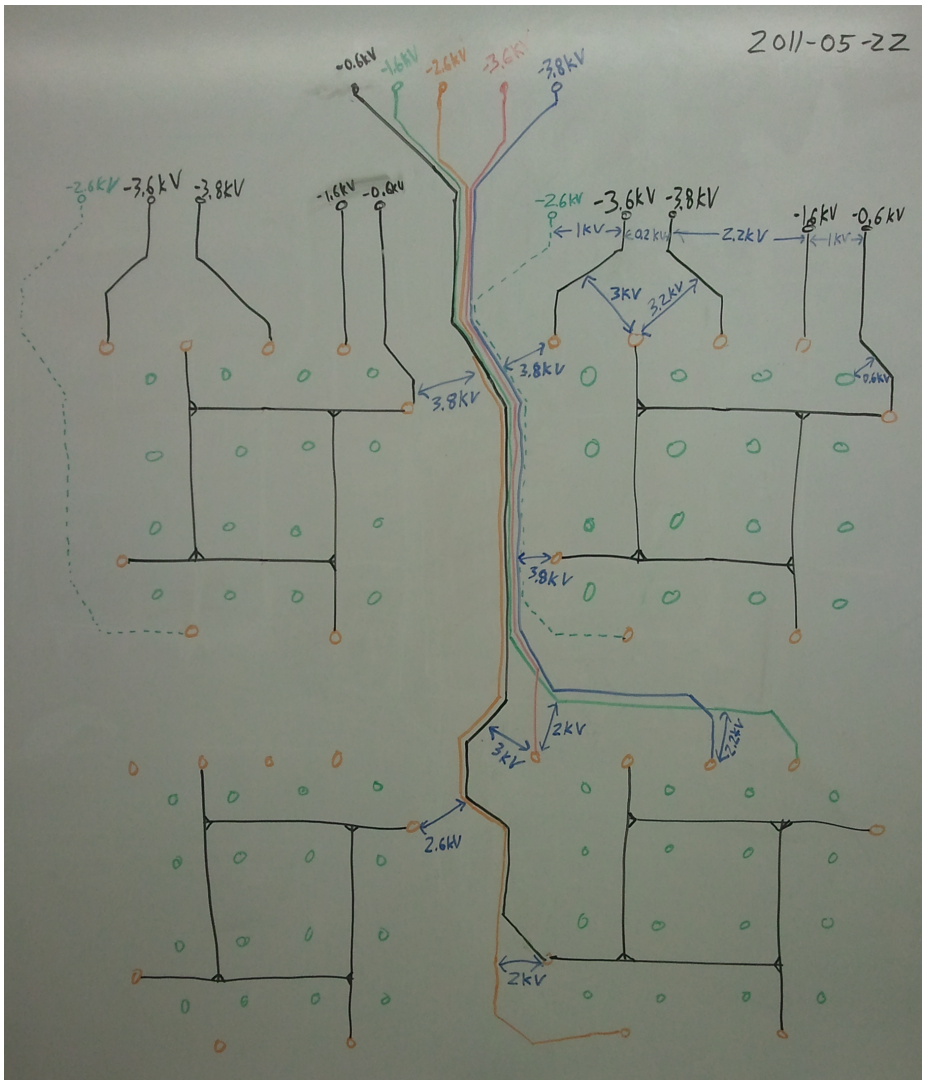

Figure 4: potential 'front board' HV trace routing

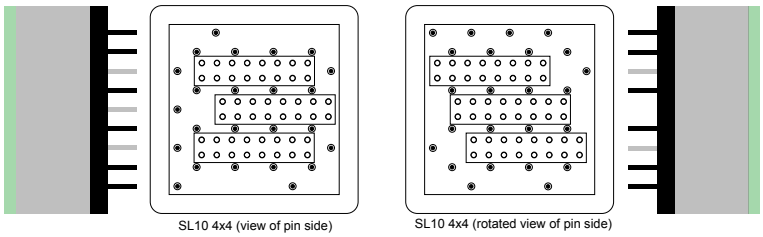

Figure 5: two orientations of an SL10 showing the various places 16 pin $2mm$ pitch connectors can fit

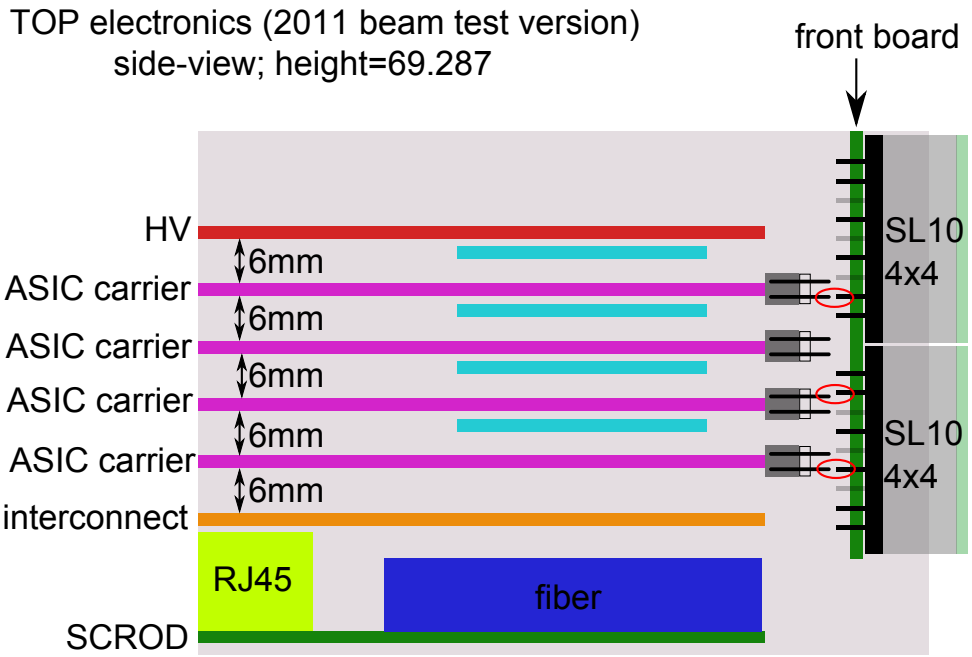

Figure 6: side view of single iTOP electronics module with $6mm$ board-stack connectors, showing mechanical conflicts with SL10 pins (conflicts indicated in red)

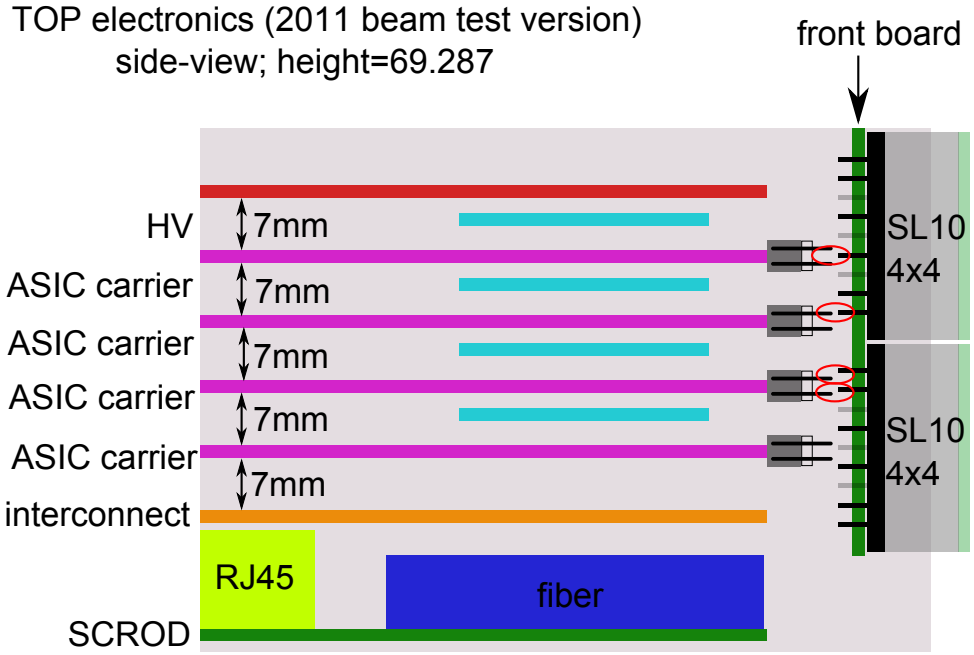

Figure 7: side view of single iTOP electronics module with $7mm$ board-stack connectors; the conflict is not resolved (conflicts indicated in red)

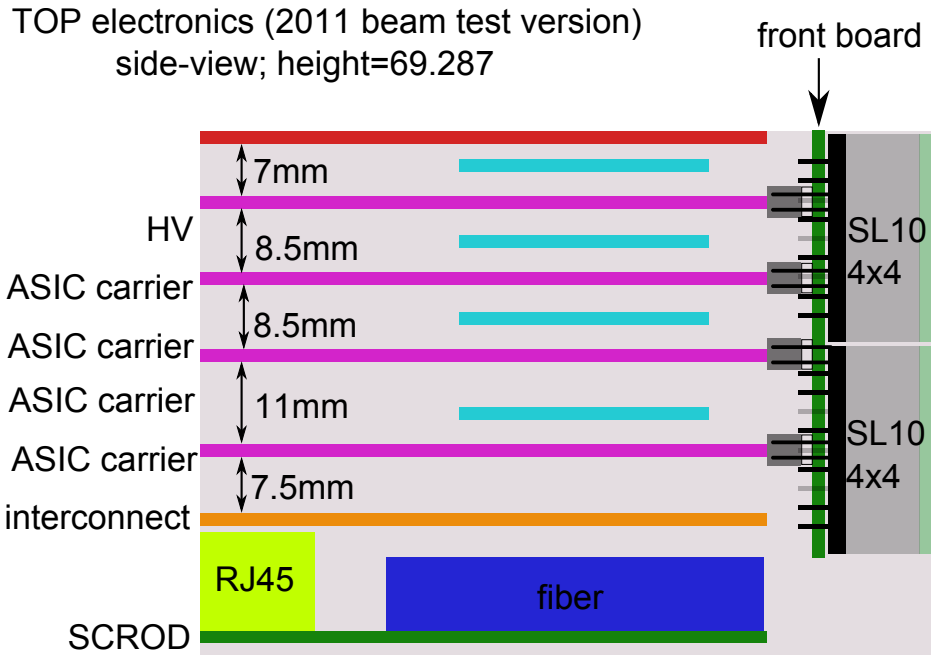

Figure 8: side view of single iTOP electronics module with various height board-stack connectors; the conflict is resolved, but the connectors do not exist

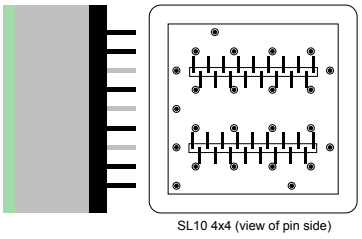

Figure 9: SL10 with a pair of 17 pin staggered $1mm$ pitch connectors

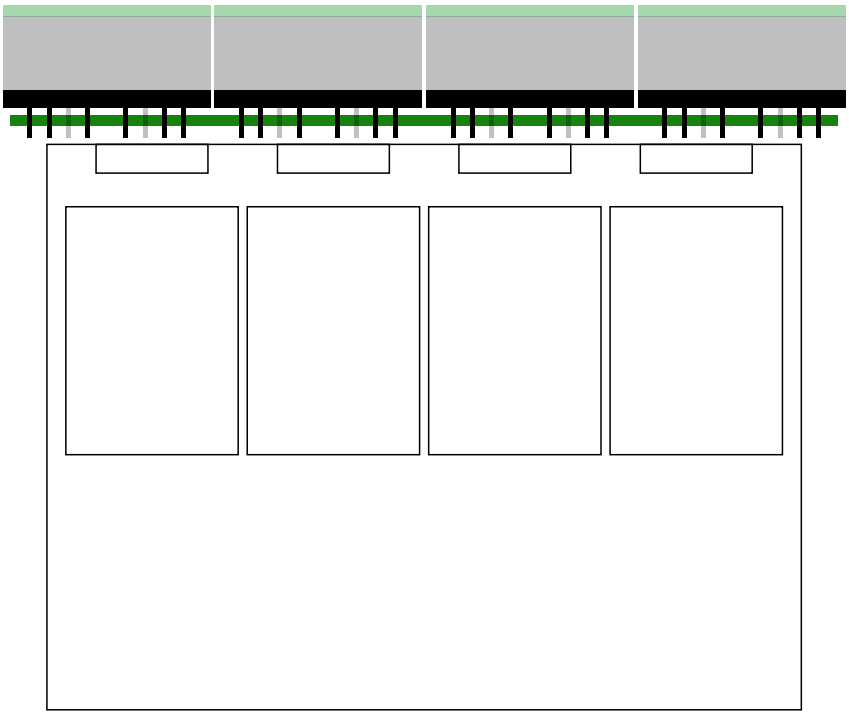

Figure 10: top view of single iTOP electronics module showing that the existing $2mm$ connector pads do not line up with the PMTs

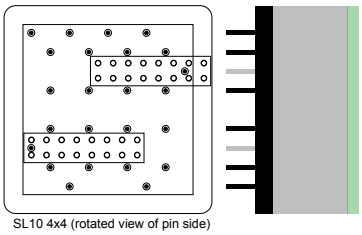

Figure 11: view of SL10 with 16 pin $2mm$ connectors showing conflict between signal and HV pins, causing HV shorts and mechanical conflict with $2mm$ connector housing