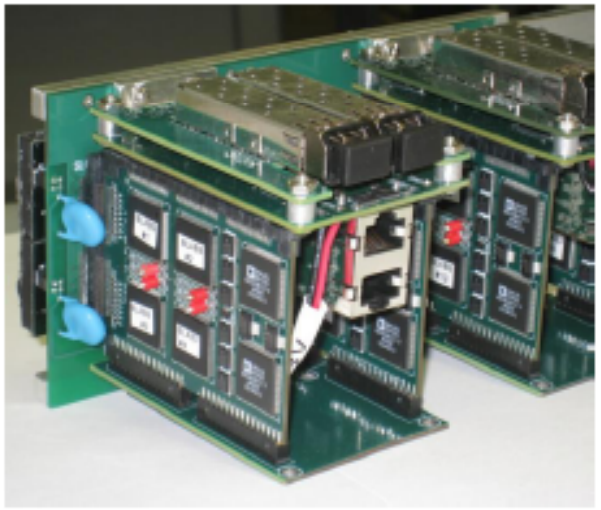
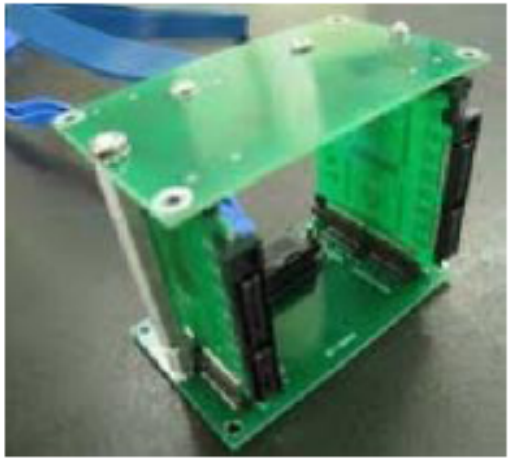
Readout Electronics – K. Nishimura (Hawai'i)

Disadvantages of Existing Board Stack

- BLAB3 issues:
  - Replacement requires re-soldering.
  - Calibration requires a front board adapter to inject test signals.
- Firmware issues:
  - No on-board clock: need clock distribution to test any firmware.
  - Fiberoptic readout only: need back-end working to verify any data out.
- Size issues:
  - Significant amount of wasted space.
  - Existing modules (top right) are too big for Belle II.
  - Split module (lower right) where transceivers are separated from digitizers might meet size restrictions, but this is untested and may not preserve signal fidelity.





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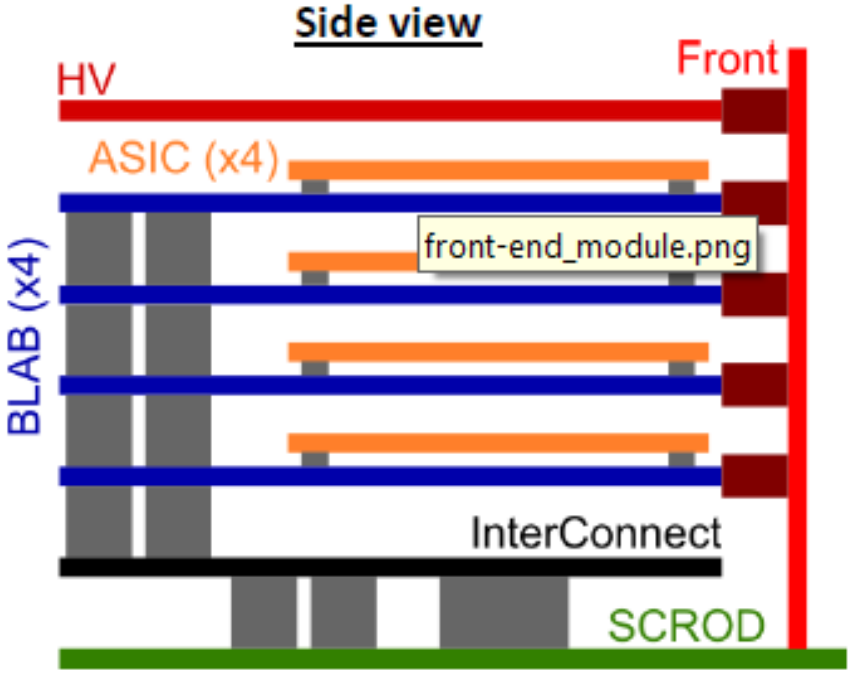
New Front-end Board Stack



= board-to-board connectors

Front
- Connects HV board to PMTs
- Connects PMT output to ASIC input

HV
- High voltage components for PMTs
- Cooling for high voltage components

Standard Control, Read-Out, Data (SCROD)
- FPGA (ASIC control)
  - Virtex4, Spartan6
- 2 Fiber transceivers
- 2 RJ45
  - Clock Distribution
  - LVDS (JTAG)
- Mini USB – for easy bench testing

Digitizer Boards (BLAB)
- Carrier card for ASICs
  - 4 ASIC daughter cards per carrier
- ASIC in-situ testing components
  - e.g., pulser for channel checks

ASIC
- 1 BLAB3 per card
- DACs

Interconnect Board
- Connects SCROD & BLAB
  -Layout of connectors are forced to be unique because of size constraints
- Power regulation/distribution

K. Nishimura (Hawai'i)

New Front-end Board Stack

Mechanical Mockup – Isometric View

Front
- Connects HV board to PMTs
- Connects PMT output to ASIC input

HV
- High voltage components for PMTs
- Cooling for high voltage components

Sto
- FP
-
- 2
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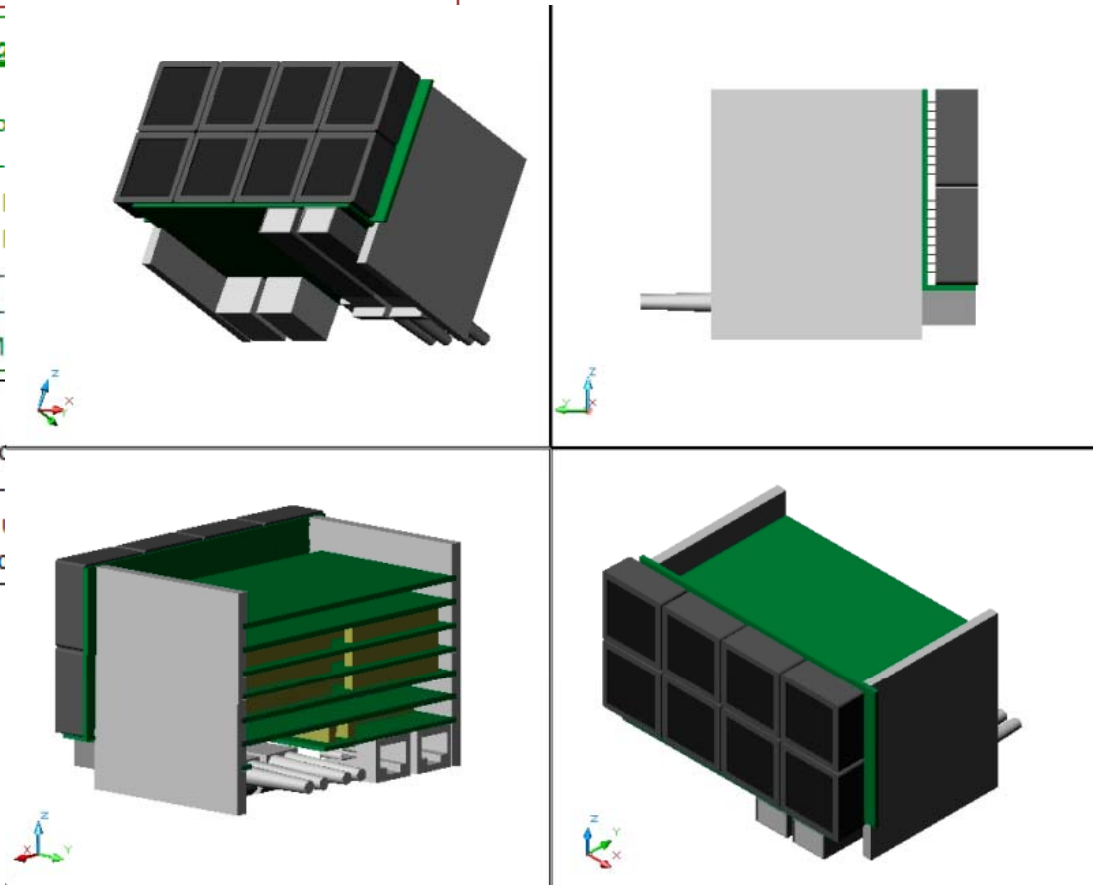
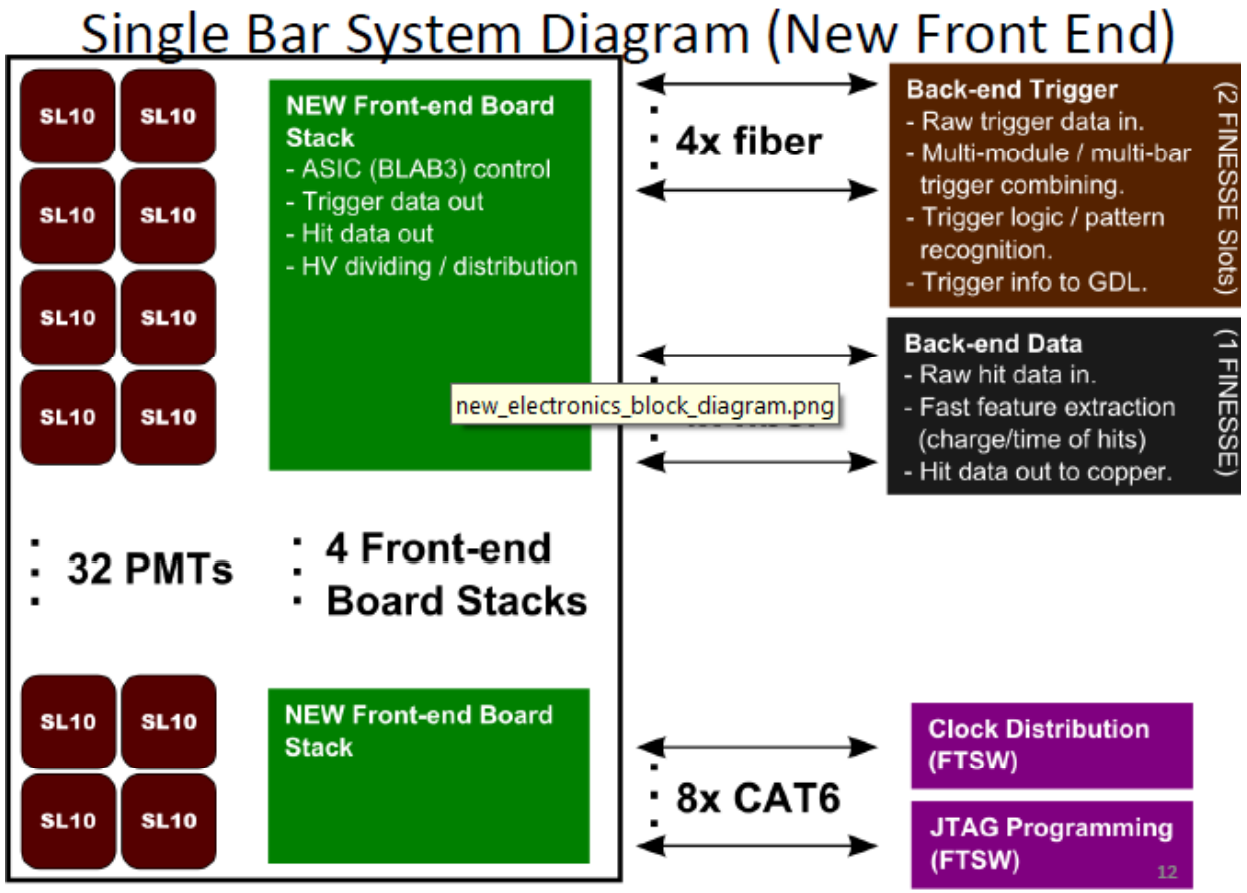


Digitizer Boards (BLAB)
- Carrier card for ASICs
  - 4 ASIC daughter cards per carrier
- ASIC in-situ testing components
  - e.g., pulser for channel checks

ASIC
- 1 BLAB3B per card
- DACs for bias voltages

- Co
-
be
- Po



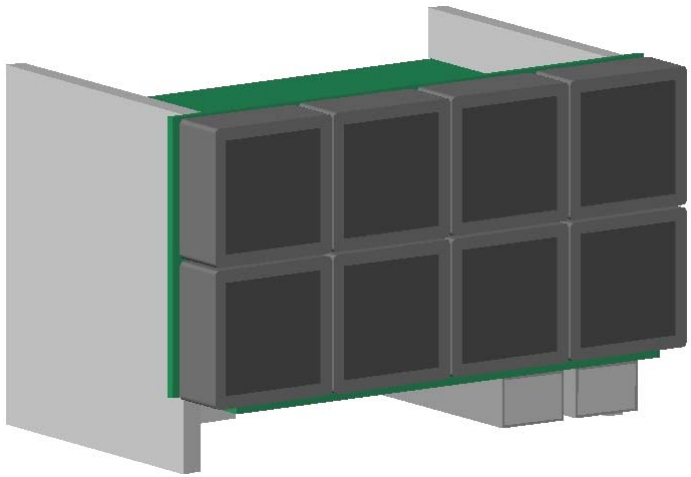
•Remaining system pieces are being developed/tested.

–Changes to front-end don't significantly impact other elements (actually require fewer numbers of boards on back-end).

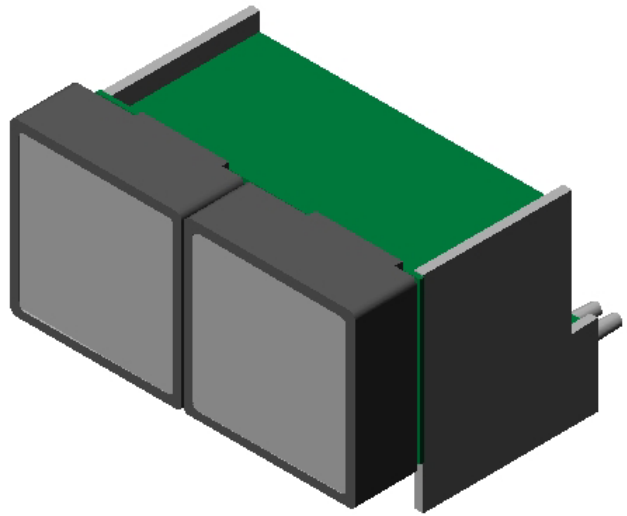
•Calibration studies in Hawaii are ongoing in preparation for the arrival of the next round of ASICs.

FEE under development: parallel effort with Belle II

Belle II bPID FEE module: based on a 2 x 4 array of Hamamatsu SL-10 MCPs with a 4x4 anode structure (16ch per PMT).



mTC FEE module: based on a 1 x 2 array of Planacon MCPs with a 8x8 anode structure (64ch per PMT).



- Both of these FEE modules are being developed in parallel.
- Each module provides 128 readout channels.
- **Five of seven PCBs are common to each module.**