

CDC Trigger Merger

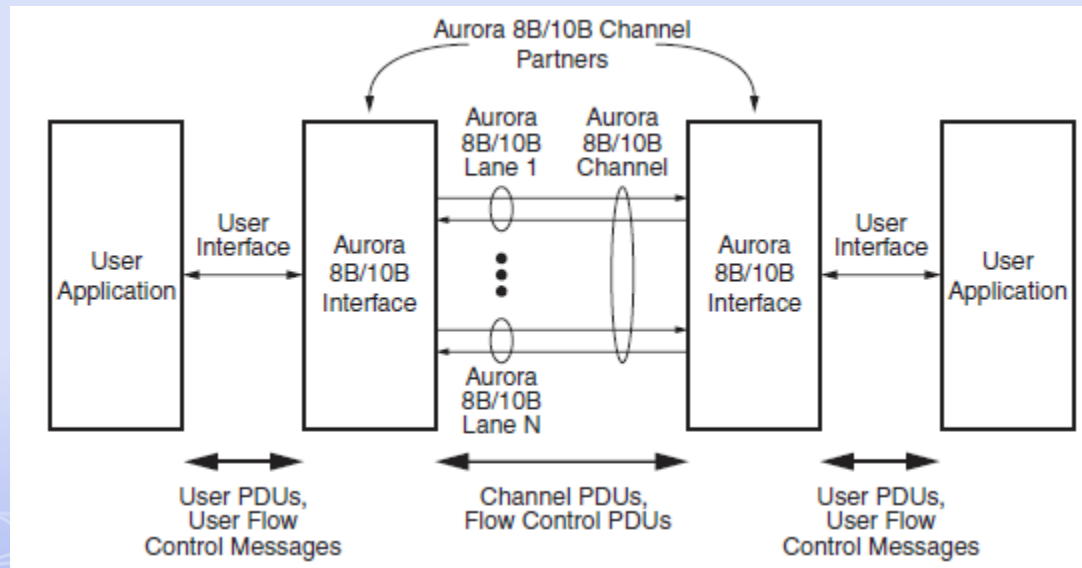
Shih-Min Liu; Alan, Teng; C.H. Wang
NUU, Taiwan

Outline

- ❑ Multi-lane Aurora protocol in Altera
- ❑ Aurora protocol link test results
- ❑ Merger prototype
- ❑ Summary

Multi-lane Aurora Protocol in Altera

- multi-lane can be combined as one Aurora channel to use.



- ❑ Multi-lane structure in Xilinx and Altera
 - Deskew FIFO in Altera transceiver can't be used in basic mode, so we add our Deskew FIFO.

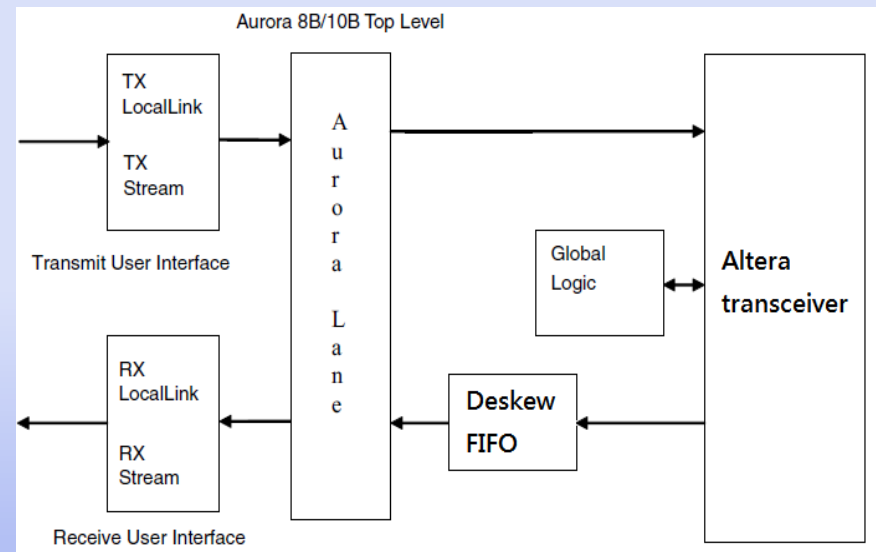
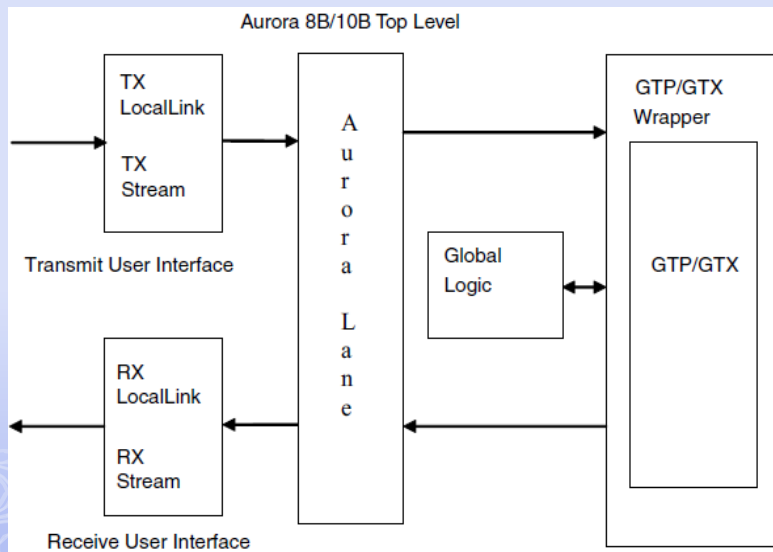


Figure 1–58. Deskew FIFO—Lane Skew at the Receiver Input

Lane 0	K	K	R	A	K	R	R	K	K	R	K	R
--------	---	---	---	---	---	---	---	---	---	---	---	---

Lane 1	K	K	R	A	K	R	R	K	K	R	K	R
--------	---	---	---	---	---	---	---	---	---	---	---	---

Lane 2	K	K	R	A	K	R	R	K	K	R	K	R
--------	---	---	---	---	---	---	---	---	---	---	---	---

Lane 3	K	K	R	A	K	R	R	K	K	R	K	R
--------	---	---	---	---	---	---	---	---	---	---	---	---

Lane Skew at Receiver Input

Lane 0	K	K	R	A	K	R	R	K	K	R	K	R
--------	---	---	---	---	---	---	---	---	---	---	---	---

Lane 1	K	K	R	A	K	R	R	K	K	R	K	R
--------	---	---	---	---	---	---	---	---	---	---	---	---

Lane 2	K	K	R	A	K	R	R	K	K	R	K	R
--------	---	---	---	---	---	---	---	---	---	---	---	---

Lane 3	K	K	R	A	K	R	R	K	K	R	K	R
--------	---	---	---	---	---	---	---	---	---	---	---	---

Lanes are Deskewed by Lining up the "Align"/A/ Code Groups

Aurora Protocol Link Test

□ 1 channel 1 lane

Data rate	Altera chip feedback test	Link test with Xilinx chip
2.5 Gbps	Successful	Successful
3.125 Gbps	Successful	Successful
5 Gbps	Successful	Successful
6.25 Gbps	Successful	Successful

□ 1 channel 2 lane

Data rate	Altera chip feedback test	Link test with Xilinx chip
5 Gbps	Successful	Successful
6.25 Gbps	Successful	Successful

□ 1 channel 4 lane

Data rate	Altera chip feedback test	Link test with Xilinx chip
6.25 Gbps	Testing	Testing

1 channel 4 lane Aurora protocol in Altera system is still testing, we need to make it work more stable.

Merger Prototype

- ❑ Chip : Altera Arria II GX
 - EP2AGX95EF29I3N
 - Limited ECC function
- ❑ Buffer
 - 128M bits or more, DDR or DDRII
- ❑ I/O :
 - 3.125G transceiver *8(Optical connector)
 - 6.25G transceiver *2 (Optical connector)
 - 6.25G transceiver *2 (SMA)
 - Button(System reset, Aurora reset, test option)
 - LED Indicator(link status, error detect)
 - TTL,LVDS signal(flexible test I/O)

□ Clock source

- 50MHz system clock on board
- 156.25MHz MGT clock on board
- 1~2 external clock input

□ Down-load

- JTAG
- USB-blaster chip, Ethernet-blaster chip on board
- Remote upgrade system(TCP/IP)

□ Power supply

- 5V,12V DC input
- Transformer module on board

Summary

- ❑ Aurora protocol link test will be finished soon.
- ❑ We are currently working on the prototype boards design and layout . We plan to have them in Oct.
- ❑ The final Altera Arria V chips should be available in the end of this year.
- ❑ Another prototype with Arria V is planned early next year.