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**High Energy Physics Group  
Instrumentation Development Laboratory**  
2505 Correa Road, Honolulu, HI 96822

**Production Documentation for:**

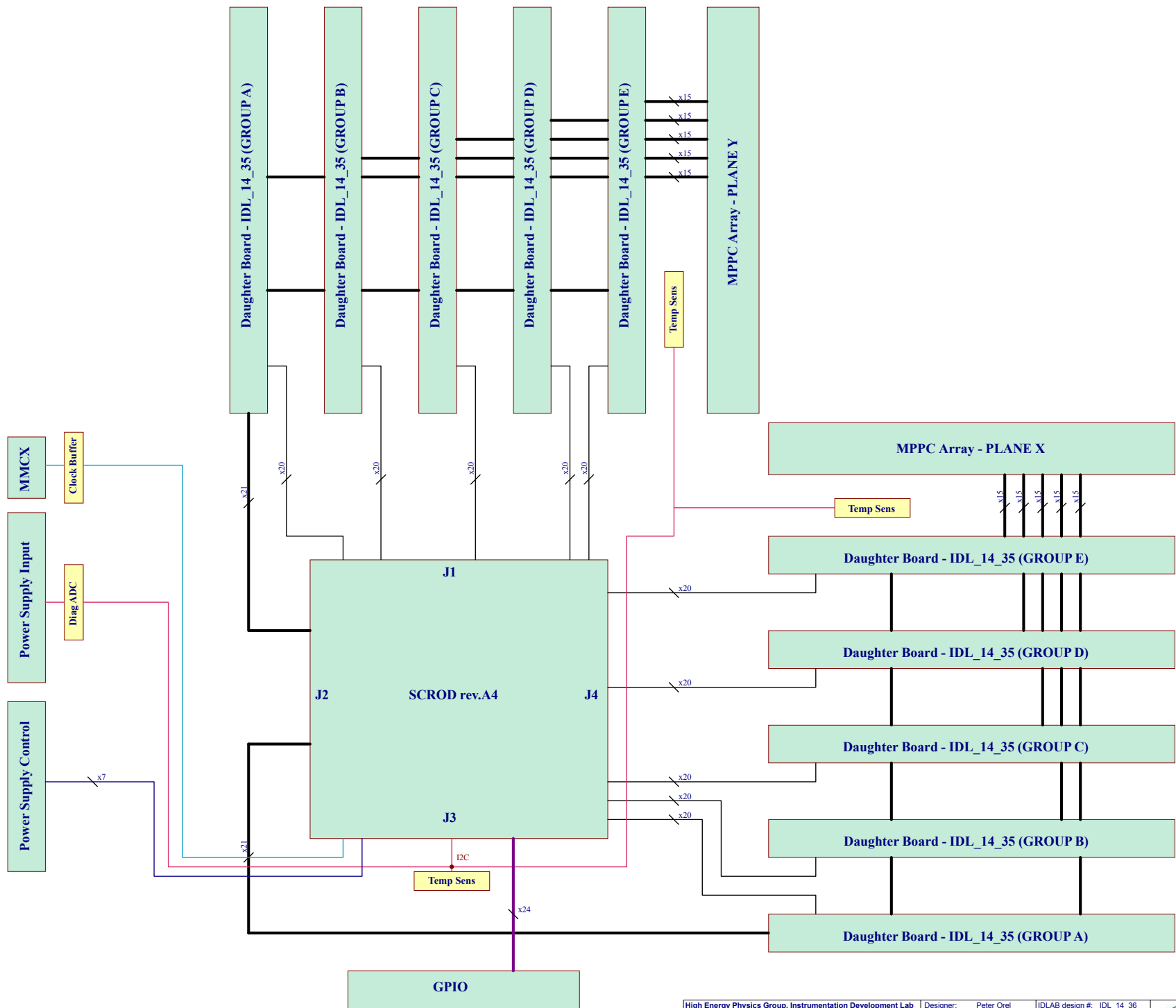
**Project Name:** Compact SciFi Tracker  
**Board Name:** MB\_SciFi\_Tracker  
**IDL num:** IDL\_14\_36  
**Revision:** C  
**Variant:** [No Variations]



High Energy Physics Group, Instrumentation Development Lab	Designer: Peter Orel	IDLAB design #: IDL_14_36
Project: MB_SciFi_Tracker	Drawn By: Peter Orel	Revision: C
	Approved By: Gary S. Varner	Variant: [No Variations]
Sheet Title: Mother Board for Compact SciFi Tracker	Modif. Date: 10-Oct-14	
	Sheet 1 of 11	



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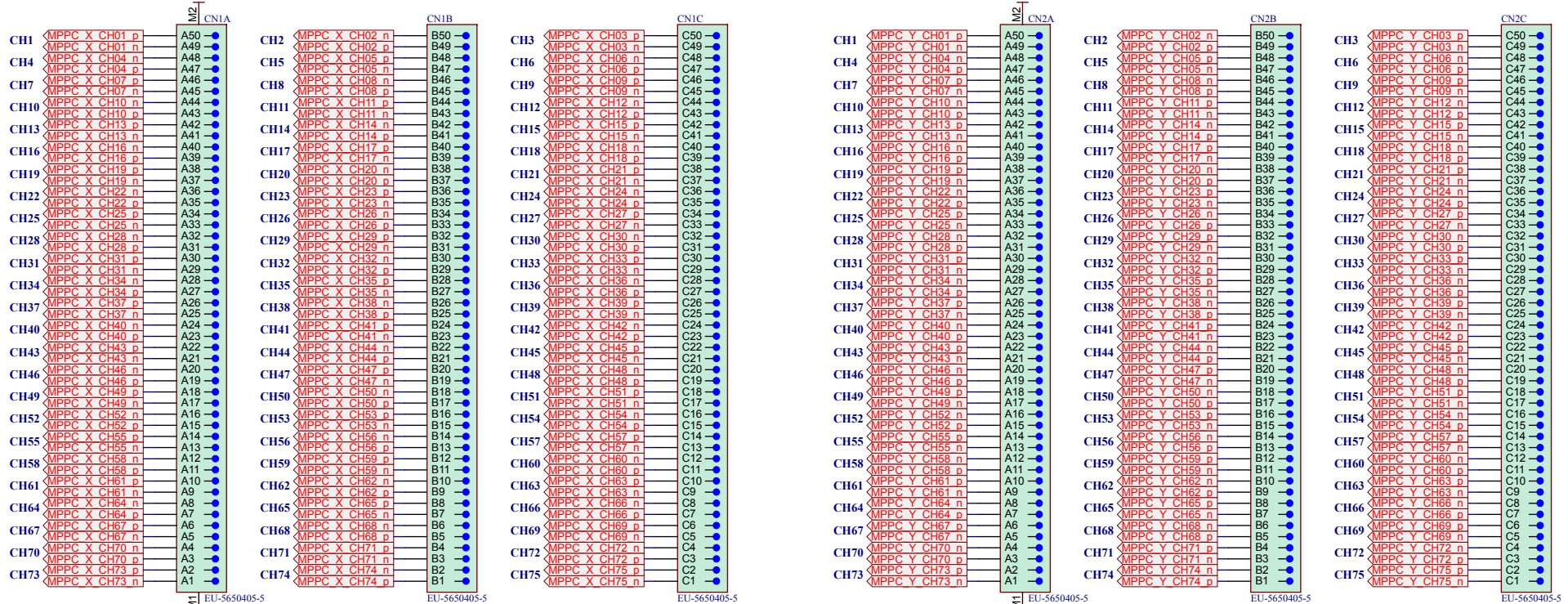
High Energy Physics Group, Instrumentation Development Lab		
Designer:	Peter Orel	IDLAB design #: IDL_14_36
Project:	<b>MB_SciFi_Tracker</b>	Revision: C
Drawn By:	Peter Orel	Variant: [No Variations]
Approved By:	Gary S. Varner	Modif. Date: 10-Oct-14
Sheet Title:	<b>Functional Schematic</b>	Sheet 2 of 11



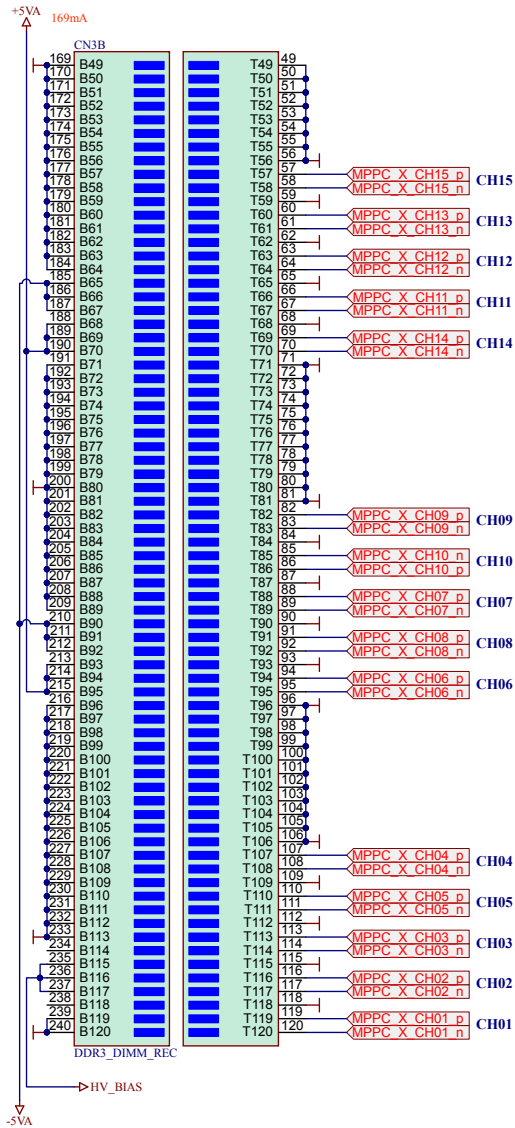
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X-Plane Analog Signal @MPPC Side

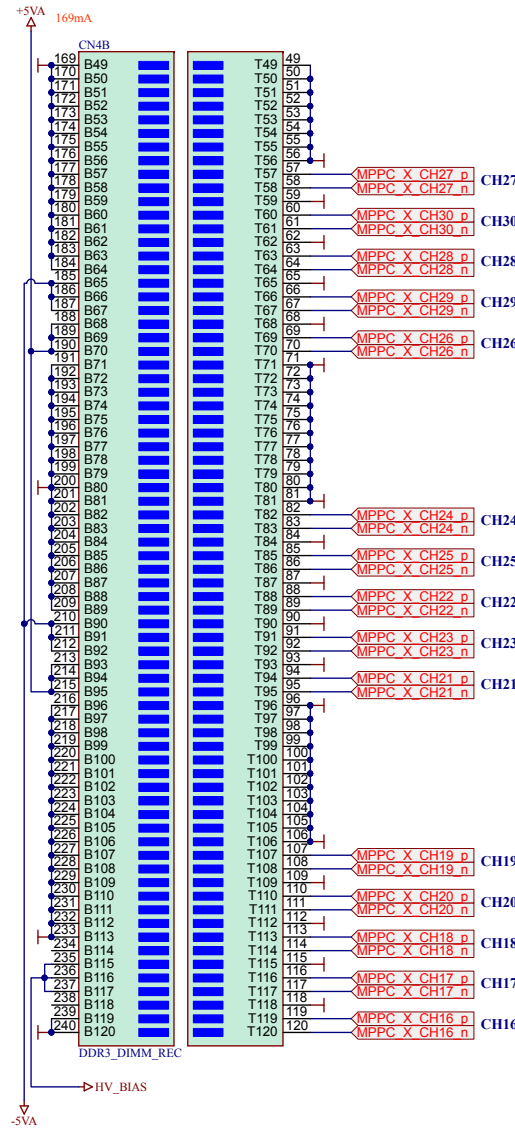
Y-Plane Analog Signal @MPPC Side



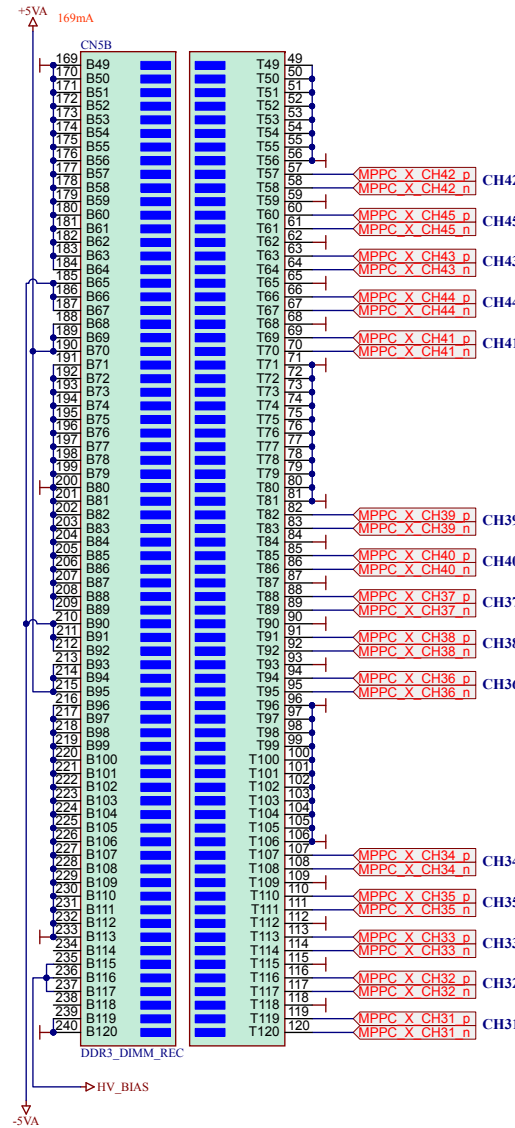
X-Plane Analog Signal Group XA@Pre-Amp Side



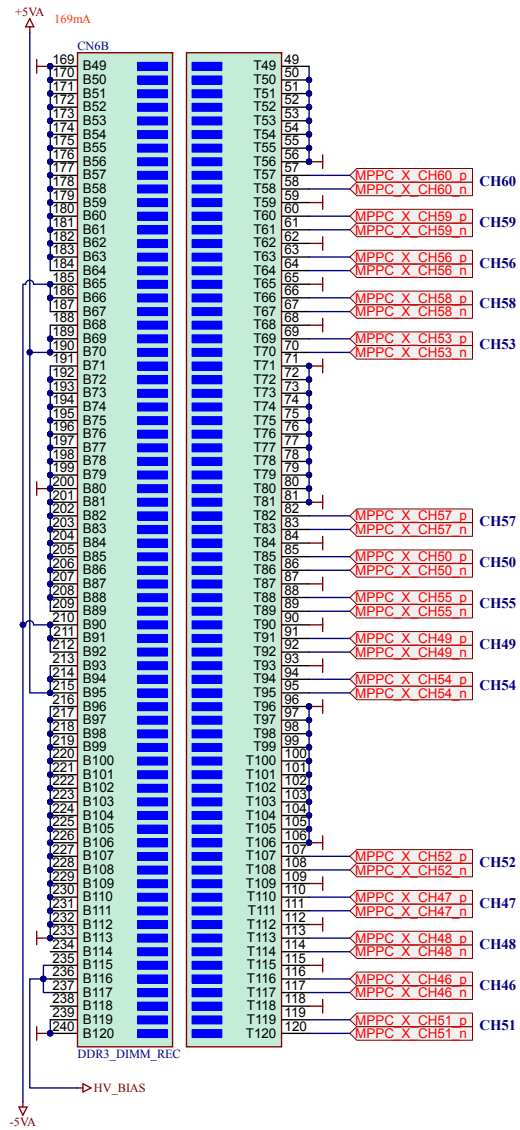
X-Plane Analog Signal Group XB@Pre-Amp Side



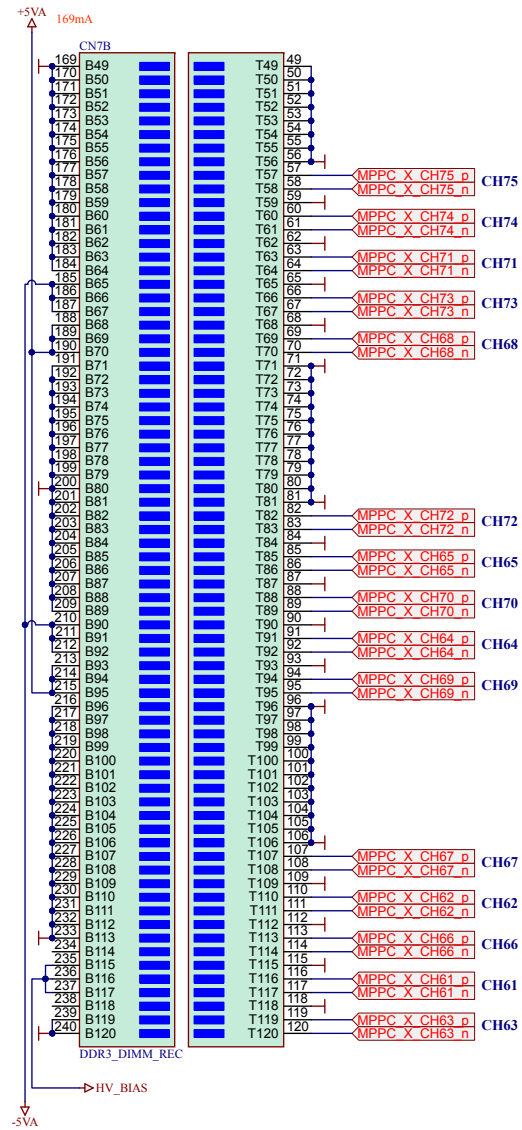
X-Plane Analog Signal Group XC@Pre-Amp Side



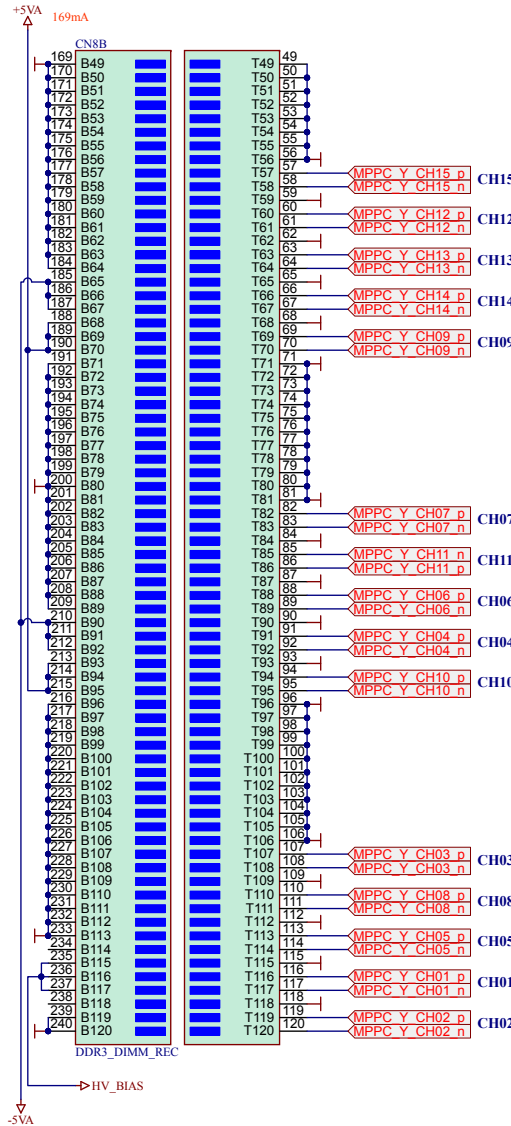
X-Plane Analog Signal Group XD@Pre-Amp Side



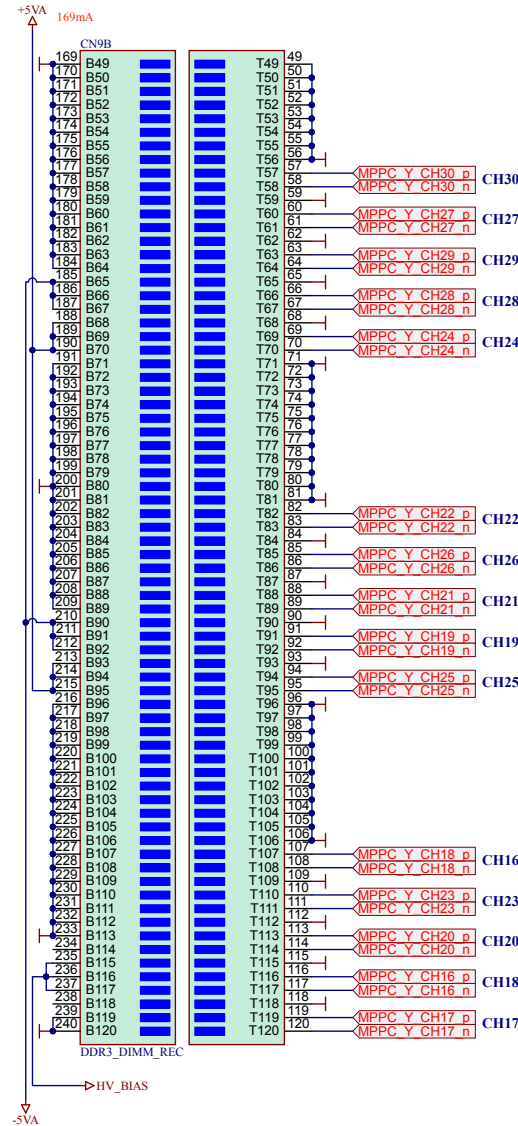
X-Plane Analog Signal Group XE@Pre-Amp Side



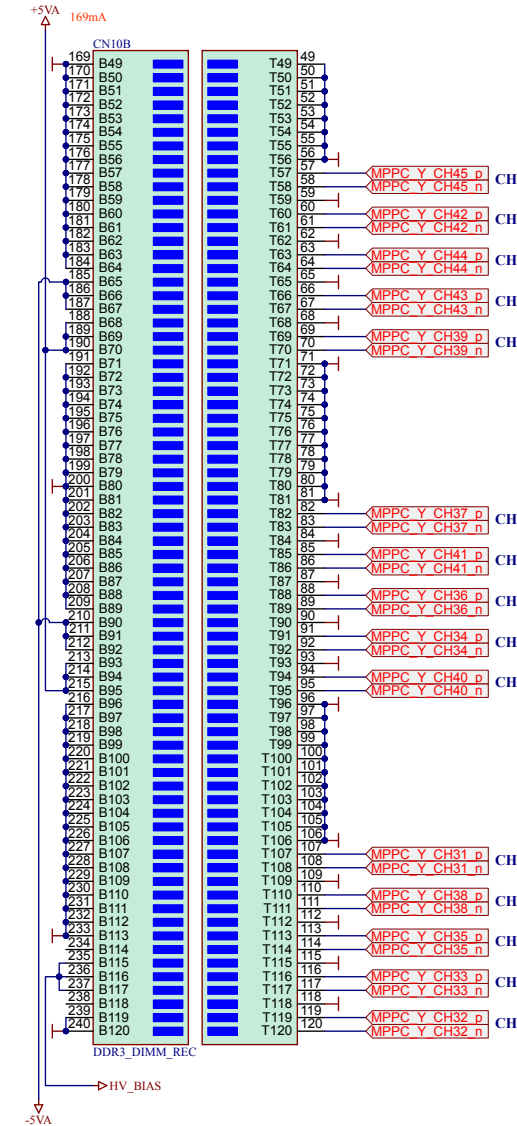
Y-Plane Analog Signal Group YA@Pre-Amp Side



Y-Plane Analog Signal Group YB@Pre-Amp Side

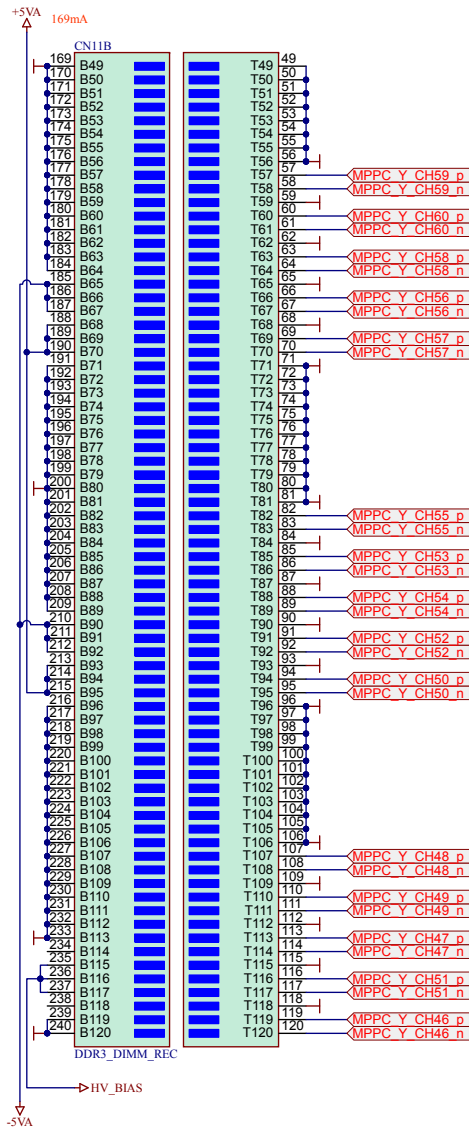


Y-Plane Analog Signal Group YC@Pre-Amp Side

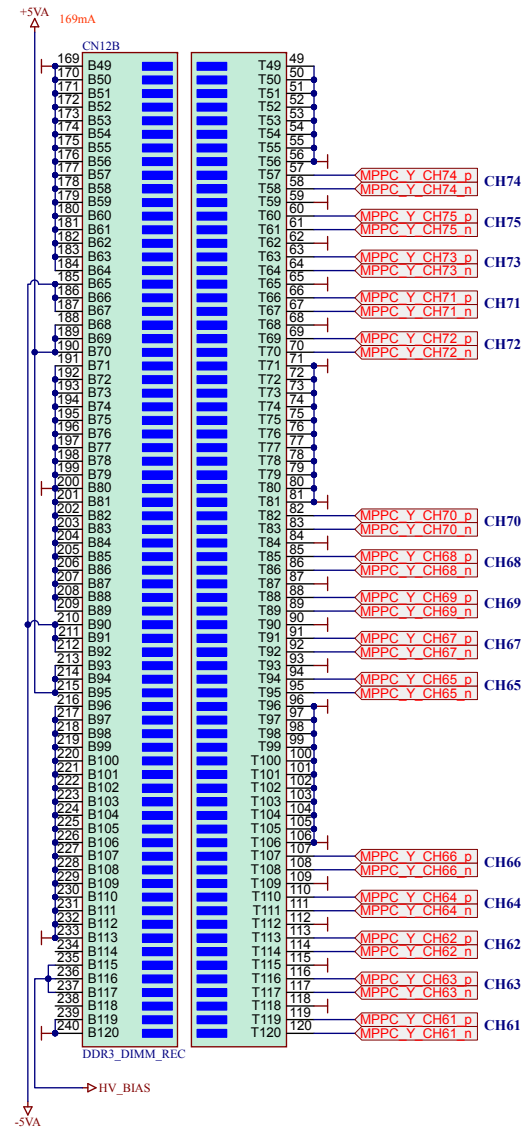




Y-Plane Analog Signal Group YD@Pre-Amp Side



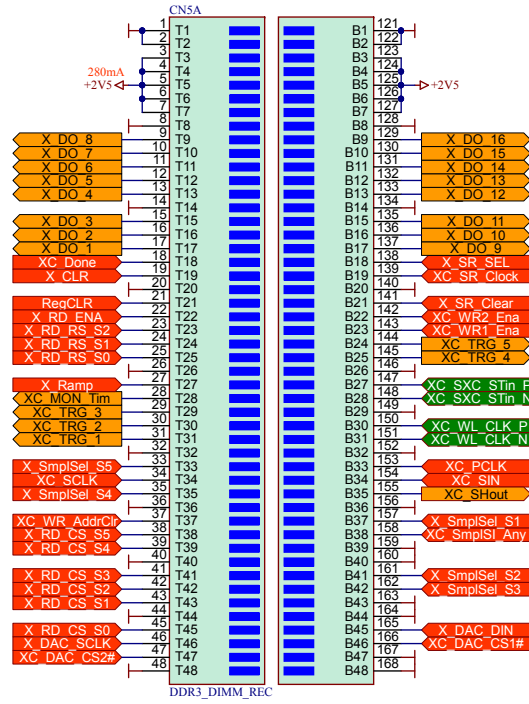
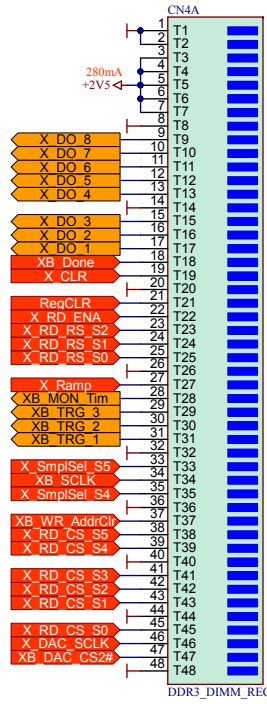
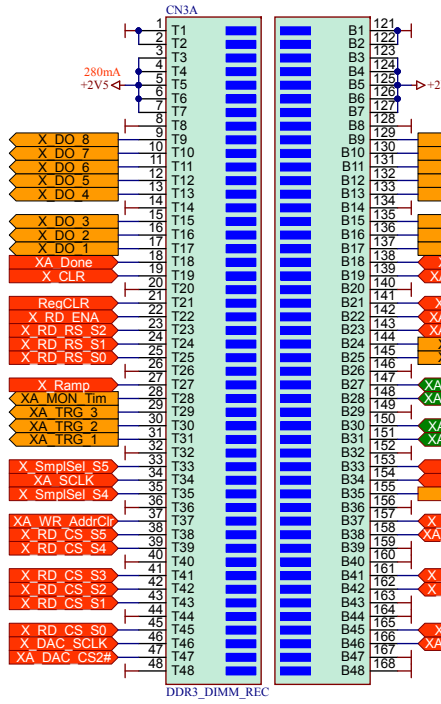
Y-Plane Analog Signal Group YE@Pre-Amp Side



X-Plane Digital IO Signal Group XA@Pre-Amp Side

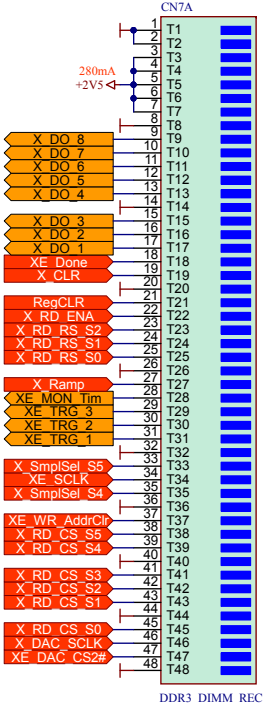
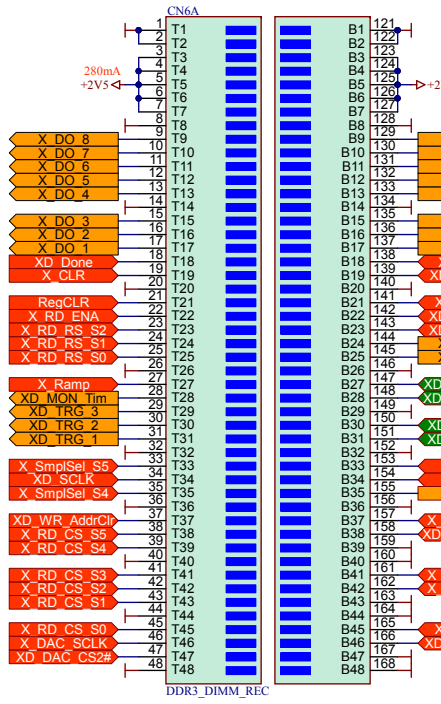
X-Plane Digital IO Signal Group XB@Pre-Amp Side

X-Plane Digital IO Signal Group XC@Pre-Amp Side



X-Plane Digital IO Signal Group XD@Pre-Amp Side

X-Plane Digital IO Signal Group XD@Pre-Amp Side



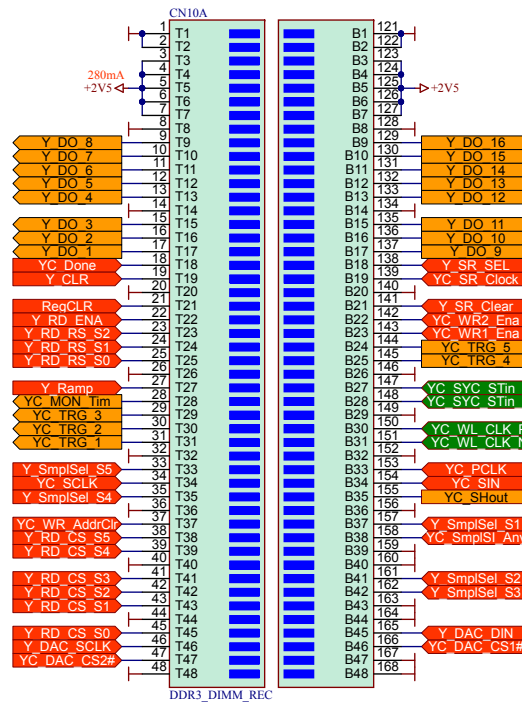
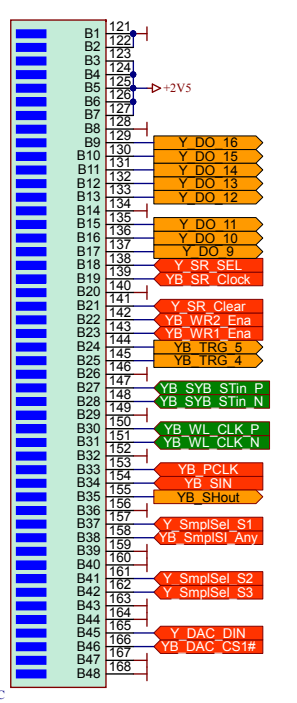
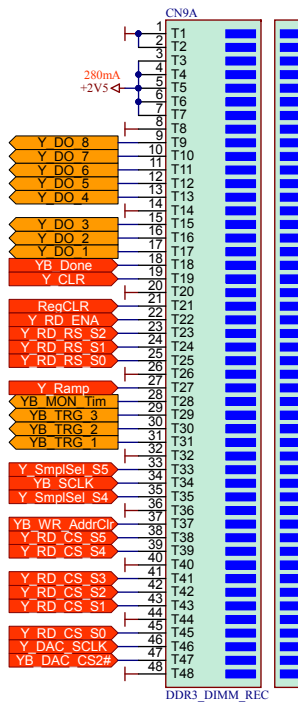
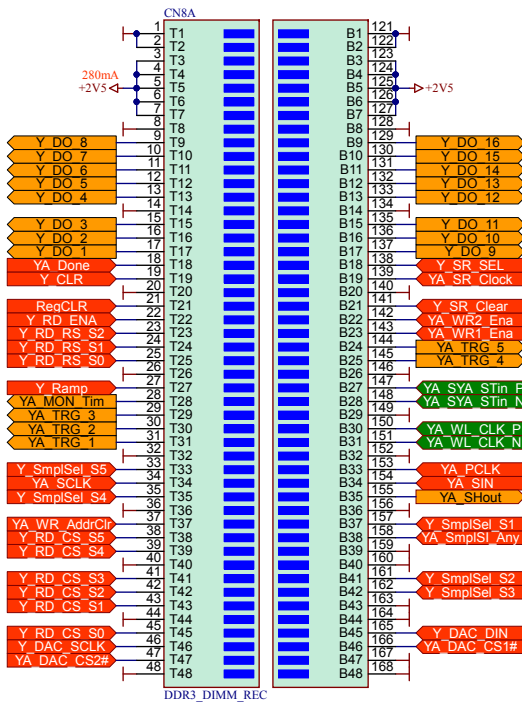
point-to-point	point-to-multipoint within plane	point-to-multipoint overall
10*21	2*38	1
210	76	



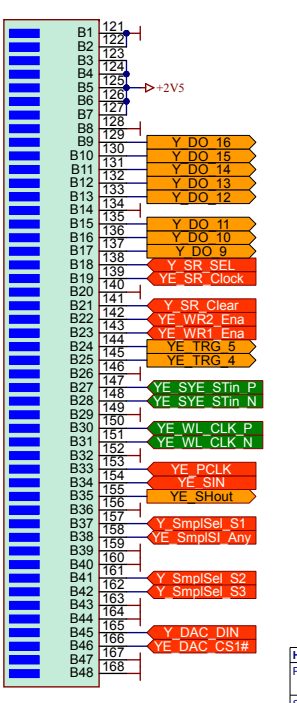
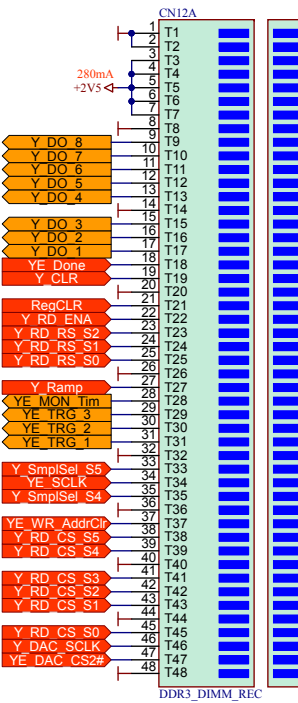
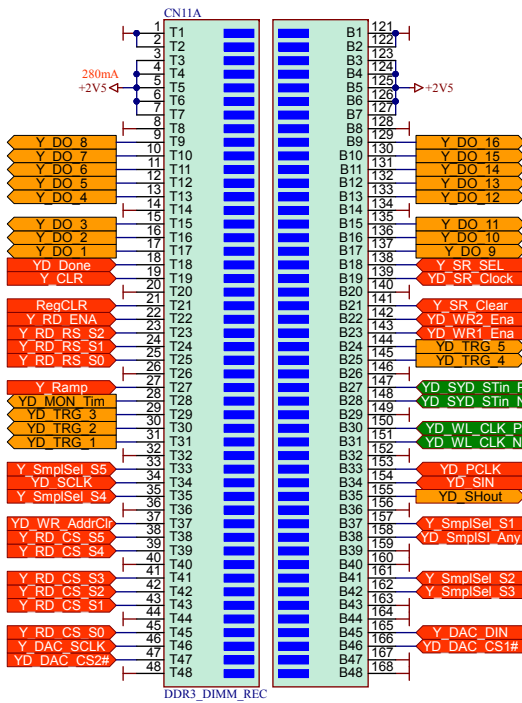
Y-Plane Digital IO Signal Group YA@Pre-Amp Side

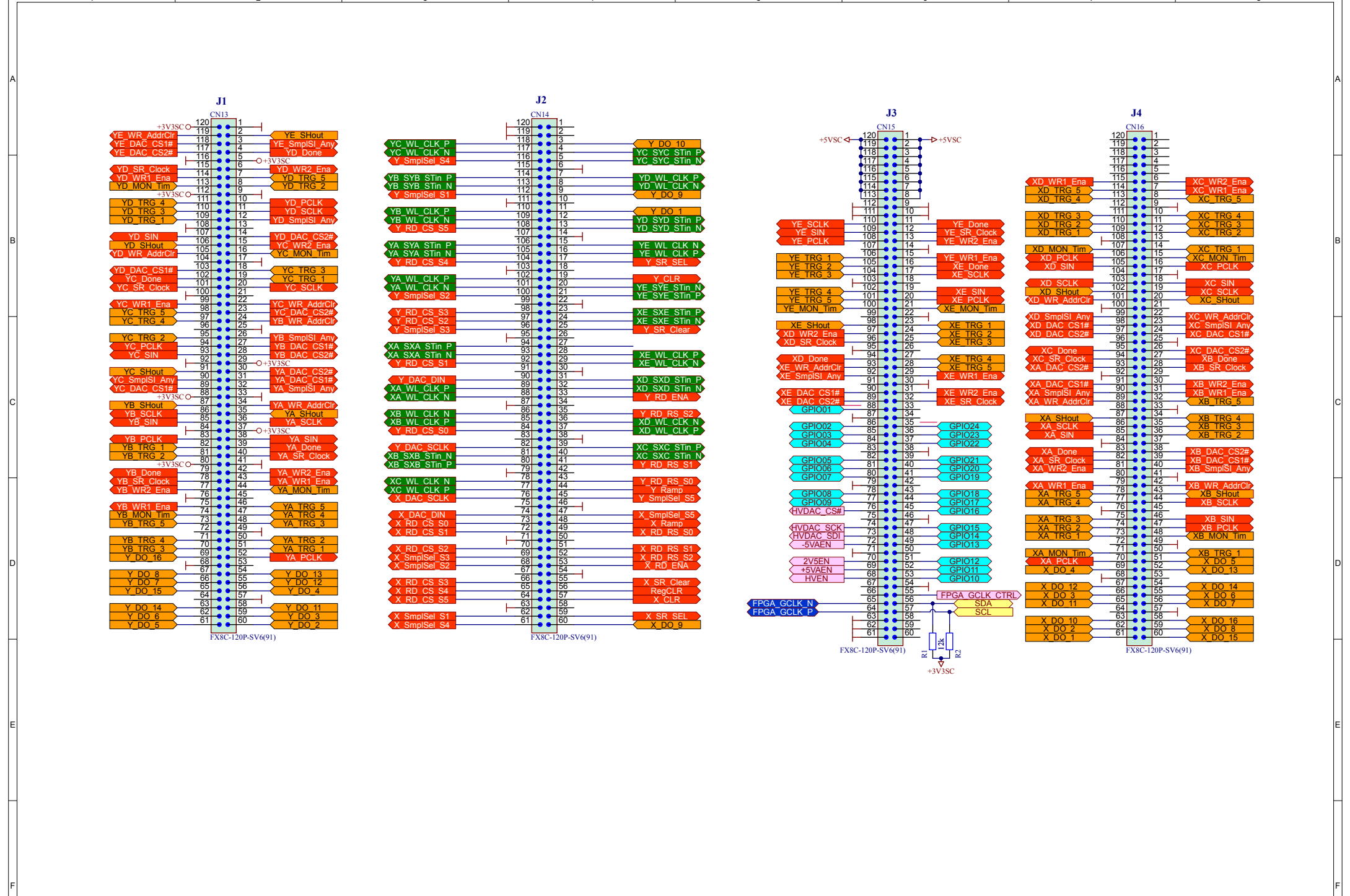
Y-Plane Digital IO Signal Group YB@Pre-Amp Side

Y-Plane Digital IO Signal Group YC@Pre-Amp Side

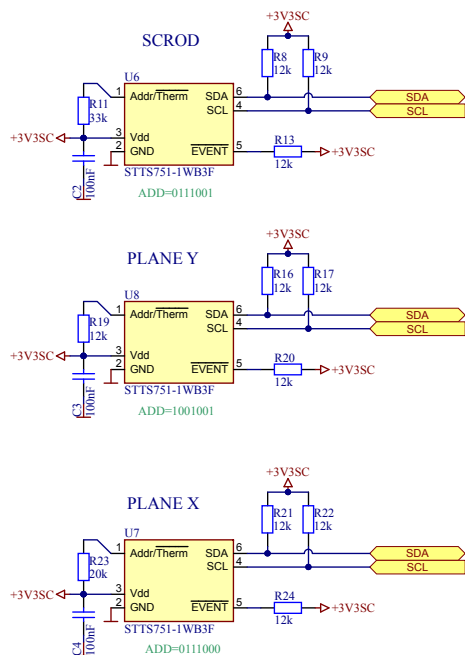


Y-Plane Digital IO Signal Group YE@Pre-Amp Side

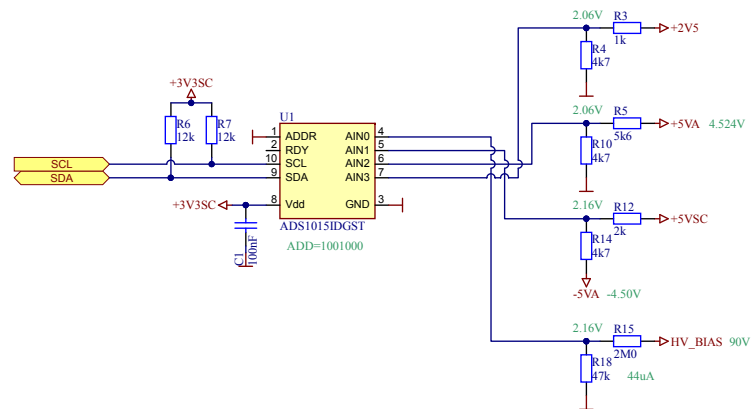




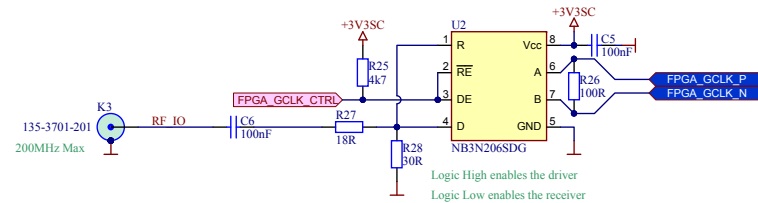
### Temperature Sensors



### Diagnostic ADC

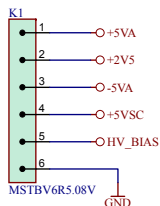


### General Purpose Bidirectional Clock Buffer

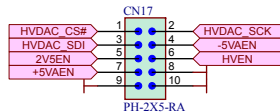


### Power Supply

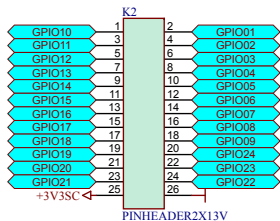
#### PS Input



#### PS Control



### General Purpose IO Connector



### Mechanical

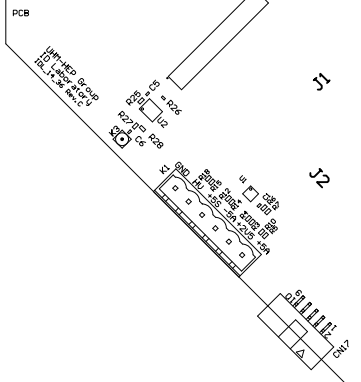
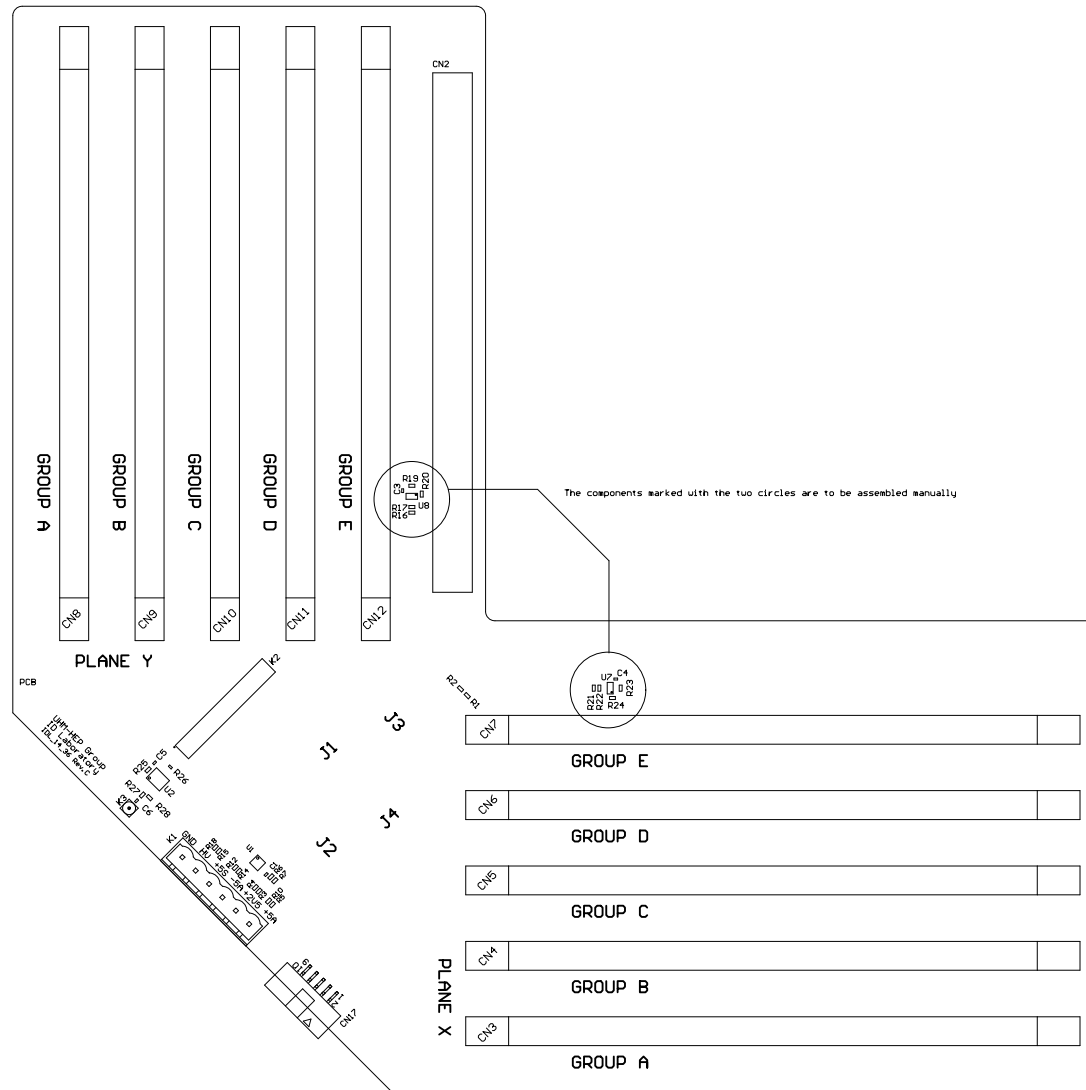
PCB

FID1 FID2 FID3  
FIDRTB FIDRTB FIDRTB

High Energy Physics Group, Instrumentation Development Lab	Designer: Peter Orel	IDLAB design #: IDL_14_36
Project: MB_SciFi_Tracker	Drawn By: Peter Orel	Revision: C
Sheet Title: Diagnostics, Power Supply and Mechanical	Approved By: Gary S. Varner	Variant: [No Variations]
		Modif. Date: 10-Oct-14
		Sheet 11 of 11

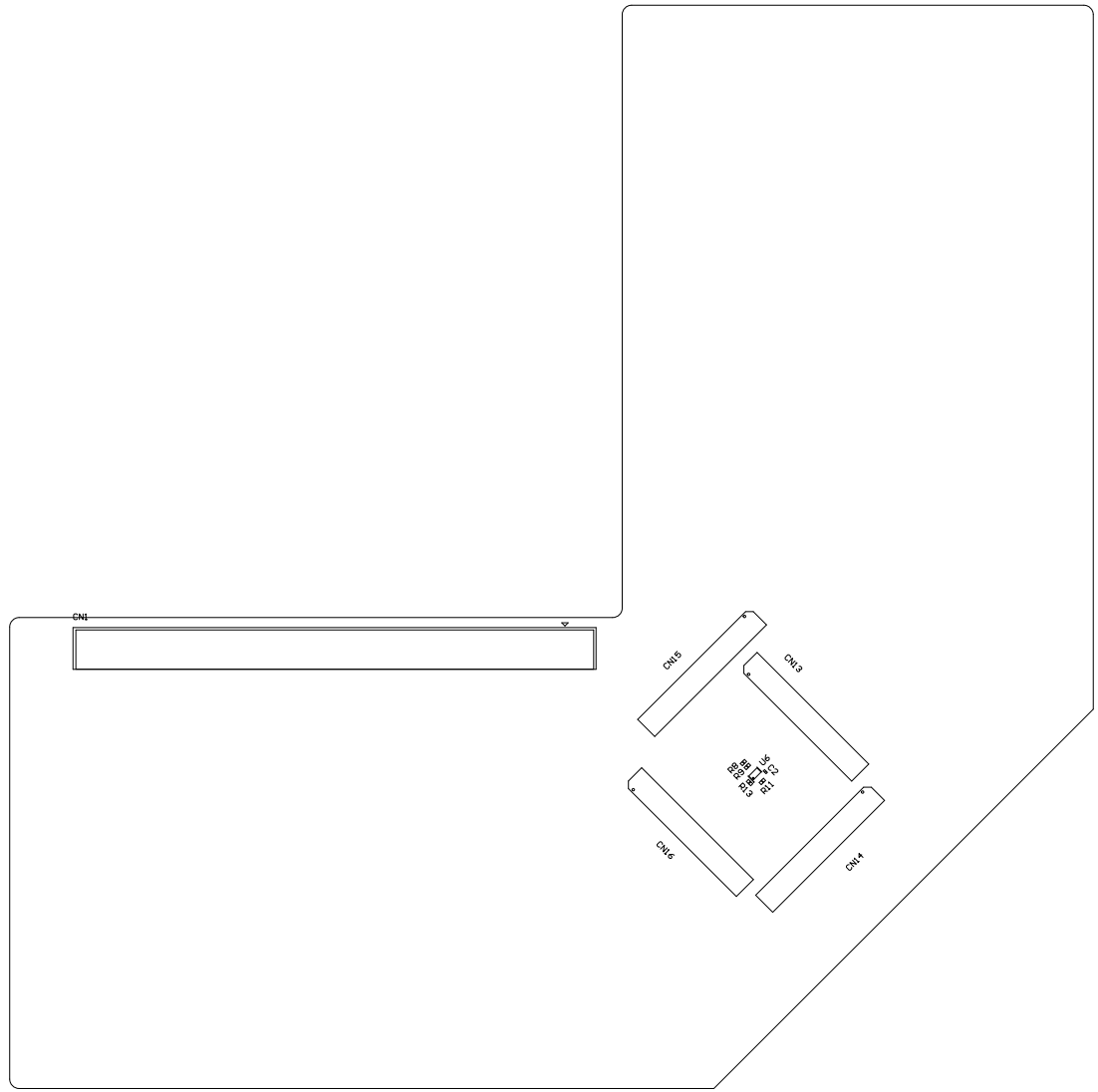


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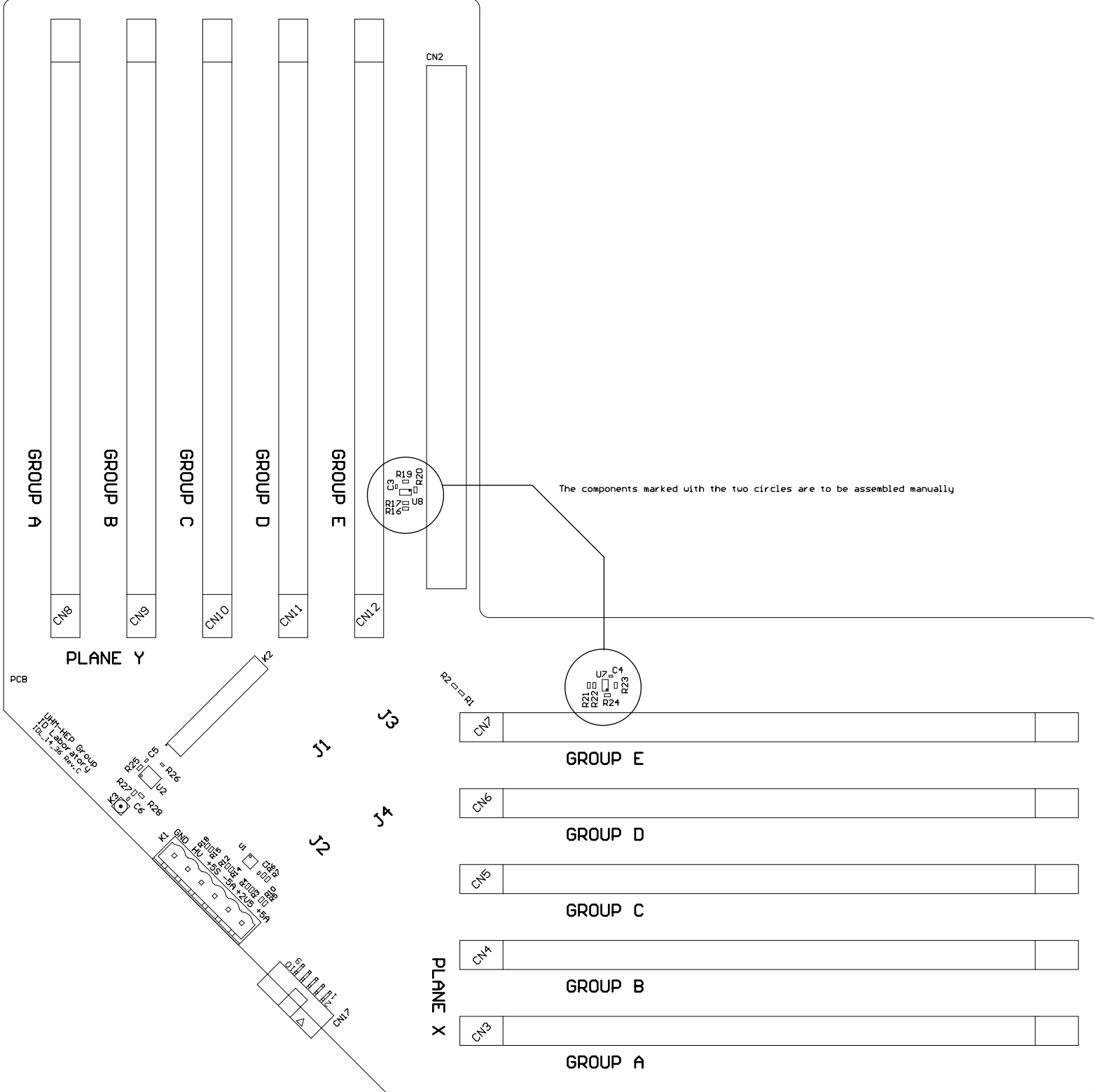


The components marked with the two circles are to be assembled manually

Designer: Peter Orel	Revision: .Version	File: IDL_14_36_C.PcbDoc	Sheet 1 of 1	Code: IDL_14_36
Drawn By: Peter Orel	Modif. Date: Date	Variant: (No Variations)	ASSEMBLY	ID: MB_SciFi_Tracker
Approved By: Gary S. Varner	Print Date: 13-Oct-14	Signature:	Size: A3 H	University of Hawaii at Manoa High Energy Physics Group Instrumentation Development Laboratory
Title: Top Assembly Drawing				



Designer: Peter Orel	Revision: .Version	File: IDL_14_36_C.PcbDoc	Sheet 1 of 1	Coder: IDL_14_36
Drawn By: Peter Orel	Modif. Date: Date	Variant: [No Variations]	ASSEMBLY	ID: MB_SciFI_Tracker
Approved By: Gary S. Varnier	Print Date: 13-Oct-14	Signature:	Size: A3 H	University of Hawaii at Manoa High Energy Physics Group Instrumentation Development Laboratory
Title: Bottom Assembly Drawing				



The components marked with the two circles are to be assembled manually

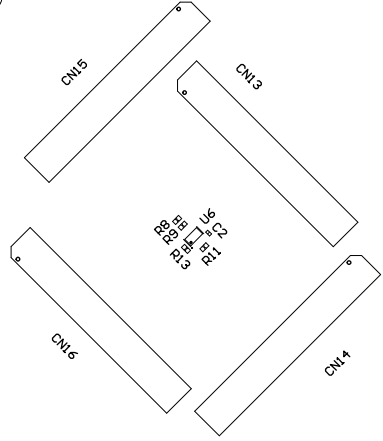
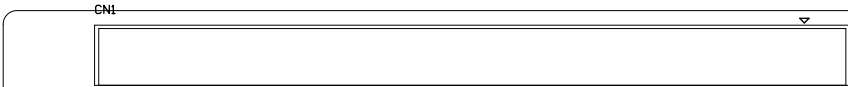
UHM-HEP Group  
 TO: Labo. at CFM  
 PC: 1.1.36 Rev. C

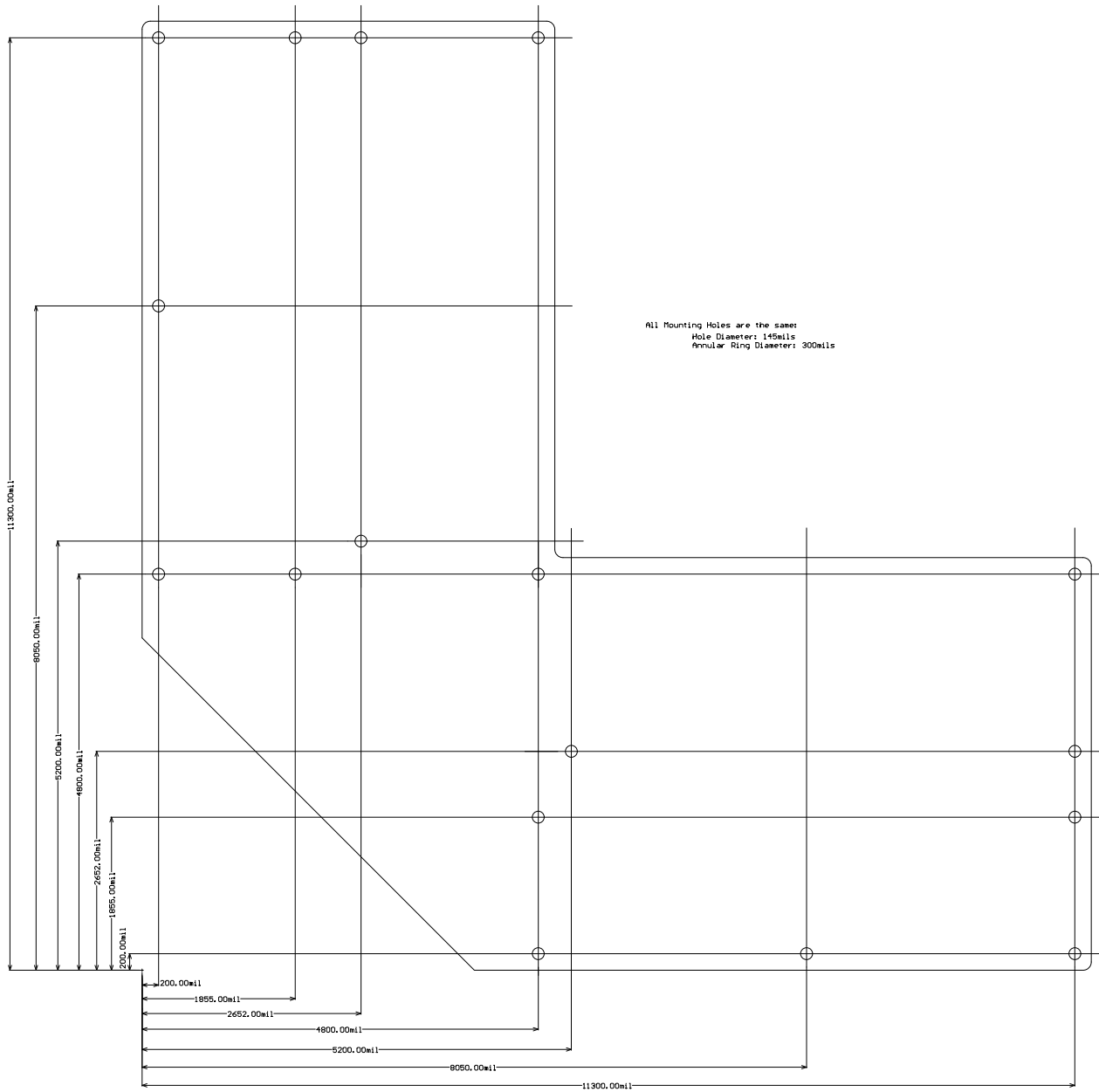
R25 = C5  
 R26 = U2  
 R27 = C6  
 R28 = C6

U1 = C82  
 U2 = C83  
 U3 = C84  
 U4 = C85

PCB







All Mounting Holes are the same:  
 Hole Diameter: 145mil  
 Annular Ring Diameter: 300mil

Designer: Peter Orel	Revision: .Version	File: IDL_14_36_C.PcbDoc	Sheet 1 of 1	Code: IDL_14_36
Drawn By: Peter Orel	Modif. Date: Date	Variant: (No Variations)	PCB	ID: MB_SciFi_Tracker
Approved By: Gary S. Varner	Print Date: 10-Oct-14	Signature:	Size: A3 H	University of Hawaii at Manoa High Energy Physics Group Instrumentation Development Laboratory
Title: Mounting Hole Dimensions				

# Bill Of Material

# Compact SciFi Tracker

Source Data From:

IDL\_14\_36\_C.PrjPcb

Project:

MB\_SciFi\_Tracker

Revision:

C

Variant:

None

IDLAB Design #:

IDL\_14\_36

Report Date:

06:46:36 PI 13-Oct-14

Print Date:

18:46 13-10-2014



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Note: The components listed in this document can be purchased from different suppliers, following the original manufacturer's part number.

Standard components (resistors and capacitors) can be produced by different manufacturers, however they must adhere to the quality requirements specified for the original components defined in this document.

For all other components, the purchasing and assembly of alternatives, not specified in this document, must be authorized by the Instrumentation Development Laboratory

#	Designator	Quantity	Description	Comment	Manufacturer	Manufacturer No	Supplier	Supplier No	Price	
1	PCB	1	Printed Circuit Board 8 layer	PCB...	PCB Universe	IDL_14_36			0	
2	FID1, FID2, FID3	3	Fiducial top & bottom round open mask	FIDRTB					0	
3	R3	1	Chip Resistor 0603	1k	Panasonic	ERJ-3EKF1001V	Digi-Key	P1.00KHCT-ND	0.1	
4	R4, R10, R14, R25	4	Chip Resistor 0603	4k7	Panasonic	ERJ-3EKF4701V	Digi-Key	P4.70KHCT-ND	0.4	
5	R5	1	Chip Resistor 0603	5k6	Vishay B.	MCT06030C5601FP500	Digi-Key	MCT0603-5.60K-CFCT-ND	0.08	
6	R11	1	Chip Resistor 0603	33k	Panasonic	ERJ-3EKF3302V	Digi-Key	P33.0KHCT-ND	0.1	
7	R12	1	Chip Resistor 0603	2k	Panasonic	ERJ-3EKF2001V	Digi-Key	P2.00KHCT-ND	0.1	
8	R15	1	Chip Resistor 0603	2M0	Panasonic	ERJ-3EKF2004V	Digi-Key	P2.00MHCT-ND	0.1	
9	R18	1	Chip Resistor 0603	47k	Panasonic	ERJ-3EKF4702V	Digi-Key	P47.0KHCT-ND	0.1	
10	R23	1	Chip Resistor 0603	20k	Panasonic	ERJ-3EKF2002V	Digi-Key	P20.0KHCT-ND	0.1	
11	R26	1	Chip Resistor 0402	100R	Panasonic	ERJ-2RK1000X	Digi-Key	P100LCT-ND	0.1	
12	R27	1	Chip Resistor 0603	18R	Panasonic	ERJ-3EKF18R0V	Digi-Key	P18.0HCT-ND	0.1	
13	R28	1	Chip Resistor 0603	30R	Panasonic	ERJ-3EKF30R0V	Digi-Key	P30.0HCT-ND	0.1	
14	R1, R2, R6, R7, R8, R9, R13, R16, R17, R19, R20, R21, R22, R24	14	Chip Resistor 0805 Precision	12k	Panasonic	ERJ-3EKF1202V	Digi-Key	P12.0KHCT-ND	1.4	
15	C1, C2, C3, C4, C5, C6	6	Capacitor chip ceramic 0402	100nF	Murata	GRM155R71C104KA88D	Digi-Key	490-3261-1-ND	0.6	
16	U1	1	ADC 12bit 3.3ksps	ADS1015IDGST	Texas Instruments	ADS1015IDGST	Digi-Key	296-25227-1-ND	3.42	
17	U2	1	3.3 V Differential Multipoint Low Voltage M-LVDS Driver Receiver	NB3N206SDG	ON Semiconductor	NB3N206SDG	Digi-Key	NB3N206SDGOS-ND	2.39	
18	U6, U7, U8	3	2.25 V low-voltage local digital temperature sensor	STTS751-1WB3F	STMicroelectronics	STTS751-1WB3F	Digi-Key	497-10662-1-ND	5.4	
19	CN13, CN14, CN15, CN16	4	Hirose Connector 120pin SMD R0.6mm male	FX8C-120P-SV6(91)	Hirose	FX8C-120P-SV6(91)	Digi-Key	H11527-ND	22.76	
20	CN17	1	PIN HEADER 2x5 R2.54mm Right-Angle	PH-2X5-RA	CNC Tech	3020-10-0200-00	Digi-Key	3020-10-0200-00	0.61	
21	K1	1	Combicon header 6 pin vertical closed R5.08mm	MSTBV6R5.08V	Phoenix Contact	1755778	Digi-Key	277-1154-ND	1.67	
22	K2	1	PIN HEADER 2x13 R2.54mm	PINHEADER 2X13V	FCI	68602-126HLF	Digi-Key	609-3367-ND	1.03	
23	K3	1	MMCX connector PCB vertical Jack	135-3701-201	Emerson	135-3701-201	Digi-Key	J597-ND	4.37	
24	CN1, CN2	2	150pin Europacard 2.54mm Connector	EU-5650405-5	TE Connectivity	5650405-5	Digi-Key	A32848-ND	17.48	
25	CN3, CN4, CN5, CN6, CN7, CN8, CN9, CN10, CN11, CN12	10	DDR3 DIMM PCB Socket	DDR3_DIMM REC	TE Connectivity	1-1932000-1	Digi-Key	A97917-ND	40.3	
<b>Approved</b>		<b>Total Quantity</b>	<b>Notes:</b>							<b>Total Price</b>
Total components:		63								102.81

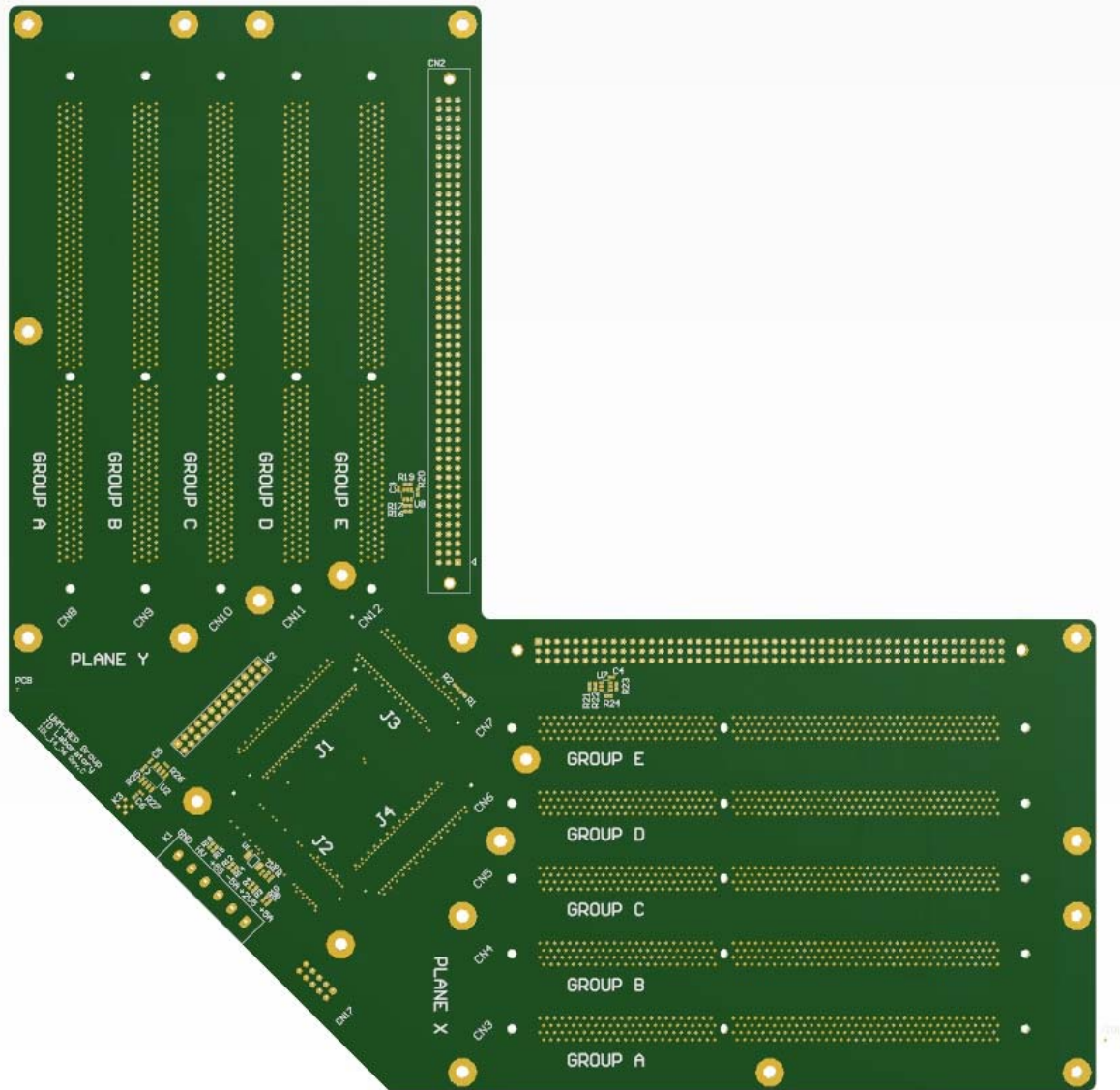


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**High Energy Physics Group  
Instrumentation Development Laboratory**  
2505 Correa Road, Honolulu, HI 96822

**Documentation for PCB:**

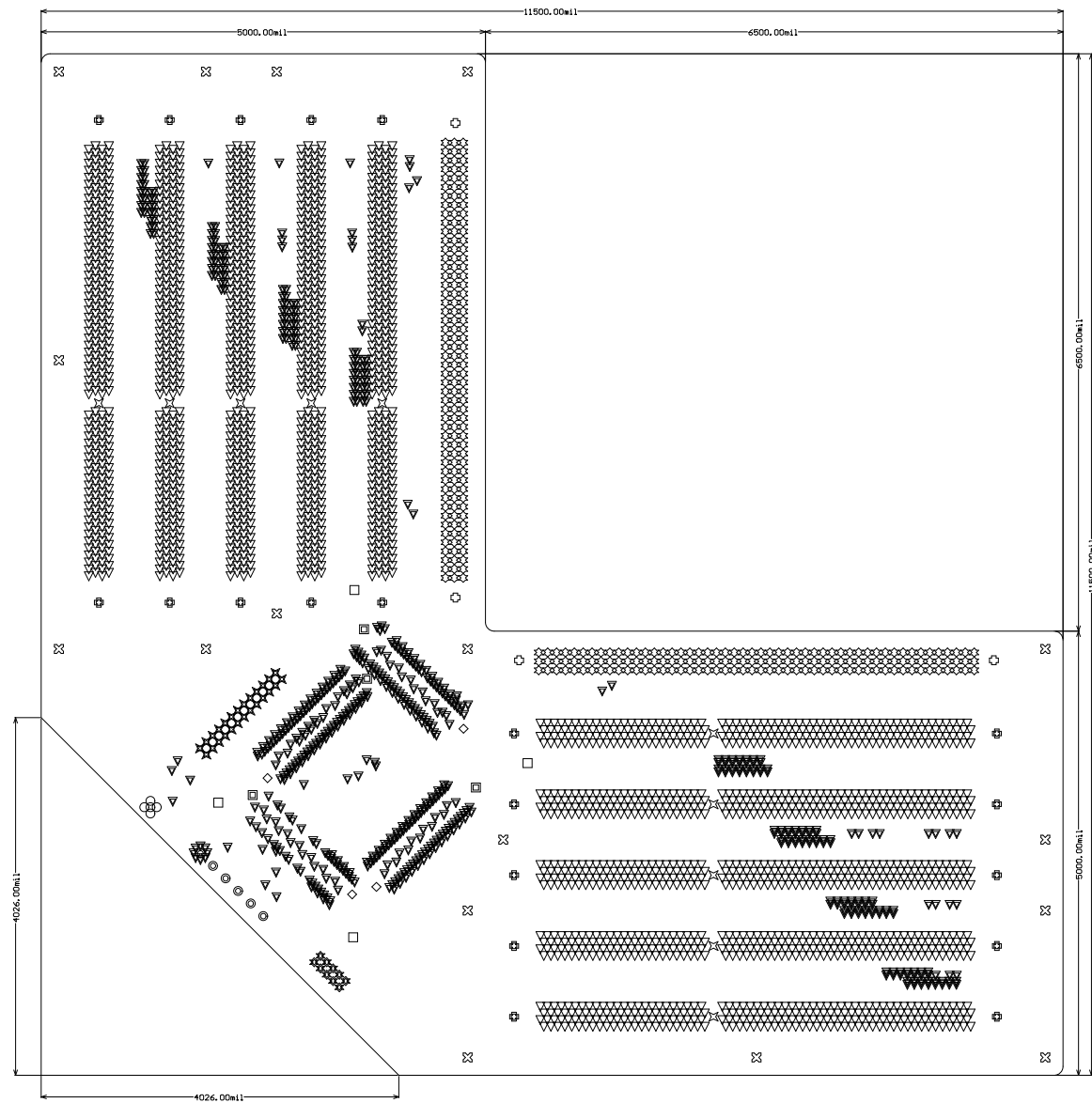
**Project Name:** Compact SciFi Tracker  
**Board Name:** MB\_SciFi\_Tracker  
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**Revision:** C



High Energy Physics Group, Instrumentation Development Lab	Designer: Peter Orel	IDLAB design #: IDL_14_36
Project: MB_SciFi_Tracker	Drawn By: Peter Orel	Revision: C
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Sheet Title: Mother Board for Compact SciFi Tracker		Modif. Date: 10-Oct-14
		Sheet 1 of 11



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- Notes:**
- Board shall be fabricated - performance class II as per IPC-6011 and IPC6012
  - PCB manufacturer logo, FIN, revision and/or date code of manufacturing shall be printed in top solder mask (not over pcb traces, allowed over copper plane). The date code shall be in the format: "WWYY" where WW=week and YY= year, max height 0.15 inches. Must be RoHS compliant and survive a lead-free assembly max reflow of 260 deg C (5 passes)
  - Silkscreen printed on both sides
  - Material: high temperature FR4 class epoxy glass rated UL94V0, UL symbol and rating shall be marked farside  
35um copper for external layers and 18um for all internal layers  
Must be RoHS compliant and survive a lead-free assembly max reflow of 260 deg C (5 passes)  
Td rating: >340 deg C  
Tg = 150 deg C (min)
  - Solder mask: SMOBC per IPC-SM-840C, class T must be RoHS compliant, 0.001" max measured over bare copper plating, must clear all lands as indicated on gerber solder mask layers, color= GREEN
  - Finish: HAL-Sn100CL, 7-10 um - over bare copper only
  - Solderability test: Category 2 of J-STD-003
  - Finished boards shall not have nicks, scratches, voids, exposed copper, poor plating or misdrilled holes
  - All holes sizes are after plating
  - PCB manufacturer may add copper thickening as needed to improve manufacturability, thickening to be 0.030" round pads at 0.050" spacing
  - Unless otherwise indicated, all linear tolerances shall be XX.X +/-0.2mm and XX.XX +/-0.1mm
  - Gerber file GM1 shows board outline (milling line)
  - Table 1 shows Layer stack details

**Additional notes:**  
A1. Finished board thickness = 2.00mm +/-10%; measured over top/bottom copper and solder mask

Table 1a: Layer Stack Details for IDL\_14\_36 Rev.C (Imperial Units)

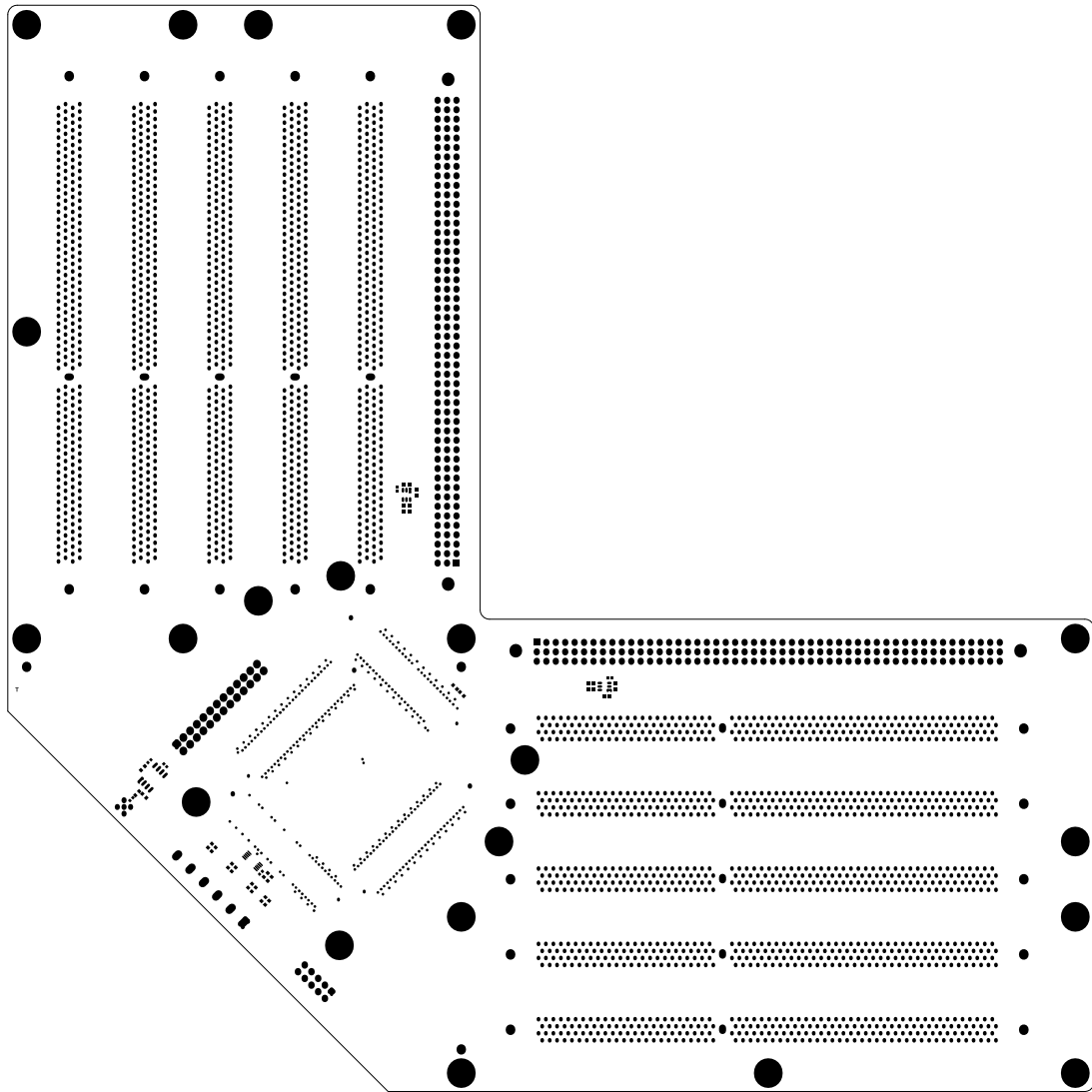
Layer	Name	Material	Thickness	Color	Prep
1	Top Overlay	Solder Mask	0.0014	3.0	None
2	Top Solder	Solder Plating	0.0014	3.0	None
3	Top Layer - PRE	Copper	0.0014	3.0	None
4	Dielectric 1	Fiber	0.0014	4.0	None
5	Layer 2 - Outermost	Copper	0.0014	4.2	None
6	Dielectric 3	Fiber	0.0014	4.2	None
7	Layer 4 - PRE	Copper	0.0014	4.2	None
8	Dielectric 2	Fiber	0.0014	4.2	None
9	Layer 6 - Innermost	Copper	0.0014	4.2	None
10	Dielectric 2L	Fiber	0.0014	4.2	None
11	Layer 5 - Outermost	Copper	0.0014	4.2	None
12	Dielectric 3	Fiber	0.0014	4.2	None
13	Layer 6 - PRE	Copper	0.0014	4.2	None
14	Dielectric 3L	Fiber	0.0014	4.2	None
15	Layer 5 - Outermost	Copper	0.0014	4.2	None
16	Dielectric 2	Fiber	0.0014	4.2	None
17	Bottom Layer - PRE	Copper	0.0014	3.5	None
18	Bottom Solder	Solder Plating	0.0014	3.5	None
19	Bottom Overlay	Solder Mask	0.0014	3.5	None

Table 1b: Layer Stack Details for IDL\_14\_36 Rev.C (Imperial Units)

Layer	Name	Material	Thickness	Color	Prep
1	Top Overlay	Solder Mask	0.0014	3.0	None
2	Top Solder	Solder Plating	0.0014	3.0	None
3	Top Layer - PRE	Copper	0.0014	3.0	None
4	Dielectric 1	Fiber	0.0014	4.0	None
5	Layer 2 - Outermost	Copper	0.0014	4.2	None
6	Dielectric 3	Fiber	0.0014	4.2	None
7	Layer 4 - PRE	Copper	0.0014	4.2	None
8	Dielectric 2	Fiber	0.0014	4.2	None
9	Layer 6 - Innermost	Copper	0.0014	4.2	None
10	Dielectric 2L	Fiber	0.0014	4.2	None
11	Layer 5 - Outermost	Copper	0.0014	4.2	None
12	Dielectric 3	Fiber	0.0014	4.2	None
13	Layer 6 - PRE	Copper	0.0014	4.2	None
14	Dielectric 3L	Fiber	0.0014	4.2	None
15	Layer 5 - Outermost	Copper	0.0014	4.2	None
16	Dielectric 2	Fiber	0.0014	4.2	None
17	Bottom Layer - PRE	Copper	0.0014	3.5	None
18	Bottom Solder	Solder Plating	0.0014	3.5	None
19	Bottom Overlay	Solder Mask	0.0014	3.5	None

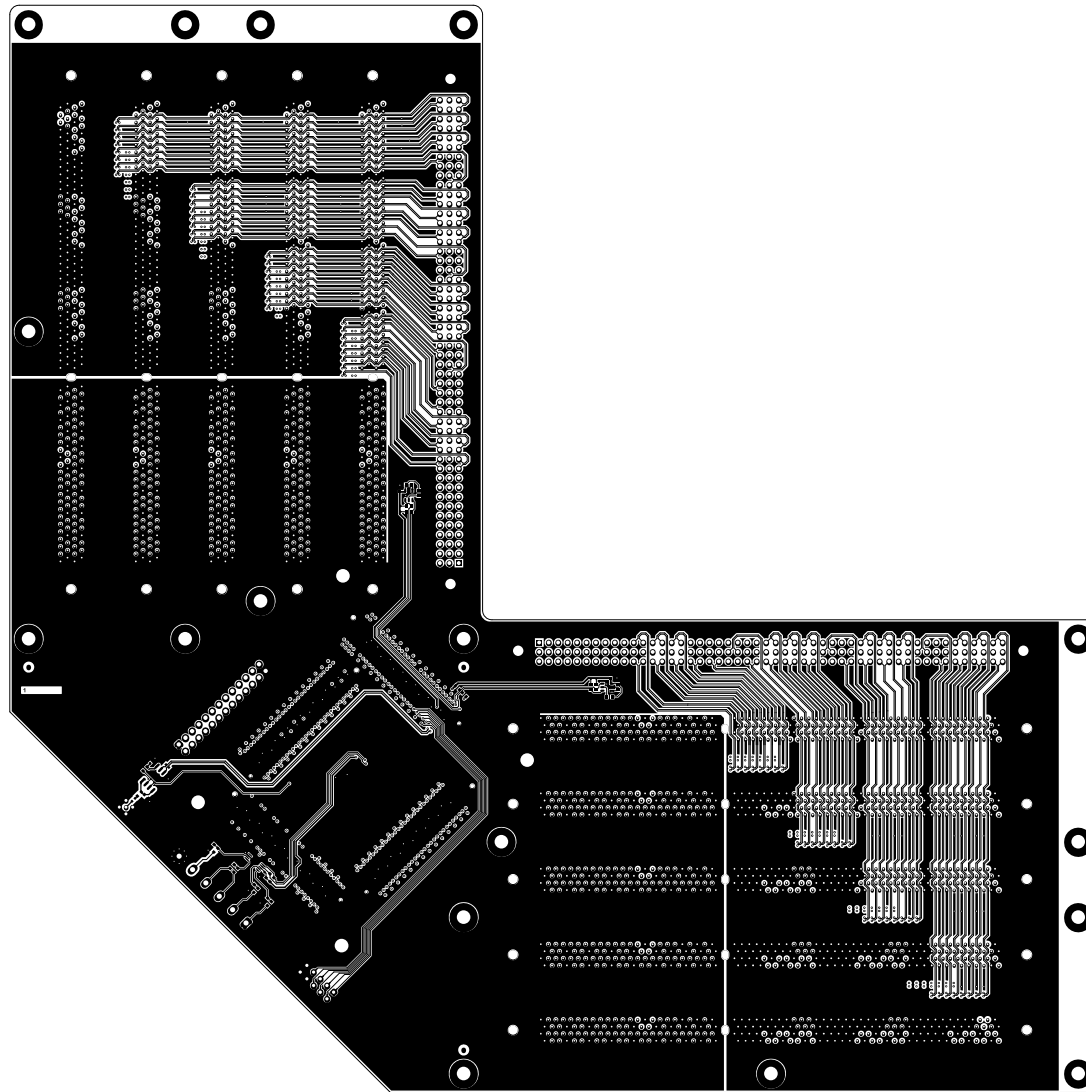
Table 2: NC Drill Details for IDL\_14\_36 Rev.C

Symbol	HR Count	Finished Hole Size	Plated	Hole Type
∅	4	1.188mm (0.0471")	None	Round
∅	4	1.588mm (0.0625")	None	Round
∅	4	2.16mm (0.0851")	None	Round
∅	4	2.68mm (0.1055")	None	Round
∅	5	2.81mm (0.1106")	None	Round
∅	5	3.48mm (0.1370")	None	Round
∅	10	3.68mm (0.1449")	None	Round
∅	10	4.88mm (0.1921")	None	Round
∅	17	3.68mm (0.1449")	None	Round
∅	17	2.68mm (0.1055")	None	Round
∅	18	1.588mm (0.0625")	None	Round
∅	300	1.61mm (0.0634")	None	Round
∅	400	2.25mm (0.0886")	None	Round
∇	400	2.25mm (0.0886")	None	Round
		4.00mm (0.1575")	None	Round

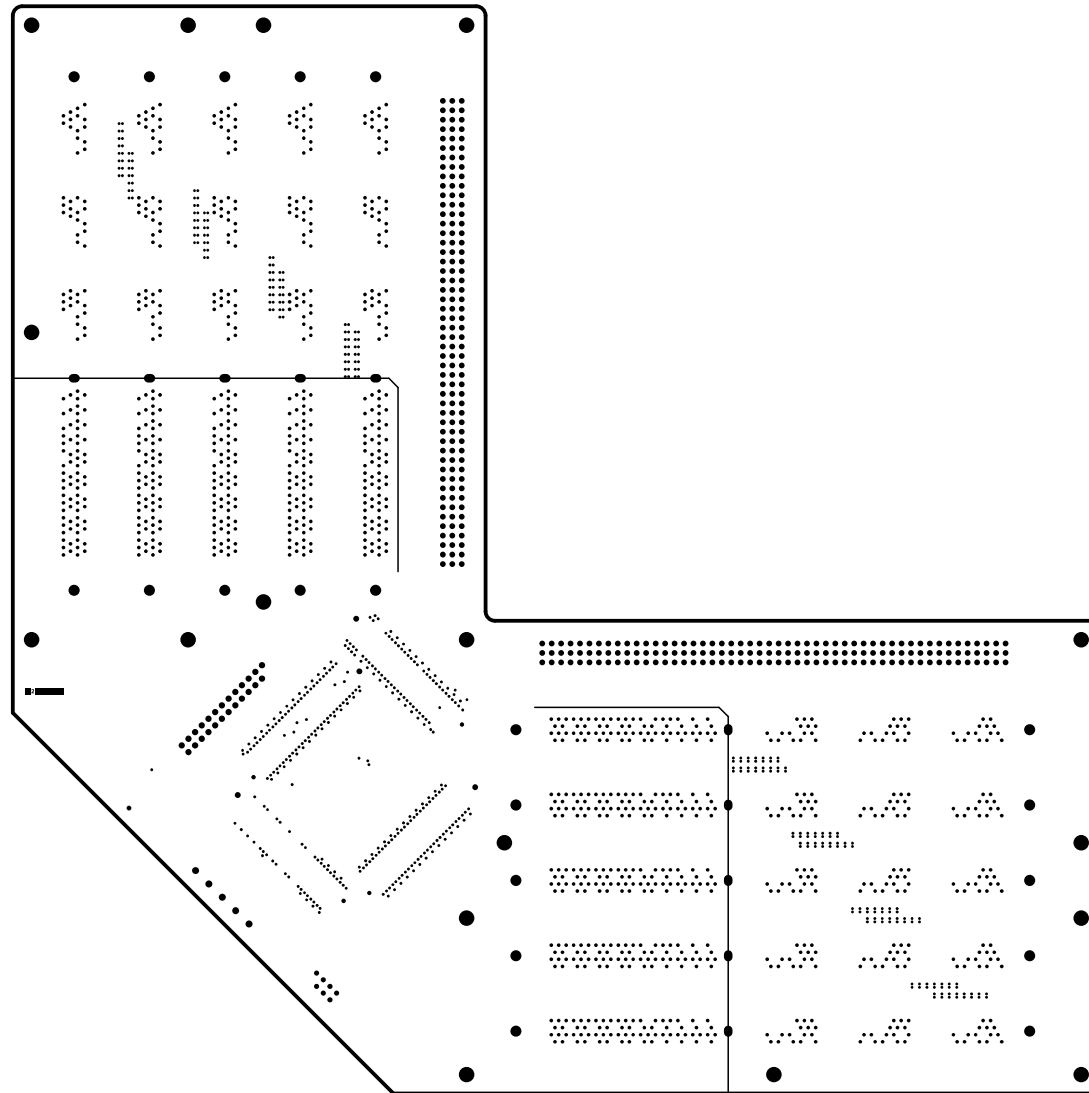


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Approved By: Gary S. Varner	Print Date: 13-Oct-14	Signature:	Size: A3 H	University of Hawaii at Manoa High Energy Physics Group Instrumentation Development Laboratory
Title: Top Solder Mask GTS				

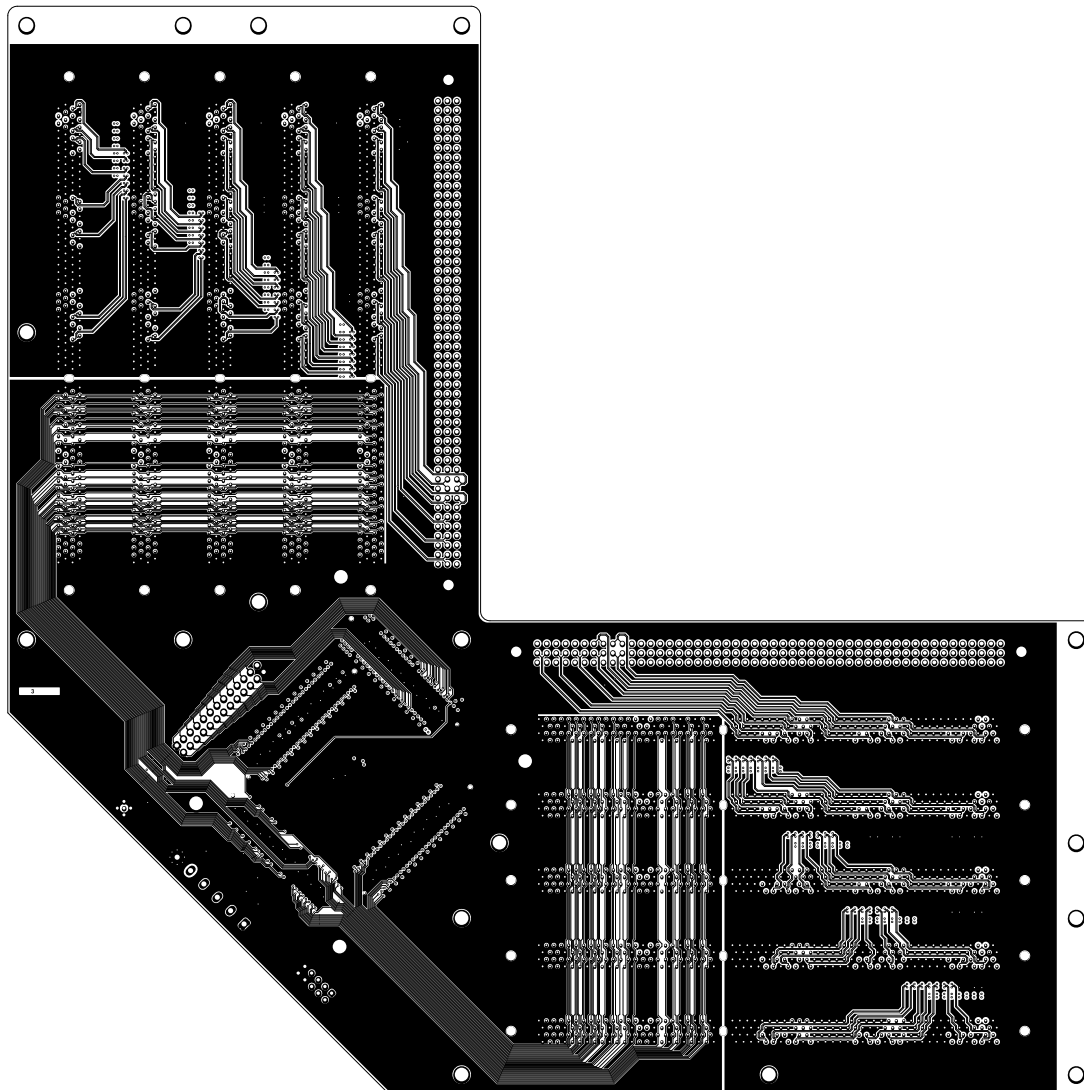




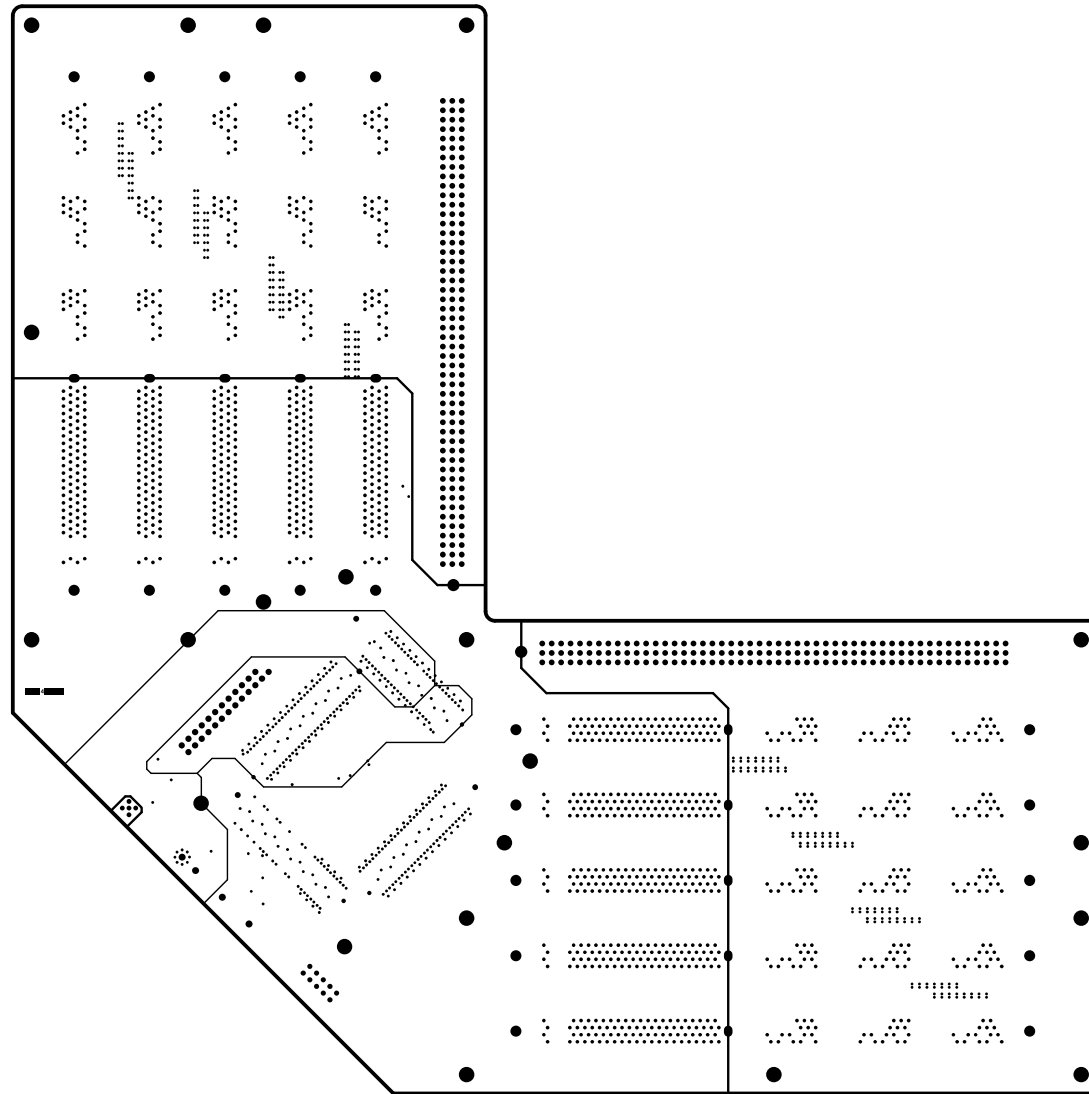
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Approved By:	Gary S. Varner	Print Date:	13-Oct-14	Signature:		Size:	A3 H		
Title:	Top Layer 1 GTL								University of Hawaii at Manoa High Energy Physics Group Instrumentation Development Laboratory



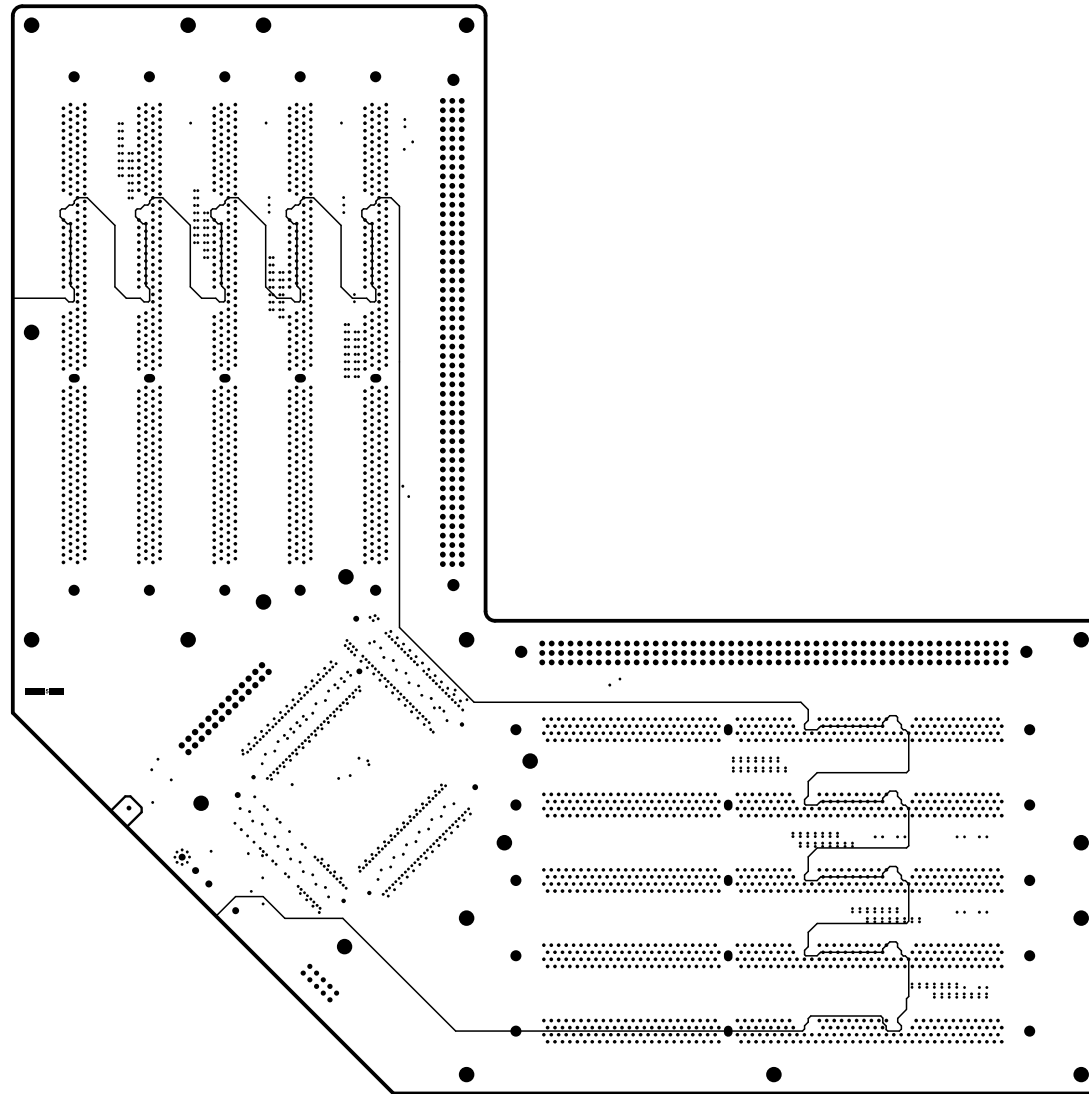
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Title: GND Plane Layer 2 GP1				



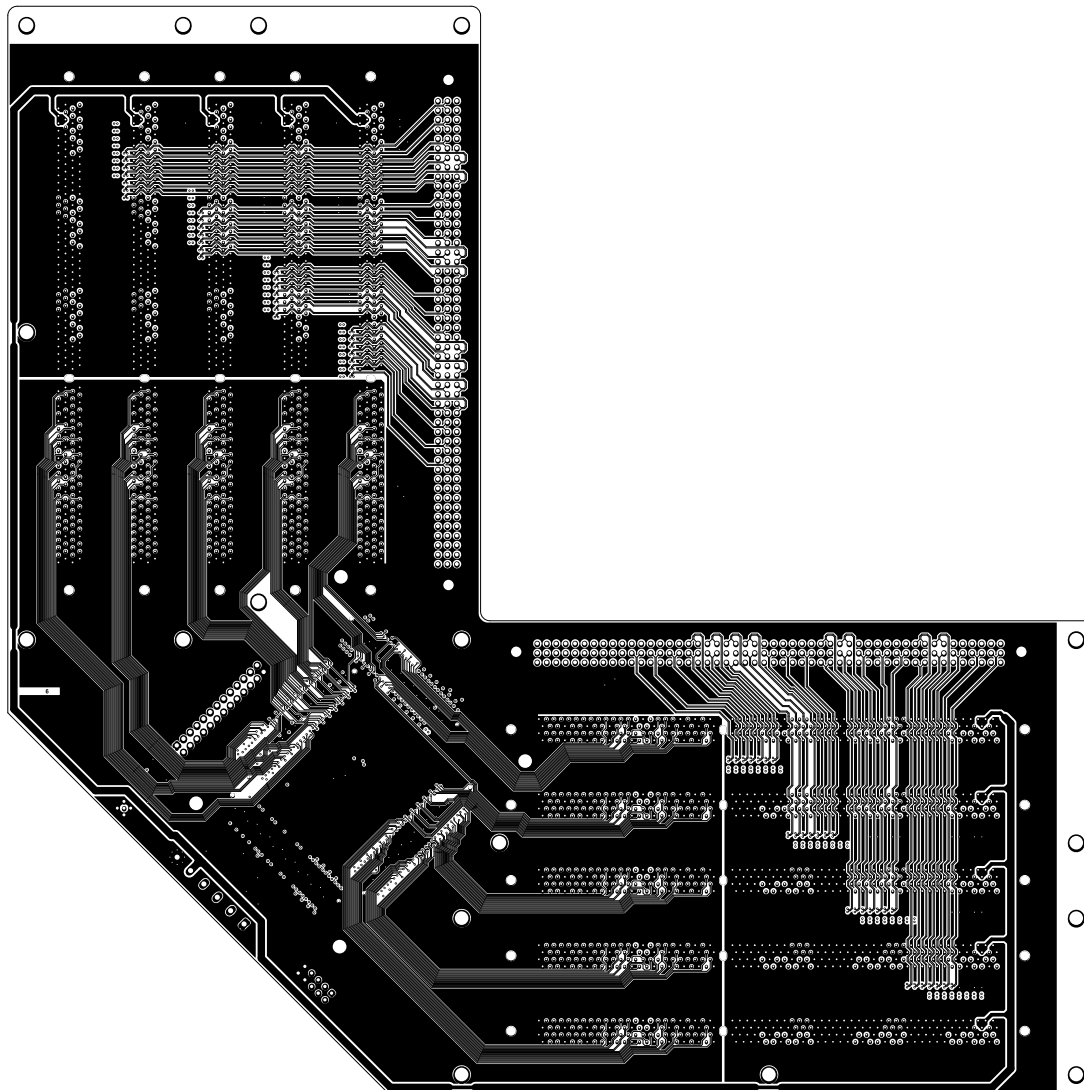
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Title: Pow/Sig Layer 3 G1				



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Title: PWR Plane Layer 4 GP2				

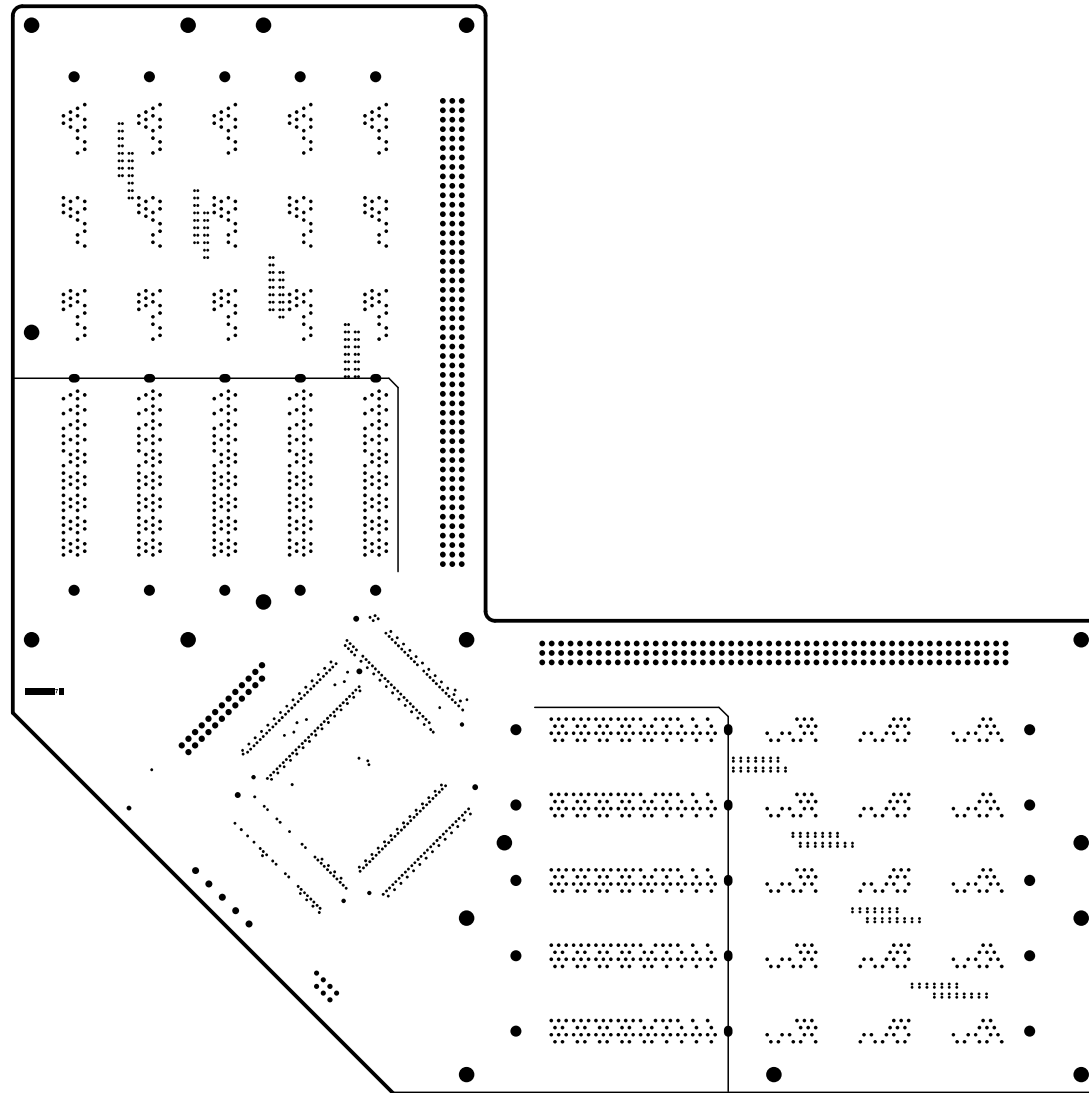


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Title: PWR Plane Layer 5 GP3				

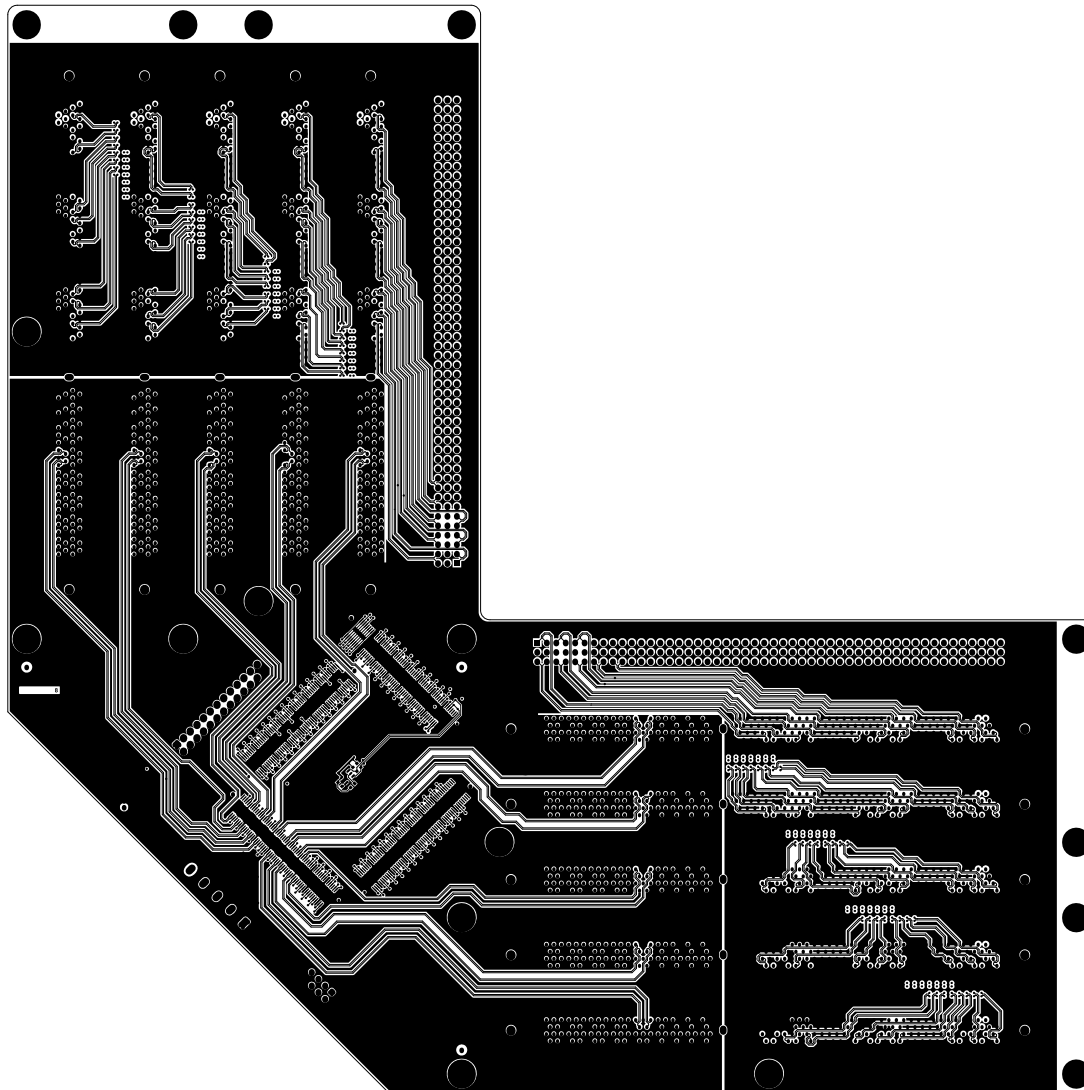


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Title: Pow/Sig Layer 6 G2				

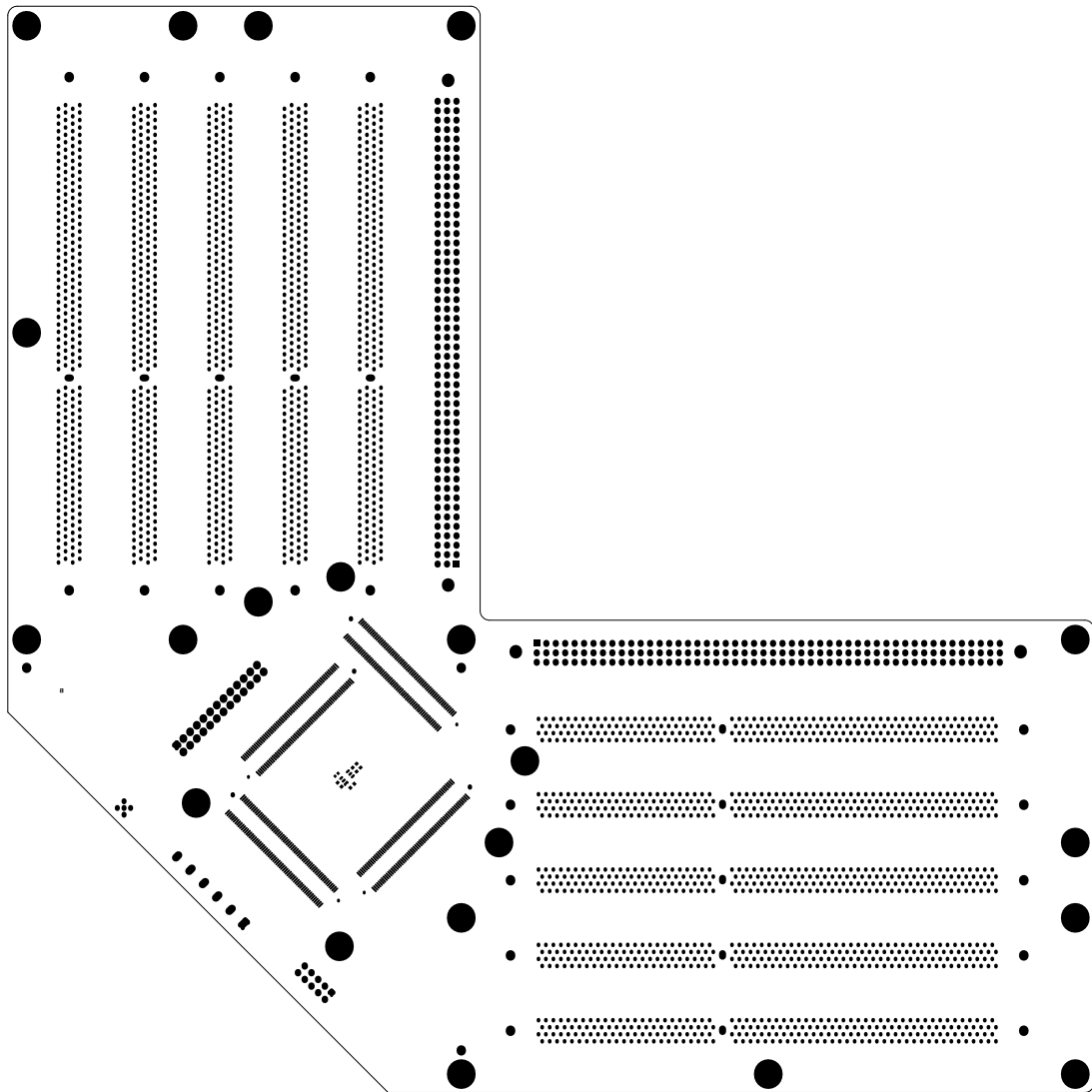




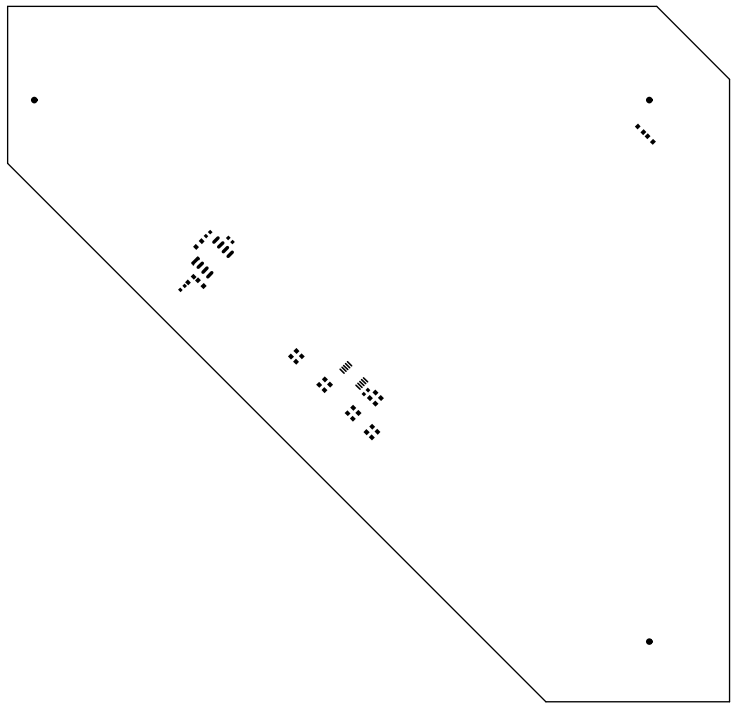
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Title: GND Plane Layer 7 GP4				



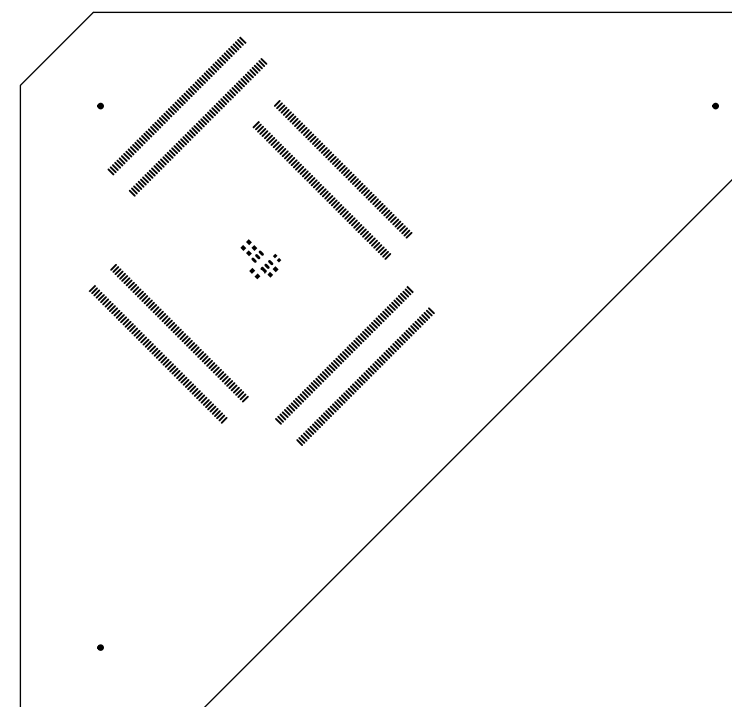
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Title: Bottom Layer 8 GBL				



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Title: Bottom Solder Mask GBS				



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Approved By: Gary S. Varner	Print Date: 13-Oct-14	Signature:	Size: A3 H	
Title: Top Paste Mask Print GTP				University of Hawaii at Manoa High Energy Physics Group Instrumentation Development Laboratory



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Title: <b>Bottom Paste Mask Print</b>				University of Hawaii at Manoa High Energy Physics Group Instrumentation Development Laboratory