TARGETX-based Electronics for WATCHMAN

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Introduction

The University of Hawaii has extensive expertise in the design of waveform sampling and digitizing application system integrated circuits (ASICs), and their implementation into corresponding systems. The UH ASIC portfolio consists both of extremely fast sampling (> 10 GSPS) for a single channel, to more moderate sampling rates for larger numbers of channels. The latter is proposed as an excellent match for WATCHMAN, with the TARGETX ASIC providing 32 channels per chip of up to 1 GSPS sampling, with over 16 μs of storage depth available at the nominal sampling rate. We describe some relevant features of the TARGETX ASIC here, along with some of its existing applications, and conclude with a short proposal of how to evaluate these electronics for WATCHMAN.

The TARGET ASICs and Applications

The TeV Array Readout Gigasample-per-second Electronics with Trigger (TARGET), was named for its original design application for next generation astroparticle observatories, such as the Cherenkov Telescope Array (CTA). Despite the name, however, the ASIC is well matched for many applications that endeavor to economically instrument large arrays of photodetectors with fast sampling. The general parameters of all TARGET chips are shown in Table 1, with detailed information and measurements available in references [1-6].

Table 1 - Parameters common to all ASICs in the TARGET series.

Parameter	Value	Unit/comment
Number of channels	16	
Sampling rate	0.4 – 1.2	GSPS
Storage depth	16,384	512 windows of 32 samples
Digitizer	On-chip	Wilkinson
Dynamic range	9-10	bits ENOB
Digitization time	2-8	μs
Trigger output		Varies by ASIC

In the CTA application, four TARGET ASICs are integrated into an assembly that mates to a Hamamatsu H10966B, 8x8 anode PMT. A photograph of an example camera module is shown in Figure 1. Example performance metrics measured in support of the CTA mission can be found in the literature [1]. Example performance metrics measured for TARGET-series ASICs for CTA are shown in Table 2.

Table 2 - Characteristics and performance of TARGET ASICs considered for CTA. Note that charge resolution is highly dependent on the photodetector and its operating conditions.

	TARGET 5	TARGET 7	TARGET C + T5TEA
Characteristics			
Number of Channels	16	16	16
Sampling frequency (Gsa/s)	0.4 - 1	0.5 - 1	0.5 - 1
Size of storage array	16384	16384	16384
Digitization clock speed (MHz)	~ 700	208	500
Samples digitized simultaneously	32 × 16	32 × 16	32 × 16
Trigger (sum of 4 channels)	integrated	integrated	companion
Performance			
Dynamic Range (V)	1.1	1.9	≥ 1.9
Integrated non linearity (mV)	75	40	≤ 70
Charge linearity range (pe*)	4 - 300	1 - ≥ 300	1 - ≥ 300
Charge resolution at 10 pe*	8%	4%	≤ 4%
Charge resolution at > 100 pe*	2%	≤ 0.8%	≤ 0.8%
Minimum trigger threshold (mV)	20	50	≤ 8
Trigger noise (mV)	5	15	≤ 1

* assuming 4 mV/pe

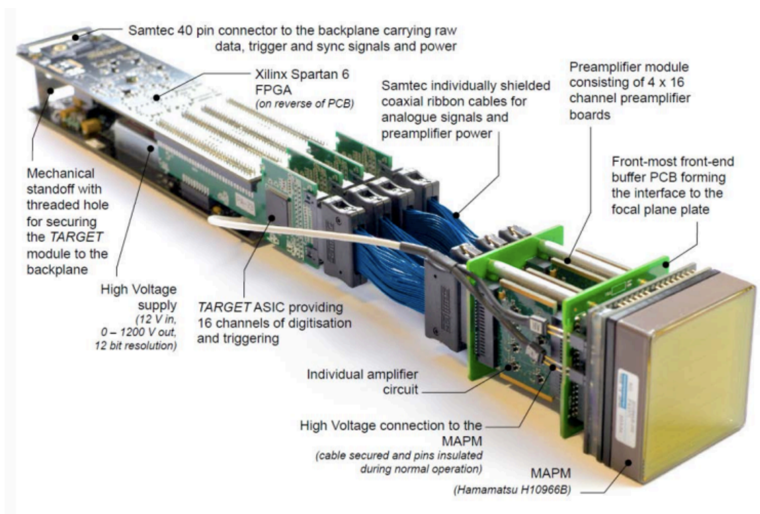

Figure 1 - A TARGET7-based camera module designed for the CTA experiment.

The TARGETX ASIC has been used to instrument over 20,000 channels of the Belle II K-long and Muon (KLM) subsystem. In this application, the TARGET captures and digitizes signals from Hamamatsu MPPCs that instrument scintillating strips. The underlying structure and capabilities of the TARGETX are identical to the TARGET7, with the main difference being how channel-level trigger bits are encoded for use by the final system. For low occupancies, where only one channel sees a hit, the TARGETX encodes the specific channel number on a 4-bit output bus. For multiple hits in coincidence, each bit of the 4-bit trigger output bus is instead used to encode a logical OR of groups of 4 channels.

Although the TARGETX was not designed for precision timing, Figure 2 demonstrates a measurement indicating that it is straightforward to reach timing resolutions under 100 ps.

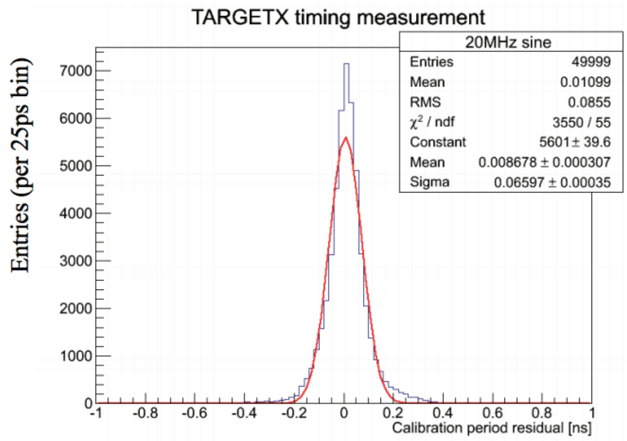

Figure 2 - Timing resolution of the TARGETX, estimated using fits to extract a period of a 20 MHz sine wave.

The University of Hawaii group has extensive experience in design for the TARGETX, as well as production testing for tens of thousands of channels. Ultimately, the TARGETX was produced in these quantities for < $1.50 per channel, making it a very economical solution, while retaining excellent timing and charge resolution capabilities.

TARGETX for WATCHMAN

The University of Hawaii proposes design of a TARGETX-based prototype to evaluate suitability for the WATCHMAN experiment. An initial crate-based design concept has been developed, shown in Figure 3. The exact input connector choice and layout would be handled on an RTM module, allowed for modular development. An initial evaluation RTM would handle 8 input BNC connections and allow for rapid immediate evaluation. A second follow-on RTM module could integrate high voltage on-board, eliminating the need for any external HV crates or systems.

Each input photodetector channel would be broken out to four channels of the TARGETX ASIC. On-board attenuators would allow four separate gain settings to be simultaneously digitized, in order to significantly extend the dynamic range of the system. The use of four channels per photodetector input would also allow individual photodetectors to provide their respective trigger primitives with no channel-ambiguity from the TARGETX ASIC, regardless of the occupancy conditions.

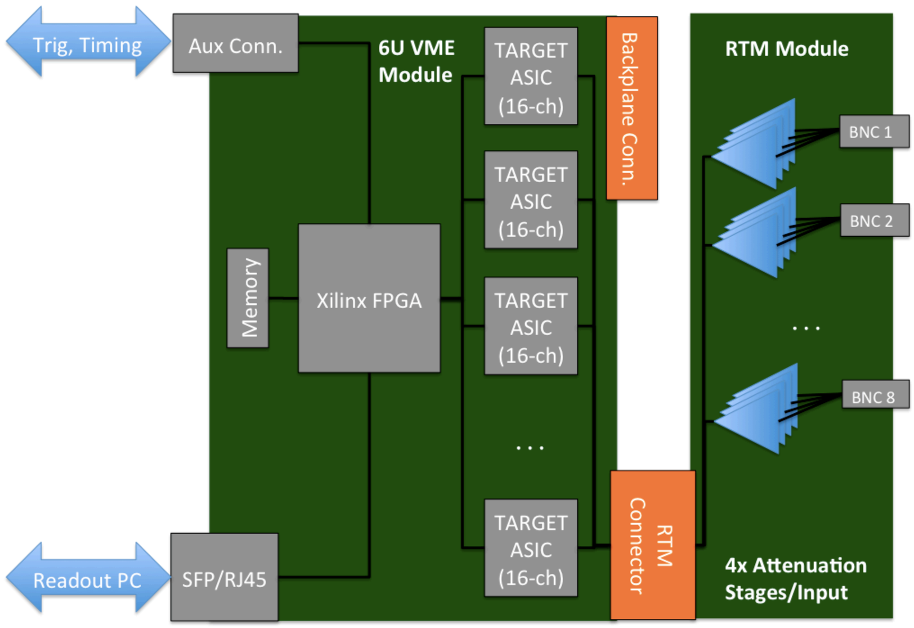

Figure 3 - Simple block diagram of a TARGETX-based evaluation platform for WATCHMAN. A future RTM module could be used to provide high voltage generation and connections in addition to signal inputs.

The ASIC would be interfaced with and read out by a Xilinx FPGA, which in turn would allow data collection and control to a readout PC via a Gigabit Ethernet connection. Existing UDP-based firmware and software would provide interfaces for initial bring-up and testing, with different or more sophisticated protocols added later via firmware modification, if required. Auxiliary connections that could be required for clock and trigger distribution can be provided on the front-panel.

While the initial readout will be focused on using the waveform capture capabilities of the system to evaluate timing and integrated charge resolutions, as well as other analog performance metrics, the full system firmware and software development would focus on firmware and software-based feature extraction to allow simplification of the full data flow. By reducing each waveform quickly to charge and time information, hits can be combined efficiently into a large data stream to allow online rejection of backgrounds.

Summary

A summary of the readout parameters described here is shown in Table 4.

Table 3 - Requested readout parameters for WATCHMAN.

Parameter	Value & Comment
Timing resolution	< 100 ps
Charge resolution	To-be-measured, < 1% achieved on CTA, but can be photodetector and operating condition dependent.
Triggering flexibility	FPGA-based control for flexible triggering
Trigger primitive	1-trigger bit per PMT, on-chip tunable thresholds
Cost per channel	$1.40, ASIC-cost per Belle II experience ~$10 per channel total in production, assuming 32-channels per board for final system.
Design lead time	6 months for initial prototype design with initial firmware, software support
Power consumption	Conservatively estimated at <1 W/channel, total, not including HV.
Maintainability	See footnote.[1]
Flexibility for other hardware	Generic connectorized input proposed for prototype. Other applications have been designed specifically for close coupling with specific detectors, e.g. MaPMTs.

[1] There is extensive experience with systems using these ASICs in a variety of systems, so documentation and training could easily be provided. As an example, a TARGET-based system intended to be deployed down a borehole [7]. Firmware and software were frozen prior to a prototype deployment, and non-experts were able to operate the system stably for months in an underground facility, based on the instructions provided. Sufficient spares (5-10%) would be produced to allow rapid swapping of modules should any fail, and the independent design of the core module and the RTM module allow for reduced overhead of board failures.

References

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