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**Meeting :** Tuesday, 9th of October 2018, Week 4

**Participants:**

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**Gary:**

Register map update of TARGETC

1 .. 64	VdlyTune
65	SSToutFB
66	SSPin LE
67	SSPin TE
68	WR_STRB2 LE
69	WR_STRB2 TE
70	WR_ADDR_Incr2 LE
71	WR_ADDR_Incr2 TE
72	WR_STRB1 LE
73	WR_STRB1 TE
74	WR_ADDR_Incr1 LE
75	WR_ADDR_Incr1 TE
76	MonTiming SEL
77	Vqbuff
78	Qbias
79	VtrimT
80	Vbias
81	VAPbuff
82	VadjP
83	VANbuff
84	VadjN
85	Sbbias
86	Vdisch
87	lsel
88	Dbbias



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89	CMPbias2
90	Pubias
91	CMPbias
92	Misc Digital Reg
93 .. 127	unused
128	TPGreg

Jose will update it to the idlab webpage.

Misc Digital Reg is a 5 bits register, needed to be all at one to have disabled and in normal operation.

Vbias is for the buffer from sampling to storage capacitor

**Ky:**

Tried the TCL script, problems the user\_ips are not integrated to the IP catalog in Vivado and they are locked. UART was missing. Vasily can help, he has a TCL script for generating the bd maybe a good solution.

**Anthony :**

Working on the UDP and Python GUI.

**Kurtis :**

Next Summer, a test for PMTs is going to take place and we should have our hardware ready to test them and characterize them. We need a connection board between PMTs and our boards.

**Schedule :**

November, have prototype ready. Keep documentation and scripts commented for anybody to use them.

December, order the new board (4 ASICs and 1 ultraZed) for January,

**Overall question :**

The new boards need to be designed and thought on. Power supplies surveillance, log files on sdcard,... Should the card reboot if major problem or after loss of connection over certain period of time.

**Documentation :**

Simple mistake with the register map, if documentation was kept up-to-date.

GitHub Wiki > Use ReadMe.md for specific

IDL Webpage > Update it to have register map, layout/schematics of TargetC blue boards.

TargetC Datasheet > needs update and changes will be posted soon too.

>> Everybody keep your documentation up-to-date and share it, for the project to advance!!

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**TODO:**

- Jose                      Incharge of updating IDL Webpage and Wiki on Github. (All documentation in one place and it is on the webpage).  
Add the MoMs from last week too.  
Diagram/Schematics of Test plan for next summer testing
  
- Vasiliy                  Register read from TargetC
  
- Jonathan                Send the MoMs to Jose for Update on the Webpage  
Update Documentation on the TARGETC  
Register read from TargetC
  
- Ky                        Merge projects (AXI Stream, UDP)
  
- Anthony                Working on Prototype GUI