Project: WATCHMAN
University of Hawaii at Manoa

Meeting : Tuesday, 25th of September 2018, Week 2

Participants:

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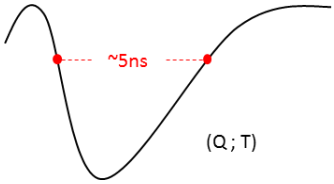
Diagram:

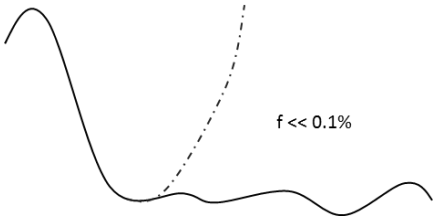
Jose made a data flow diagram. We need to concentrate on the top part (TargetC to PS), get a simple readout prototype in place.

The TARGETC readout will pass through a "De-serializer" and then the data will be stored in a FIFO per window. A select system shall be possible to select which channel from the 16 is of interest or all.

- Frequency of data transfer : max 15kHz (optimal 10kHz).
- Two type of transfer data depeinding on trigger width :
  - Feature Extraction (charge ; time) -> 48 bits



  - Full wave: 2 windows of 32 samples of 8-12 bits -> 64-96 bytes

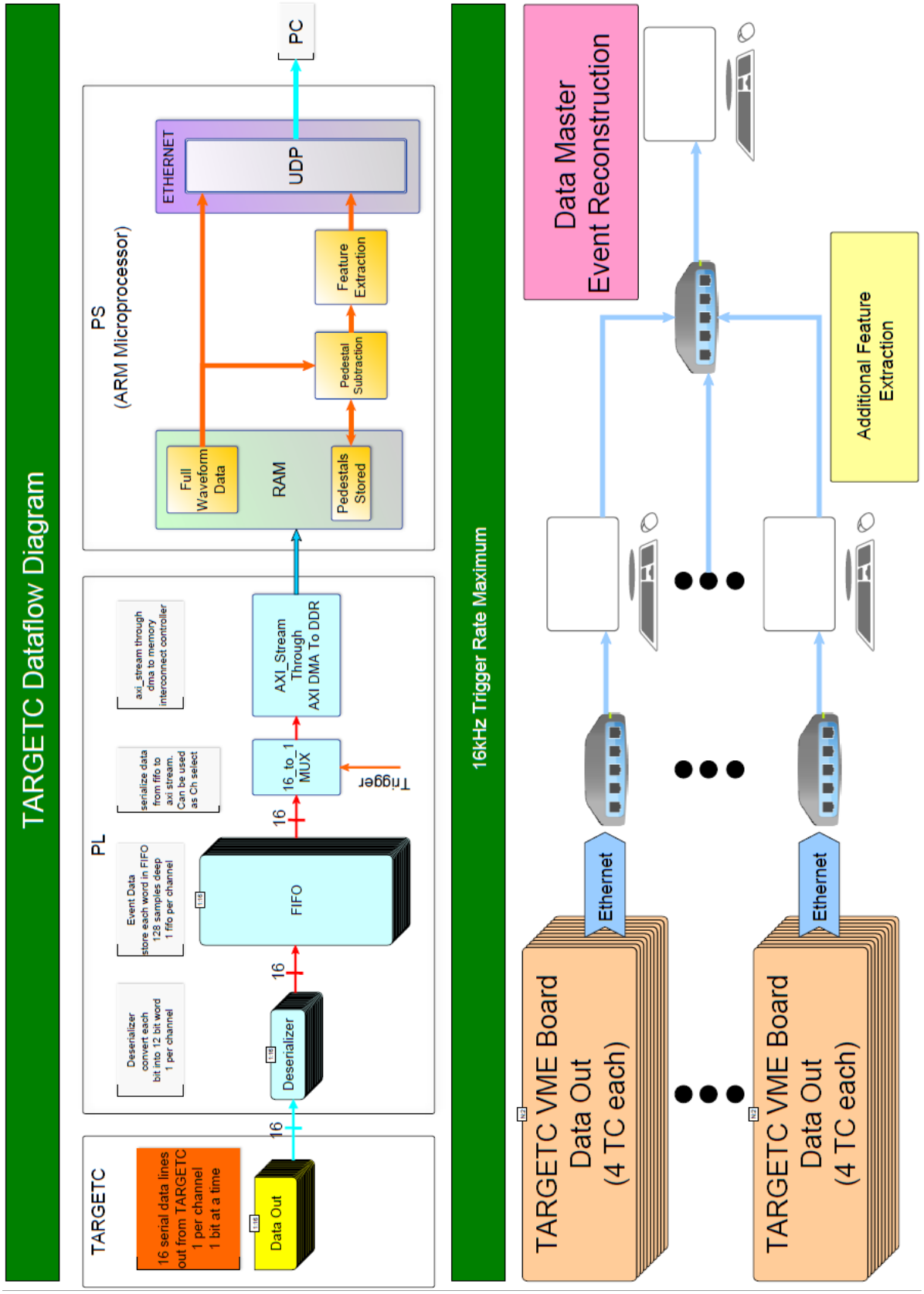


Numbers from the DAQ Meeting Sep 15-17, 2018

First architecture for basic readout capabilities will integrate the feature extraction and pedestal in the PS side of the Zynq 7Z010.

The pedestal extraction from Kurtis document showed that Pedestal extraction took ~3.6 us which is 555khits/s.

Looking at the overall system the tank will count 4000 PMTs.


TARGETC Dataflow Diagram
TARGETC
16 serial data lines out from TARGETC 1 per channel 1 bit at a time
Data Out
16
PL
Deserializer convert each bit into 12 bit word 1 per channel
Deserializer
16
Event Data store each word in FIFO 128 samples deep 1 fifo per channel
FIFO
16
serialize data from fifo to axi stream. Can be used as Ch select
16_to_1 MUX
Trigger
axi_stream through dma to memory interconnect controller
AXI_Stream Through AXI DMA To DDR
PS
(ARM Microprocessor)
RAM
Full Waveform Data
Pedestals Stored
Pedestal Subtraction
Feature Extraction
ETHERNET
UDP
PC
16kHz Trigger Rate Maximum
TARGETC VME Board Data Out (4 TC each)
Ethernet
TARGETC VME Board Data Out (4 TC each)
Ethernet
Data Master Event Reconstruction
Additional Feature Extraction

GITHub

Structure is in place and running

Vivado Projects are taking a lot of place and path don't always work. Maybe a better way to share such projects.

Vasiliy has to get on GitHub.

Jose setup a tasklist on GitHub : https://github.com/WMidlab/WATCHMAN/projects/1

TODO

Jose	I2C Module prototype Assembly another TARGETC Board
Anthony	Benchmark max data packet length and speed
Jonathan	AXI Stream TestBench
Ky	Read/Write Register with AXI-Lite on the PL from PC thourgh Ethernet
Vasiliy	Get on github Upload code that works Register read from TargetC
Others	JTAG-HS2 and MicroZed board ordered last week (19th of September) Next Moday (1st of October) DAQ Meeting, WATCHMAN Team can join.