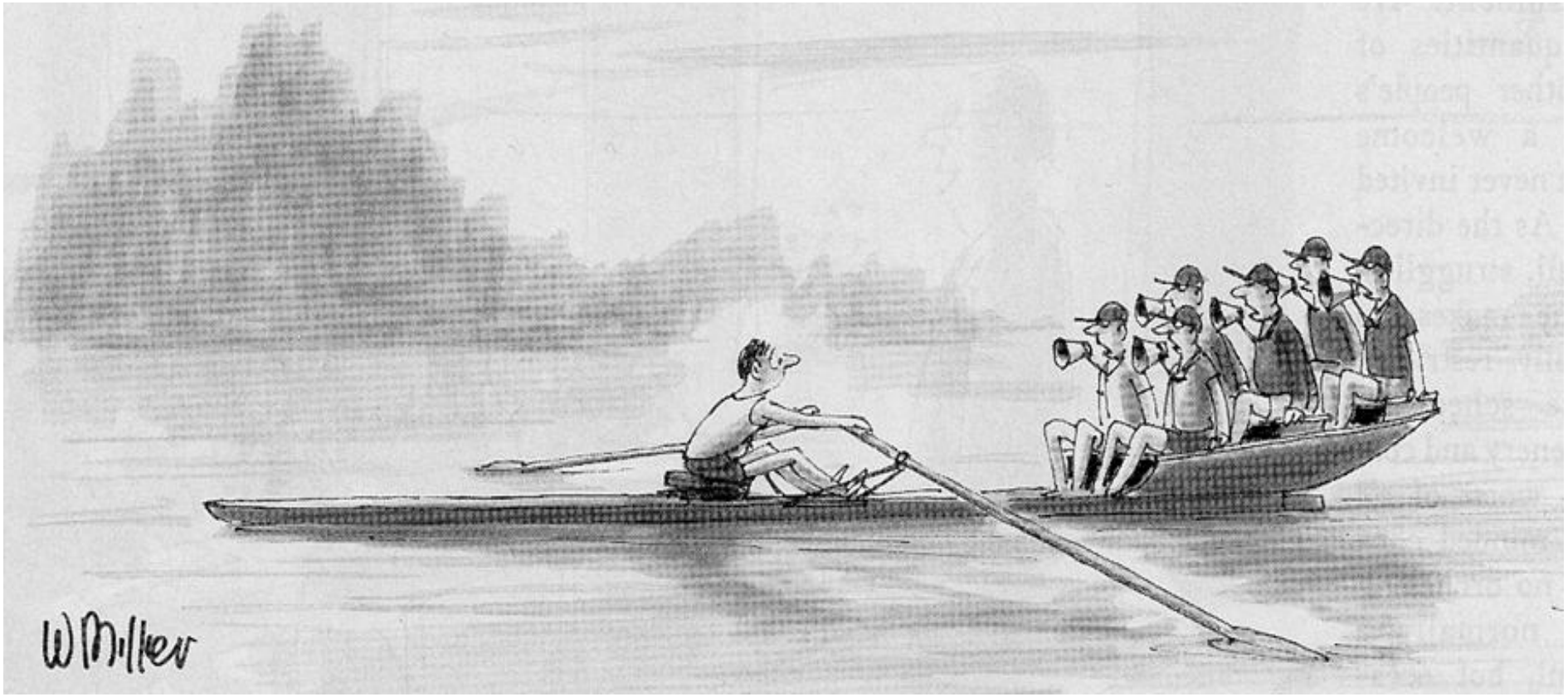
mTC recommendation



G. Varner

June 22, 2014 (nihon)

Executive Summary

• Each new generation of complex ASIC takes time to work out the wrinkles

• And much of the problem isn't the ASIC per-se, but accompanying circuitry, firmware and user knowledge

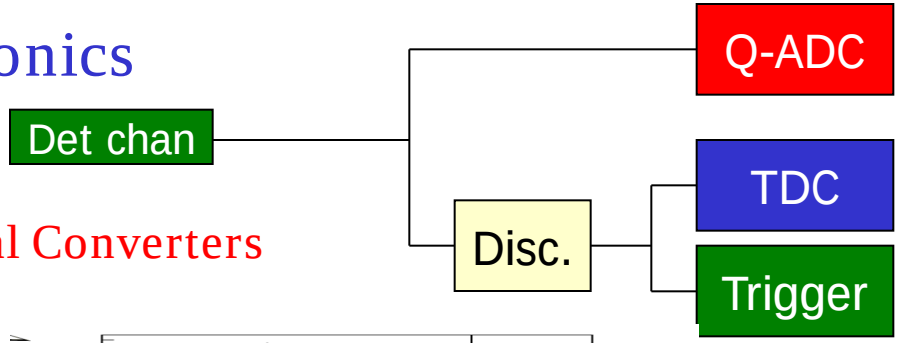
• The IRS family is unique:

- **Much deeper storage depth (worldwide unique)**
- Hardware timebase correction
- On-chip, massively parallel ADC
- Built-in, low-threshold triggering

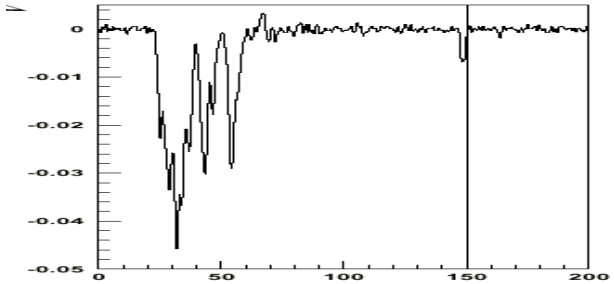
• It has taken time, but we are finally there. Let's put this in perspective

Detector Instrumentation Evolution

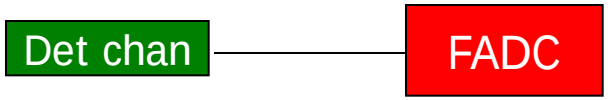
- Traditional "crate based" electronics
  - Gated Analog-to-Digital Converters
  - Referenced "triggered" Time-to-Digital Converters



- High-rate applications
  - "pipelined operation"
  - Low-speed, low-resolution sampling



- High channel counts
  - Motivation to reduce cabling
  - Integrate electronics onto detector elements



Issues: cost, power, resolution, data volume

WFS Calibration – a history

- Switched Capacitor Array waveform sampling has tremendous advantages in compactness, cost, power, cabling, etc.
- No free lunch theorem applies – have to learn how to operate/calibrate them due to timing/voltage non-linearities

ANITA: Engineering flight

- Sampling unstable
- Thermal, control loop problems (x2, /2 sampling on some ASICs)
- 200-250ps “asymptote”
- “had” to make it work – alternatives weren’t viable

Circa 2005

“Phase 1”

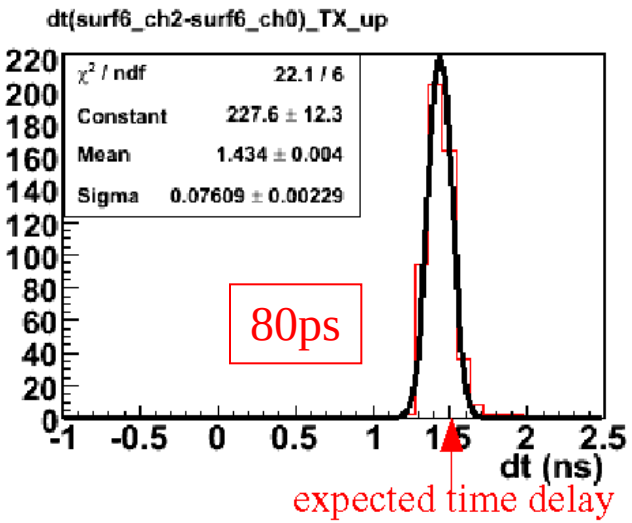
ANITA: second pass – 80 – 150 ps

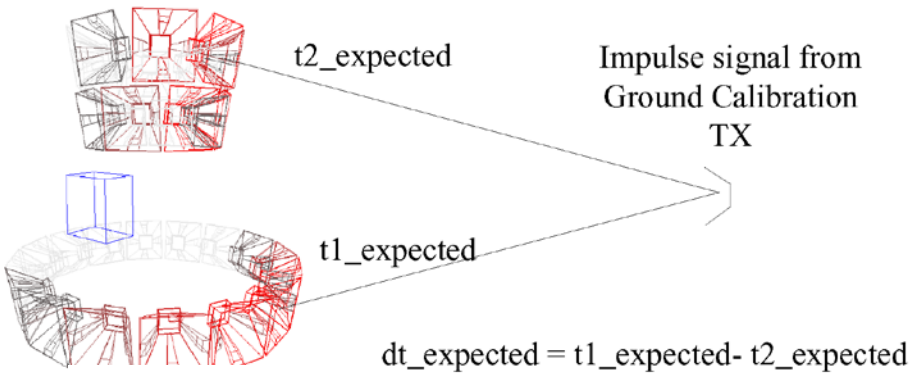
TX Up by 1.56 m

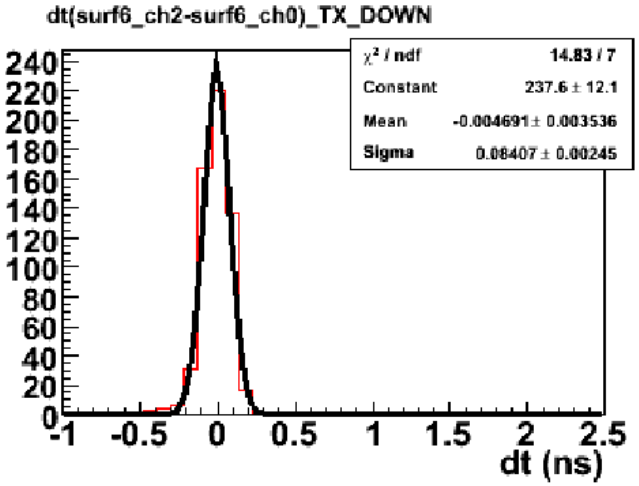
Vertical Angle Dependency

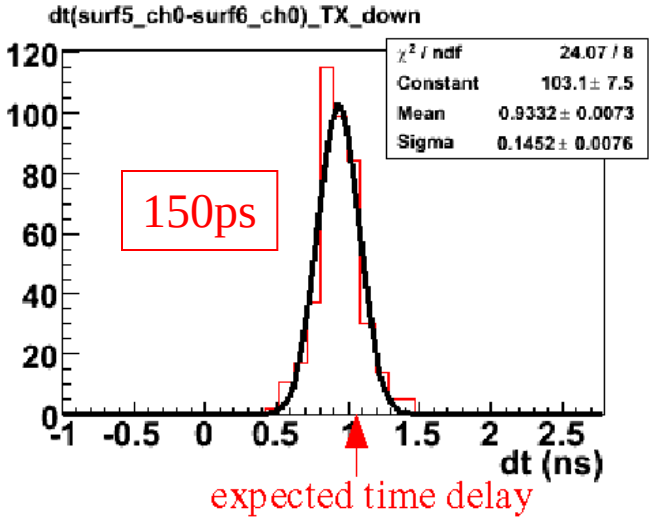
TX Down

Summer 2006









"Phase 2"

Face to TX ← Horizontal Angle Dependency → Off by 1 Antenna

ANITA: third pass – 30 (16) ps

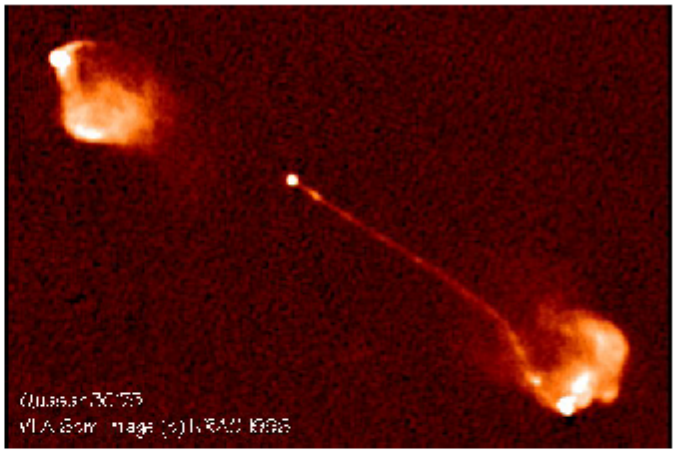
"Phase 3"

Ultrawide-band Interferometry

-Interferometric technique applied by radio astronomers.

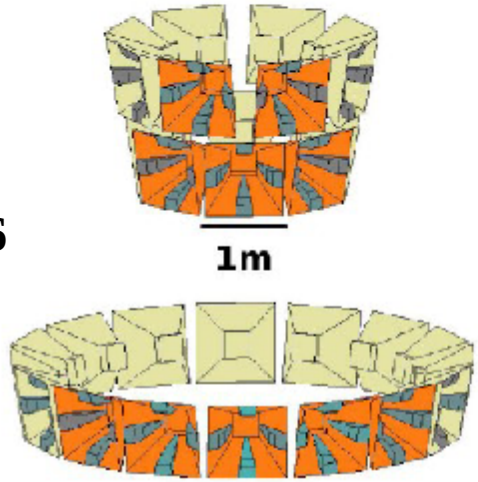
-They use single narrow band frequency.

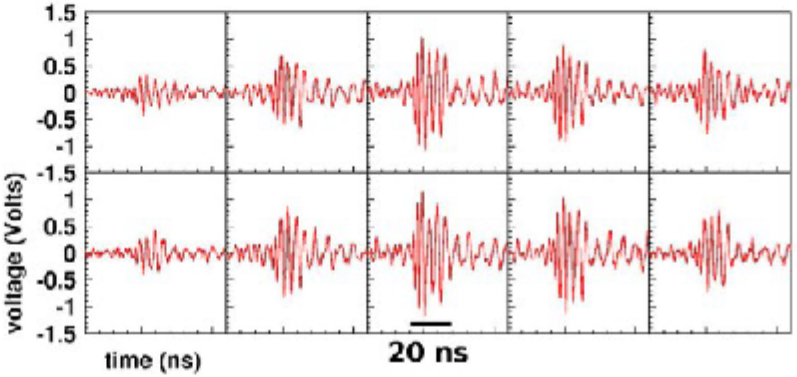
-More interested in source imaging rather than point source direction reconstruction.



Produce Ultrawide-band Interferometric Images with ANITA

Winter 2006



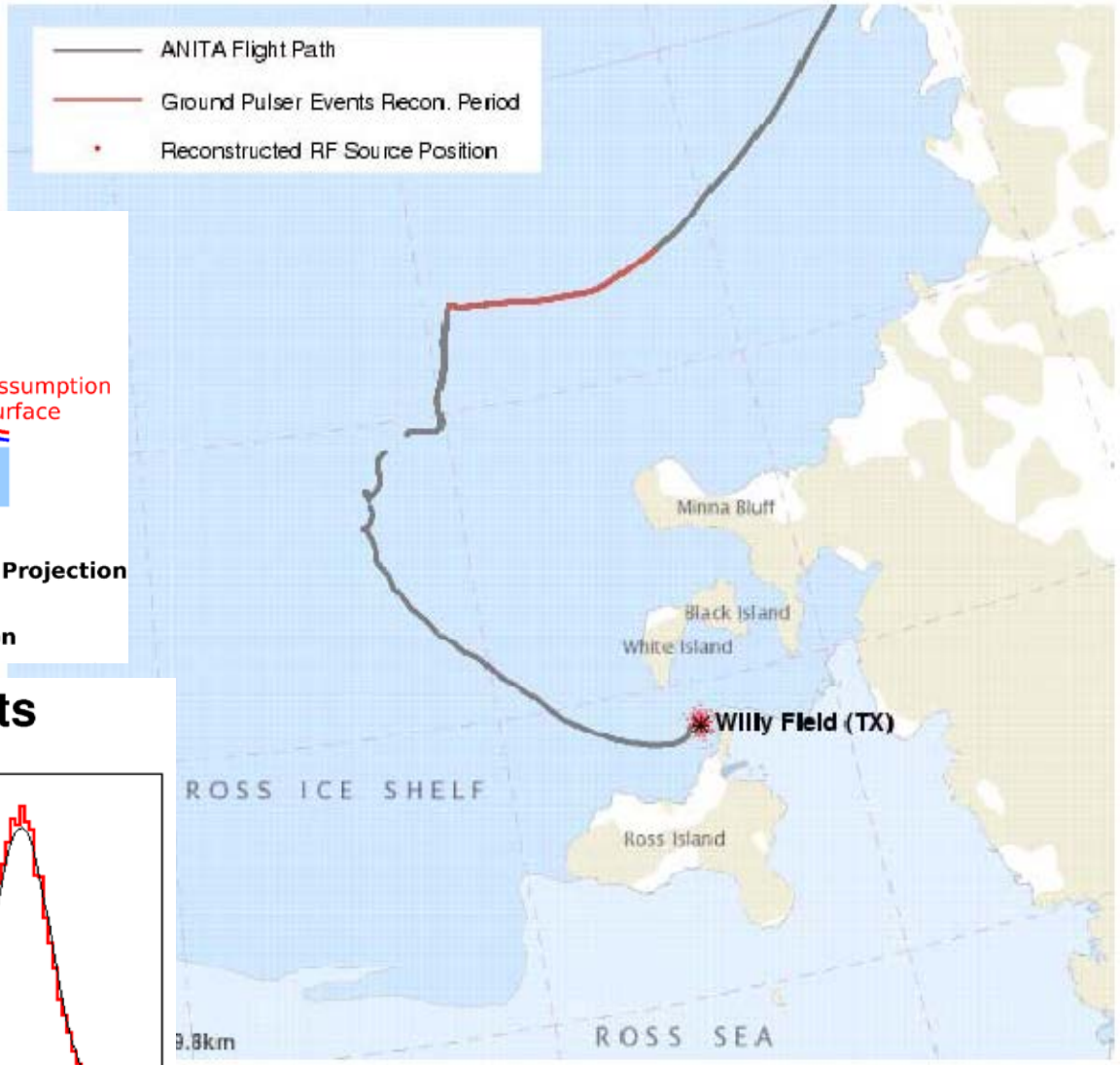


With distributed clock → **~30ps (16ps) resolution between channels**

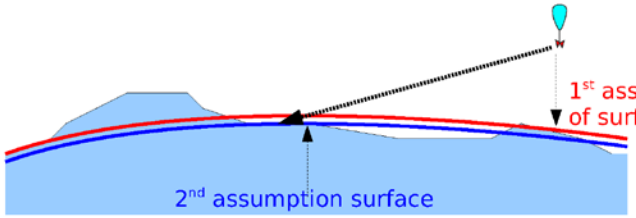
Not just on the bench – in the field

After full calibration – 100's km downrange

<30ps timing



RF Projection onto the surface



Fast Algorithm: Line Sphere intersection

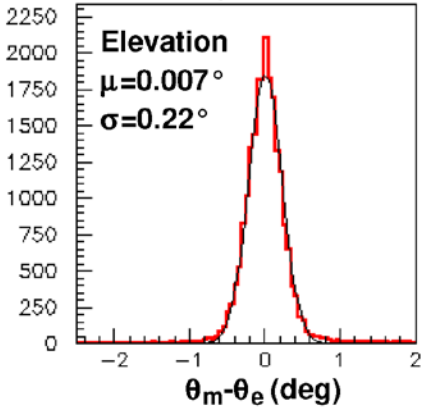
1st R_{earth} =Geoid + Surface @ Ballon position -> Rough Projection

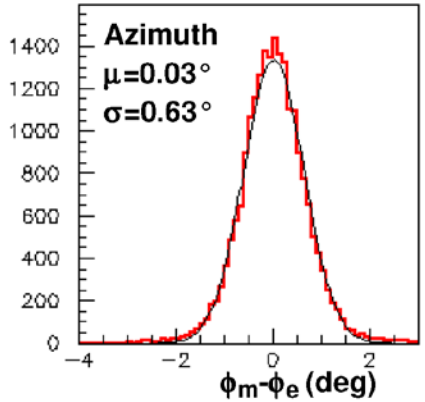
2nd R_{earth} = Geoid + Surface @ (position from 1st)

3rd: one more iteration -> converged after 2nd iteration

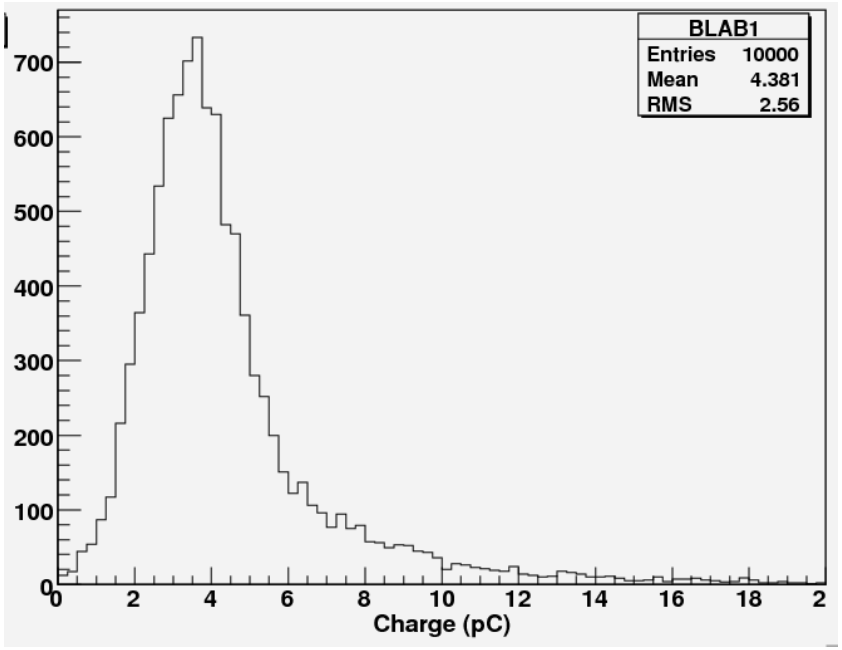
V-pol results

Borehole Data (used for calibrations)

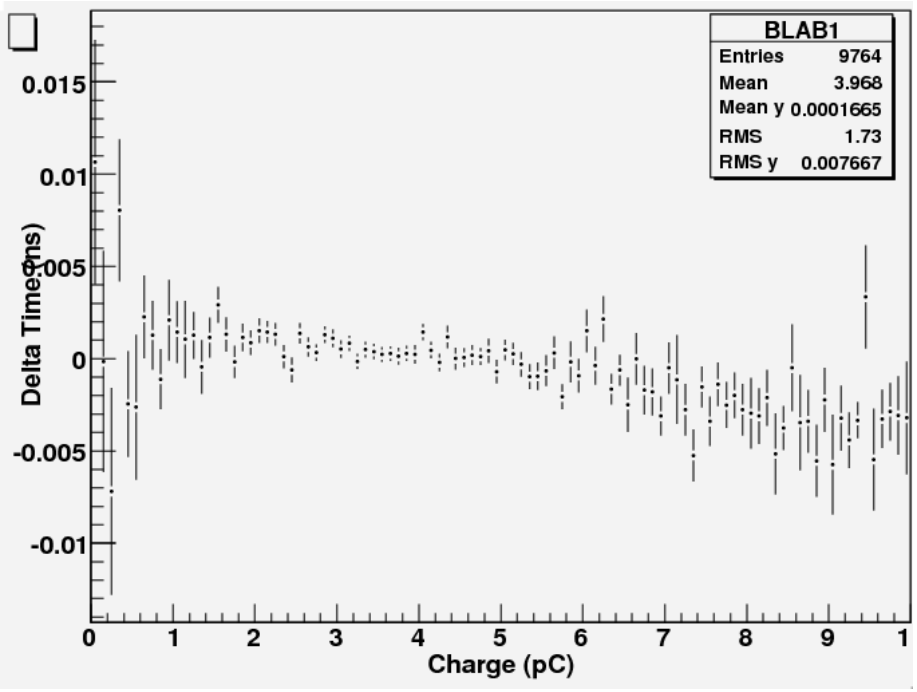


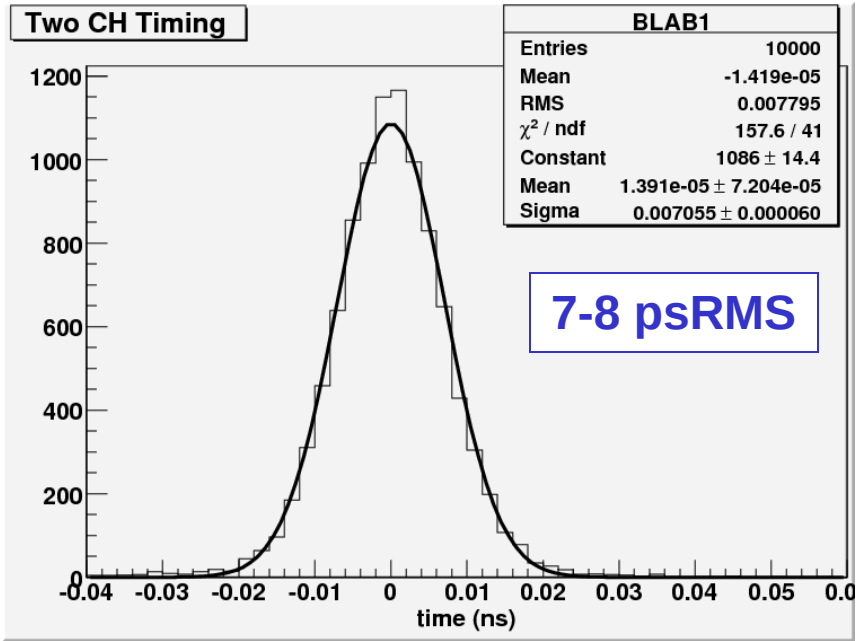


Laboratory Environment: real MCP-PMT Signals



Residual Time Walk

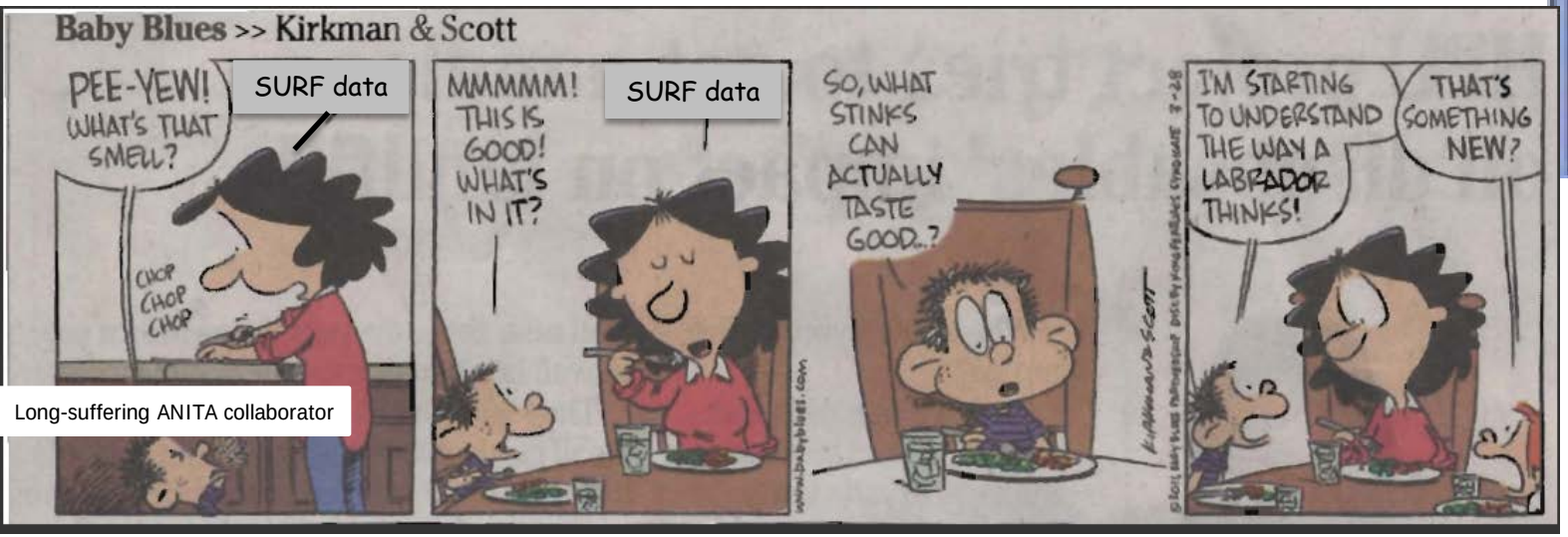




7-8 psRMS

Rather robust for amplitude invariant signals, and infinite SNR (no distributed clock)

Learning to how to deal with



Long-suffering ANITA collaborator

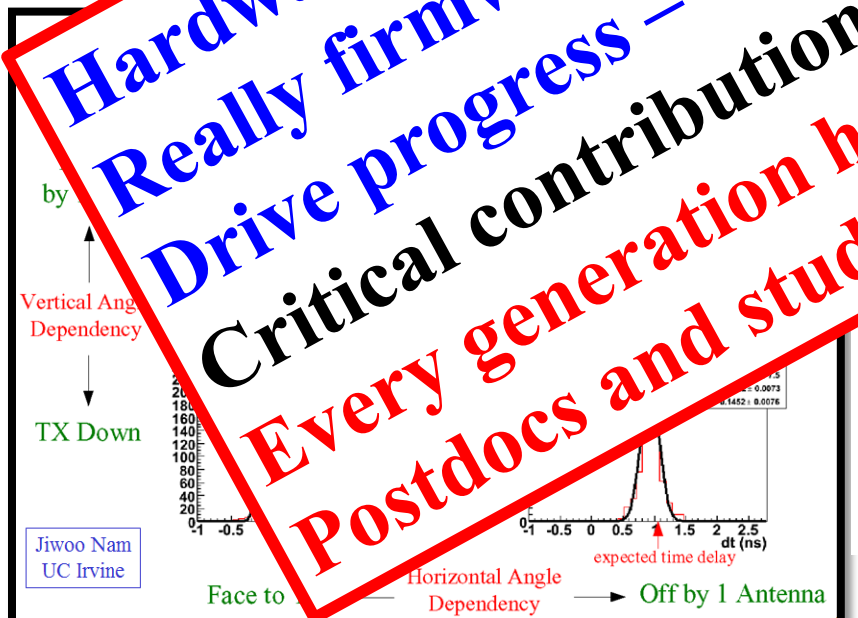
A comment on 3 phase

WFS Calibration – a history

- Switched Capacitor Array waveform sampling has tremendous advantages in compactness, cost, power, cabling, etc.
- No free lunch theorem applies – have to learn how to operate/calibrate them due to timing/voltage non-linearities

ANITA: Engi… e 1)

- Sampling…
- T…

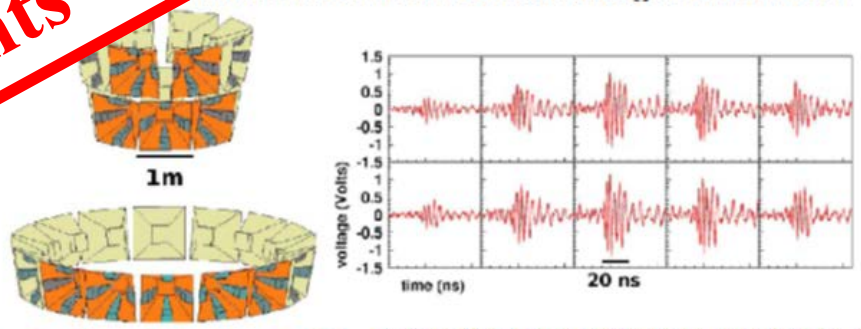


Jiwoo Nam
UC Irvine

Hardware visible, but
Really firmware/software tools
Drive progress – Calibration
Critical contributions = young people
Every generation have to train a new generation
Postdocs and students … takes time

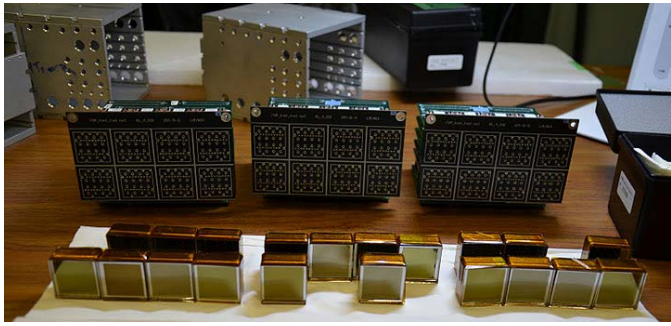
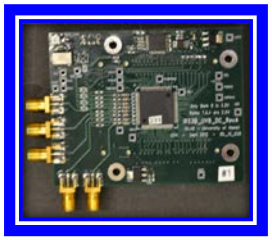
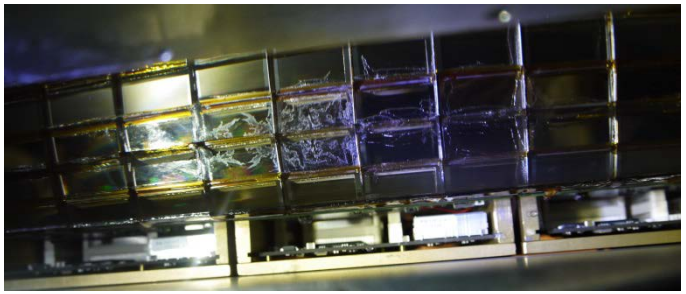
- **(low Earth orbit)**

…wide-band Interferometric Images with ANITA

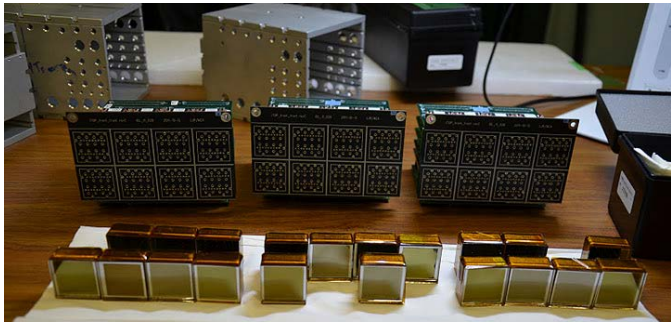
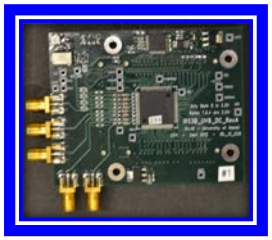
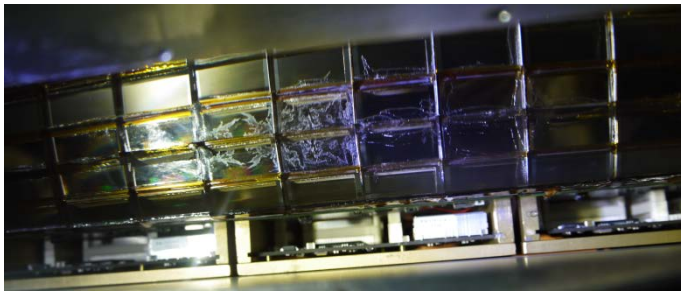


With distributed clock → **~30ps (16ps) resolution between channels**

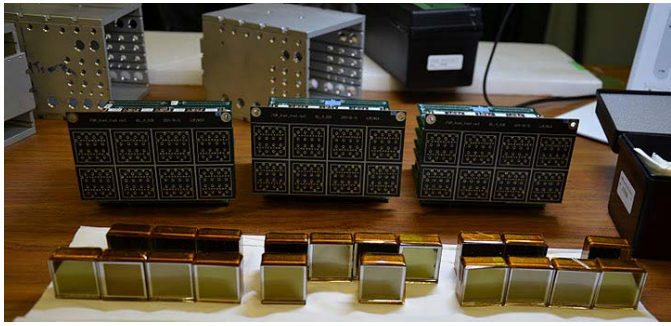
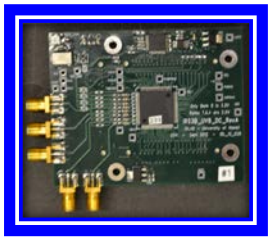
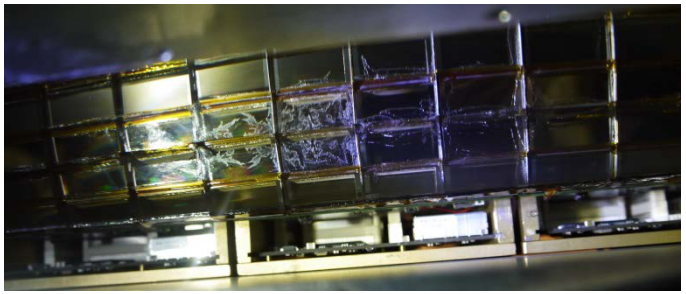
Development Timeline (ASIC)

ASIC	Dates	Milestone(s)	Hardware
BLABx	< Spring ‘11	Prototyping	
IRS2	Summer ‘11 – Winter 12	**FNAL beamtest**	
IRS3/ others	Spring ‘12 – Winter 12	Semi-infinite reviews	
IRS3B	Spring ‘13 – Summer 13	**LEPS beamtest**	

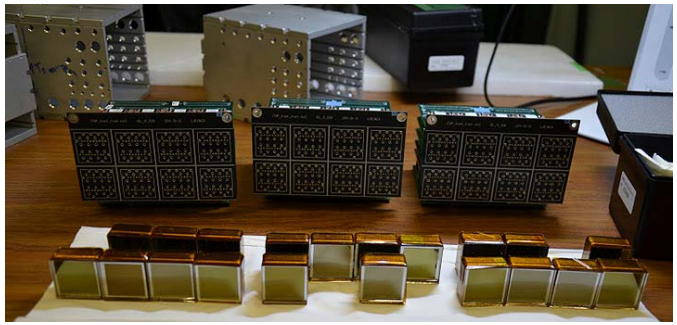
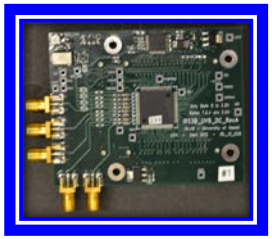
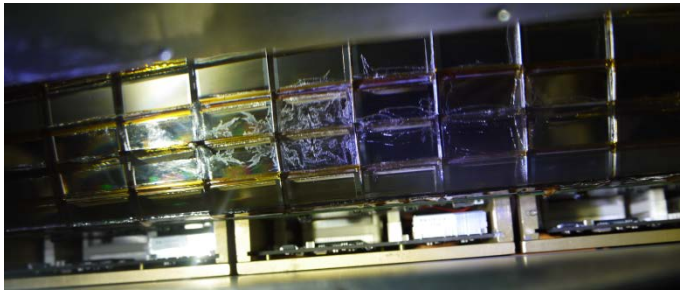
Development Timeline (critical)

Firmware	Dates	Milestone(s)	Hardware
	< Spring ‘11	Prototyping	
v. 0	Summer ‘11 – Winter 12	**FNAL beamtest**	
v. 1	Spring ‘12 – Winter 12	Semi-infinite reviews	
v. 2 v. 3	Spring ‘13 – Summer 13	**LEPS beamtest**	

Development Timeline (software tools)

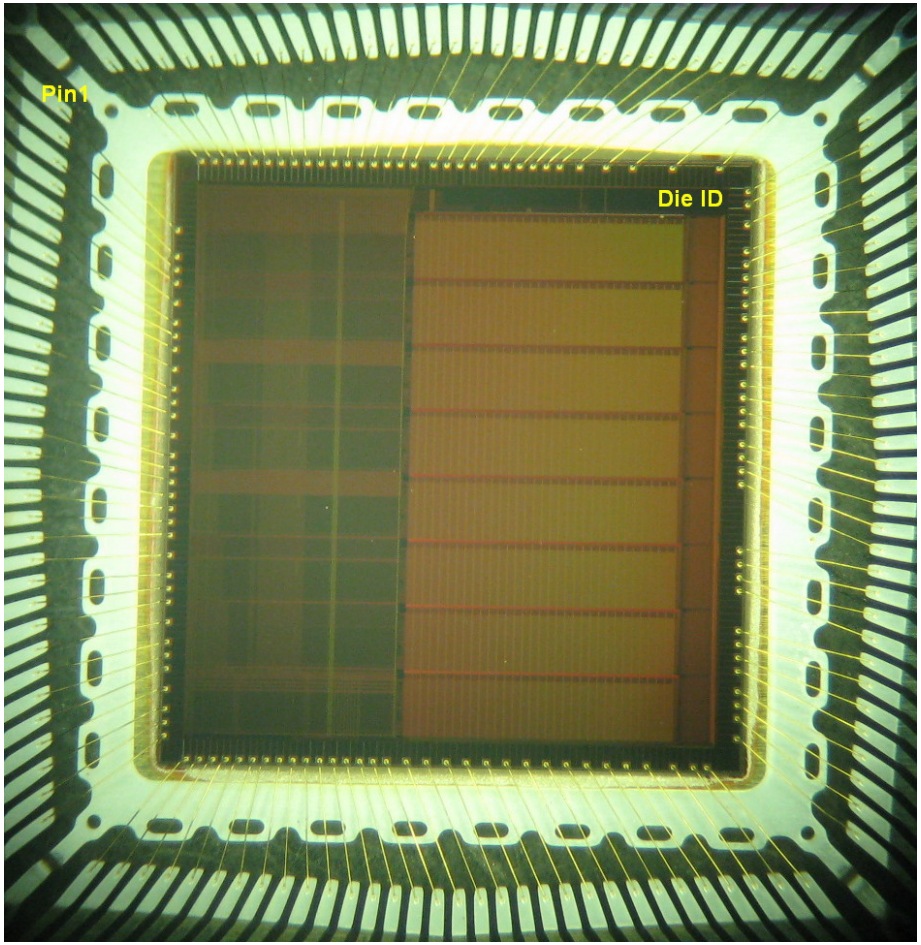
S/W	Dates	Milestone(s)	Hardware
	< Spring ‘11	Prototyping	
Ad hoc	Summer ‘11 – Winter 12	**FNAL beamtest**	
	Spring ‘12 – Winter 12	Semi-infinite reviews	
v. 0	Spring ‘13 – Summer 13	**LEPS beamtest**	

Completion Timeline

	Dates	Milestone(s)	Hardware
	< Spring ‘11	Prototyping	
Phase 1	Summer ‘11 – Winter 12	**FNAL beamtest**	
	Spring ‘12 – Winter 12	Semi-infinite reviews	
Phase 2	Spring ‘13 – Summer 13	**LEPS beamtest**	
	Summer ‘14	**v. 4**	**IRS3D/IRSX** **v.1 RT recon** **Final boardstack**

IRS3D/IRSX

• Baseline ASIC for production (~670 were fabricated in pre-production run [March 2014])

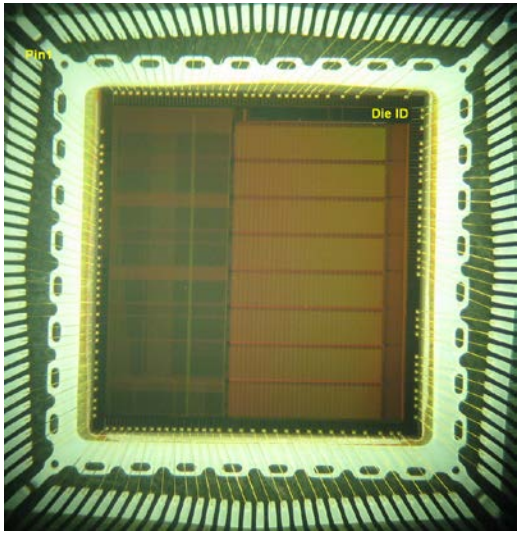


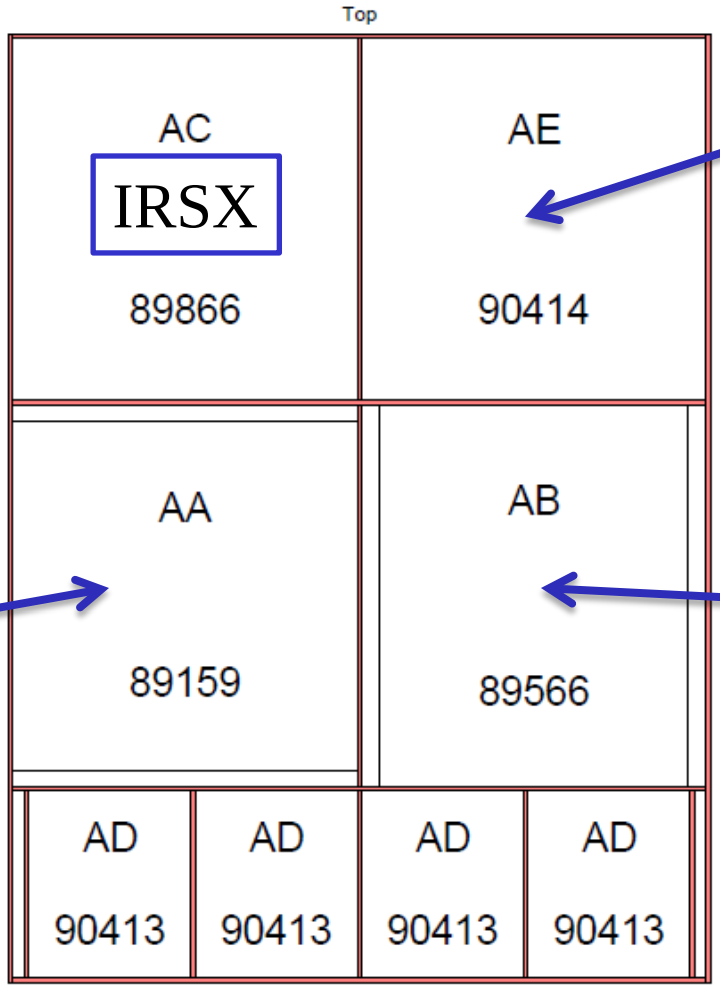
2.6M transistors, 7.7k resistors (DACs)

• High-speed, lower power/EMI LVDS outputs for fast, asynchronous signals
• Extended dynamic range comparator
• Lower-power Gray Code Counter and internal DLL demonstrated (TARGET7)
• IRS3D takes the internal improvements, but keeps simplified IRS3C user I/O

TSMC Production Run

- Files at MOSIS, start once PO received (end June, 2014)





IRS3D

IRS3C

TARGETX

Now have the masks, will make run of 25 wafers

Should receive on the order of 1500 each

Reticle Layout

IRSX/3D Improvements over IRS3C/3B

1. Improved Trigger Sensitivity
2. Timebase Servo-locking
3. dT hardware adjust
4. Improved linearity/dynamic range
5. Improved Wilkinson ADC

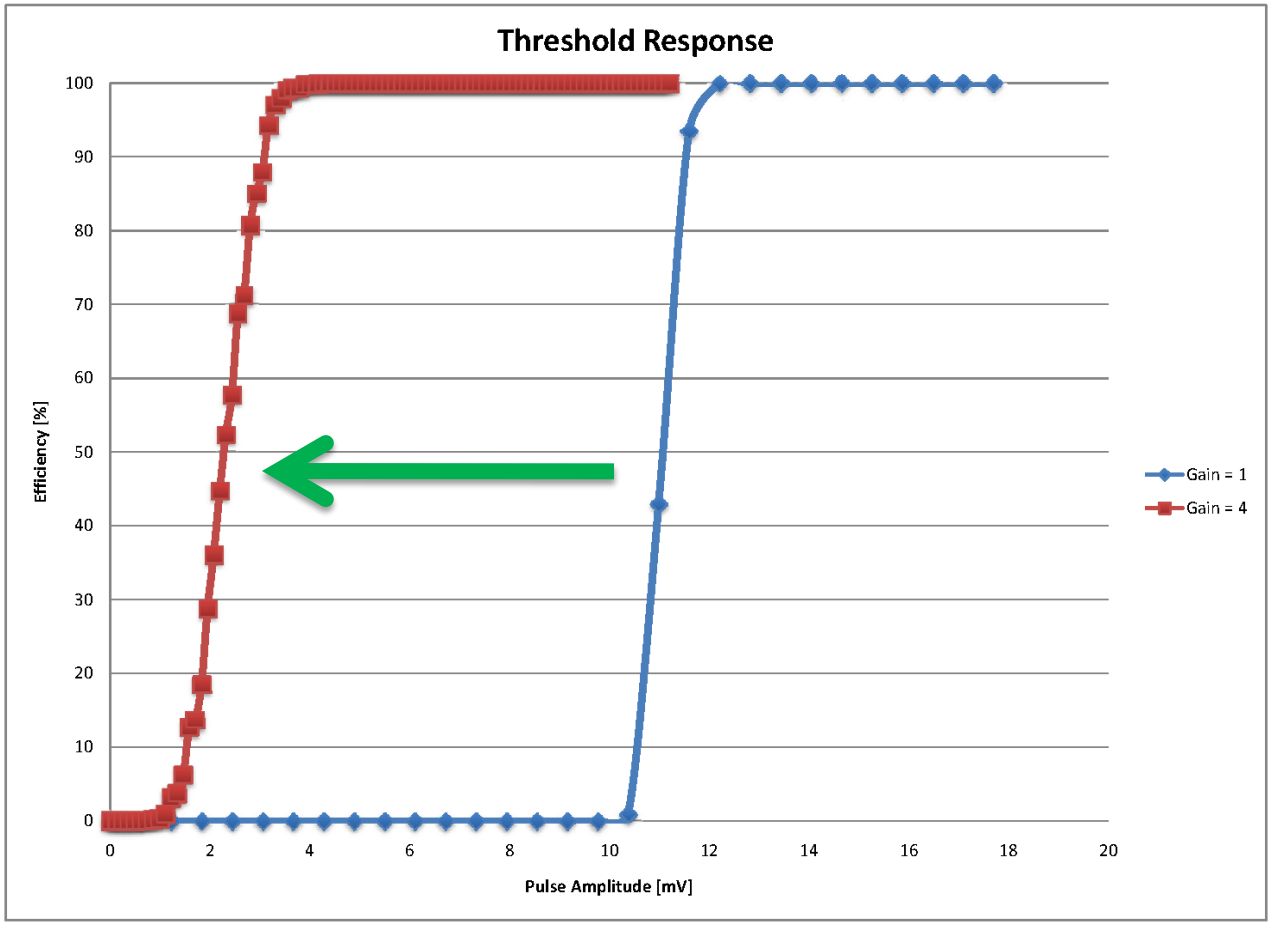
= originally reported for TARGET7/X

= demonstrated initially (TARGET7/X), detailed timing confirmed

= LABRADOR4 also

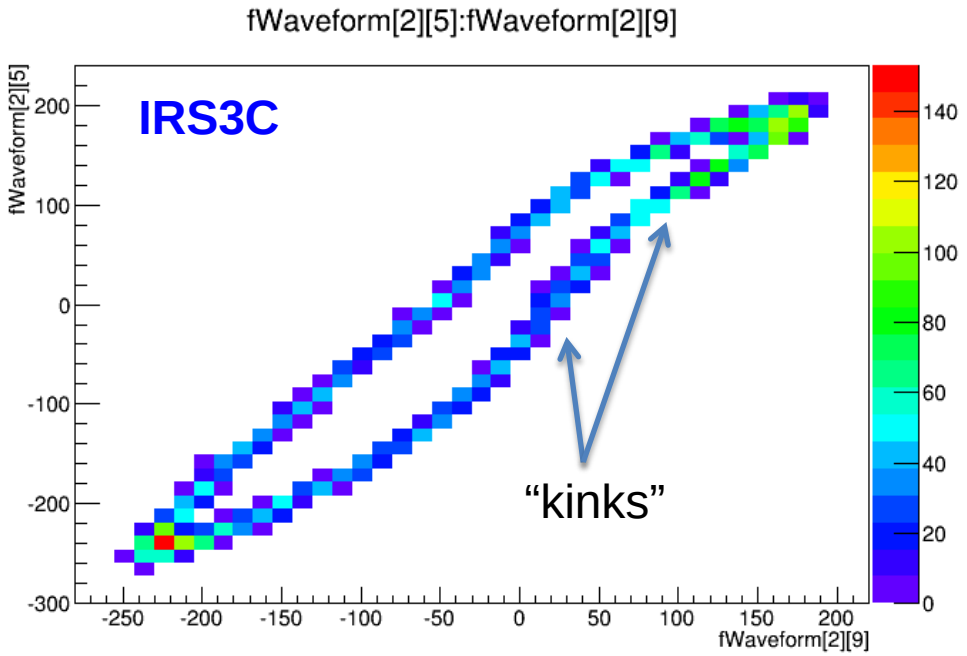
Trigger Improvement (IRS3D)

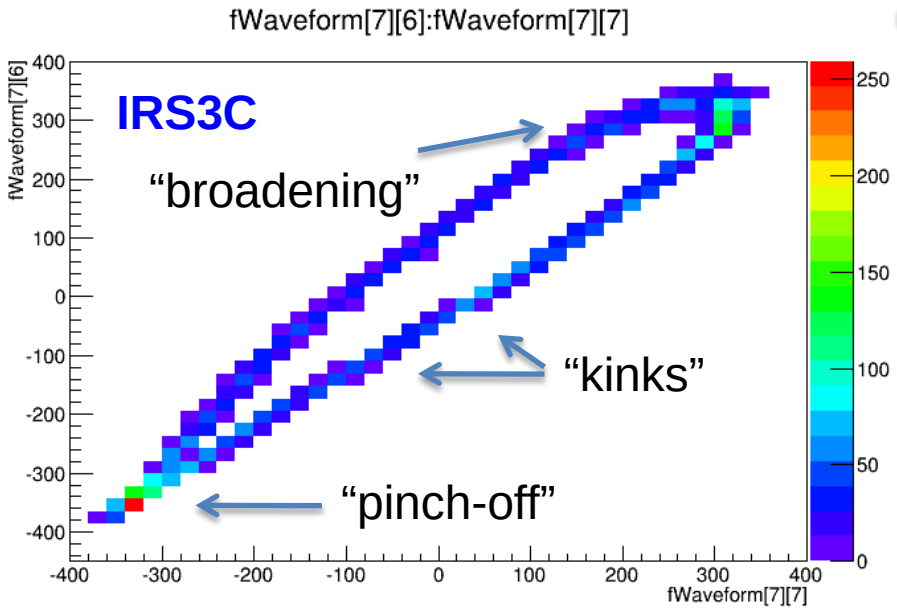
- A significant improvement for smaller pulses where “first strike” initiation of the MCP charge development is retarded



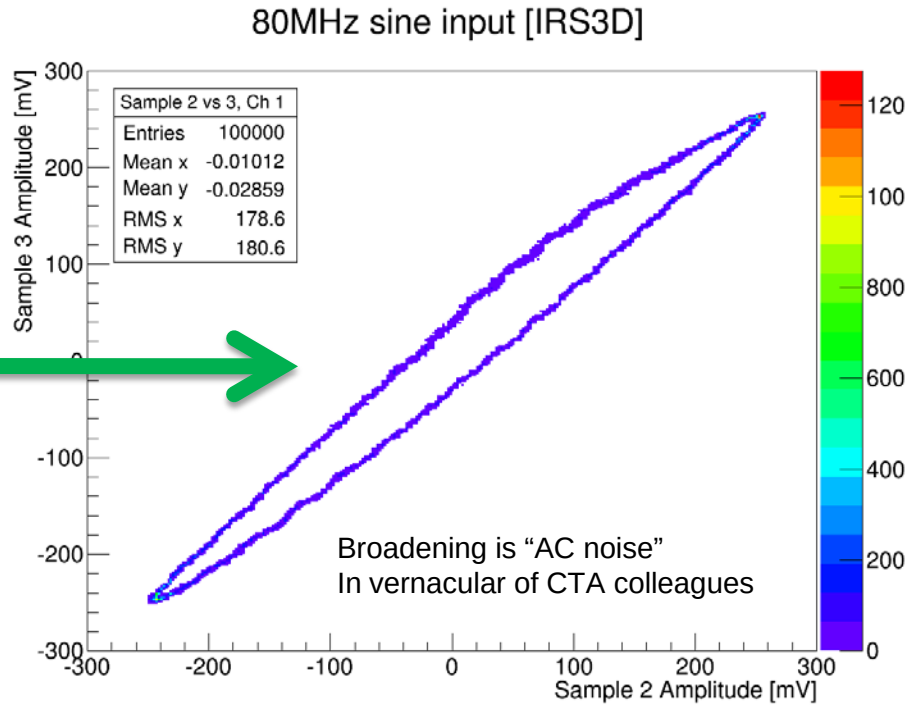
- 16x doesn’t improve further, as already at the signal-to-noise limit

Improved Wilkinson “cross-feed”



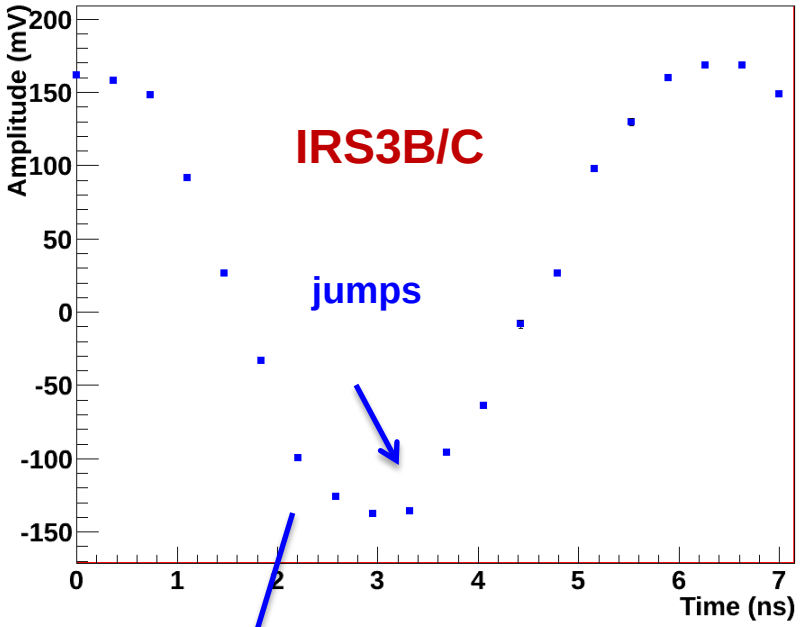


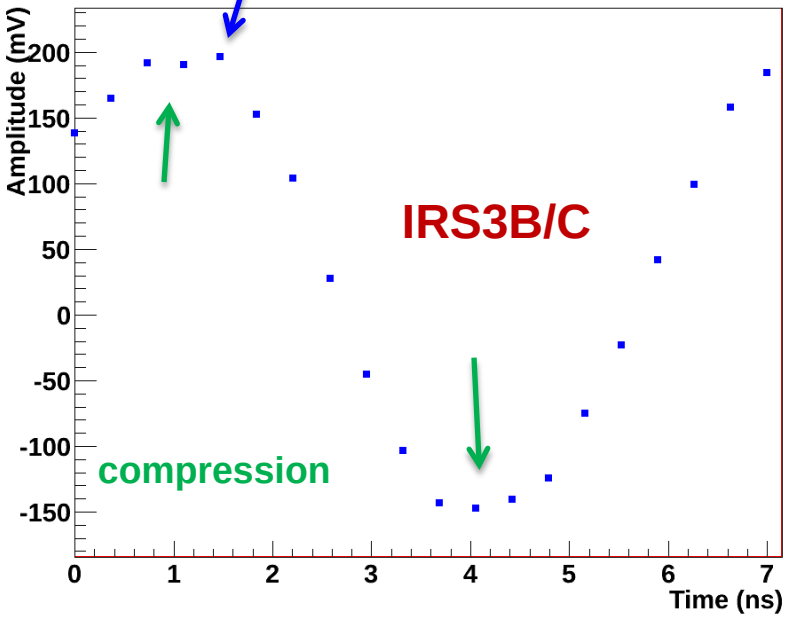
- Broadening at the extrema
- Breakdown of simple ellipses expect otherwise
- Kinks/inflections hard to manufacture without some type of digital interference



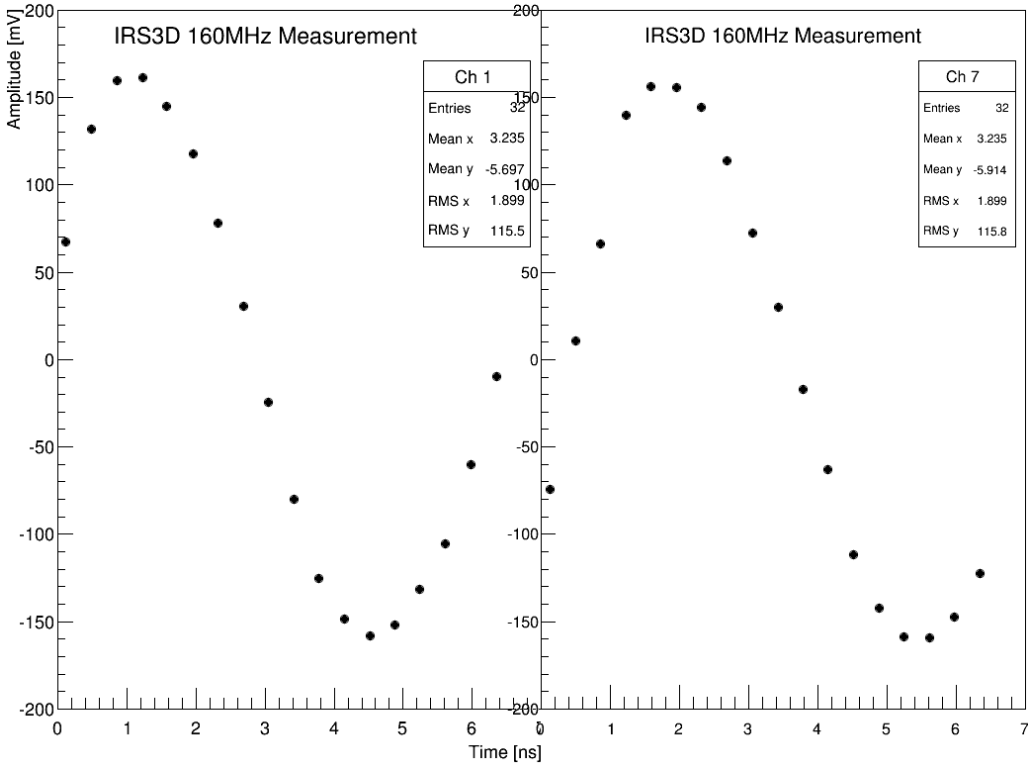
Much improved – some additional improvement expected with linearity correction

Result: visually nicer waveforms



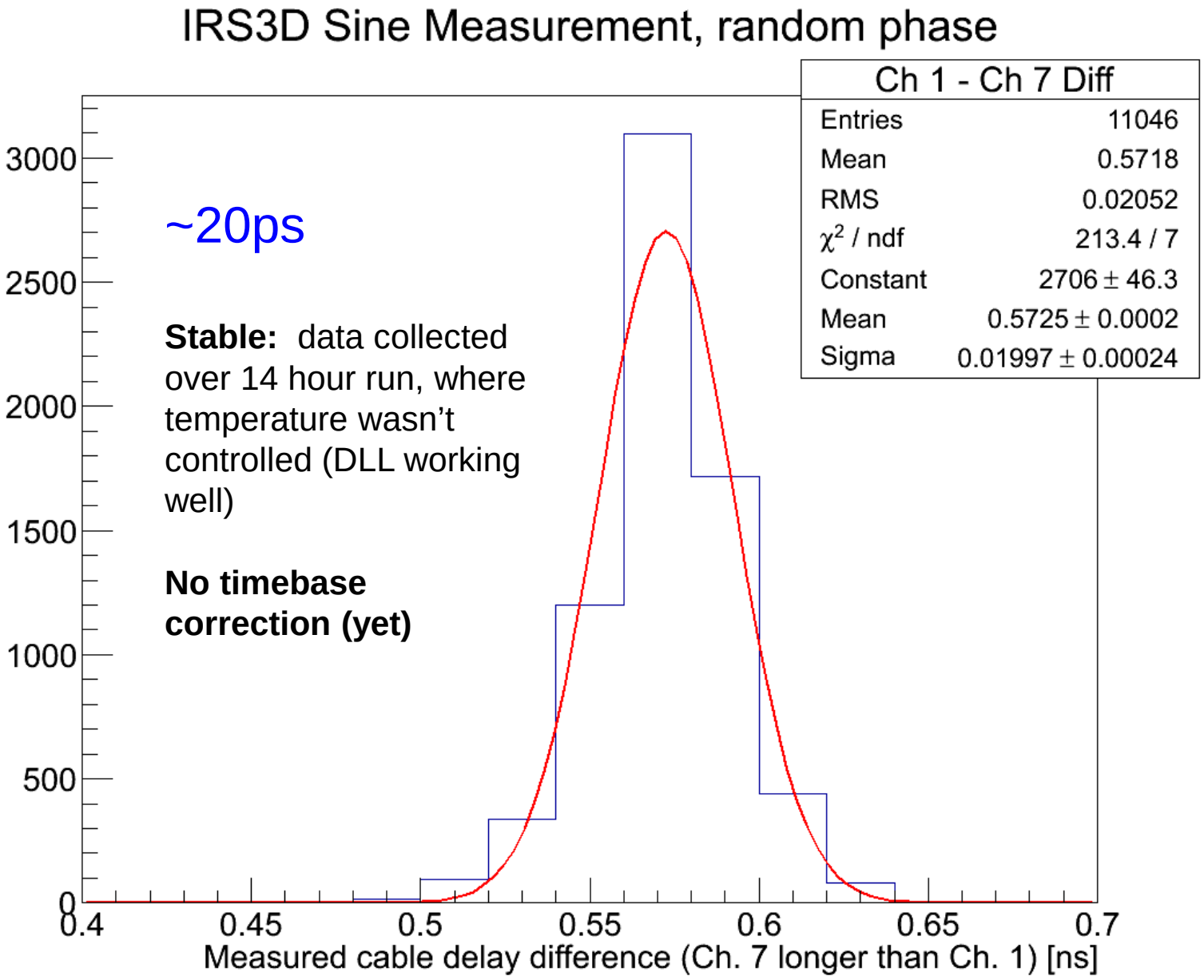


Difference most evident at the extrema of the waveforms



IRS3D

Of course, what we really care about …



CAJIPCI upgrade

- If start with clean clock, don't need/want the complexity of clock jitter cleaner
- Use something more like successful FTSW
- Compare/modify programming methodology

20110805 version

Timing signals over CAT7 cables

7 ports, O1 to O7

ACK →	ACK: 254 Mbps serialized, unused
TRG ←	TRG: 254 Mbps serialized
RSV ←	RSV: pulled down to GND
CLK ←	CLK: 127 Mhz

JTAG signals over CAT7 cables

4 ports, O9 to O12

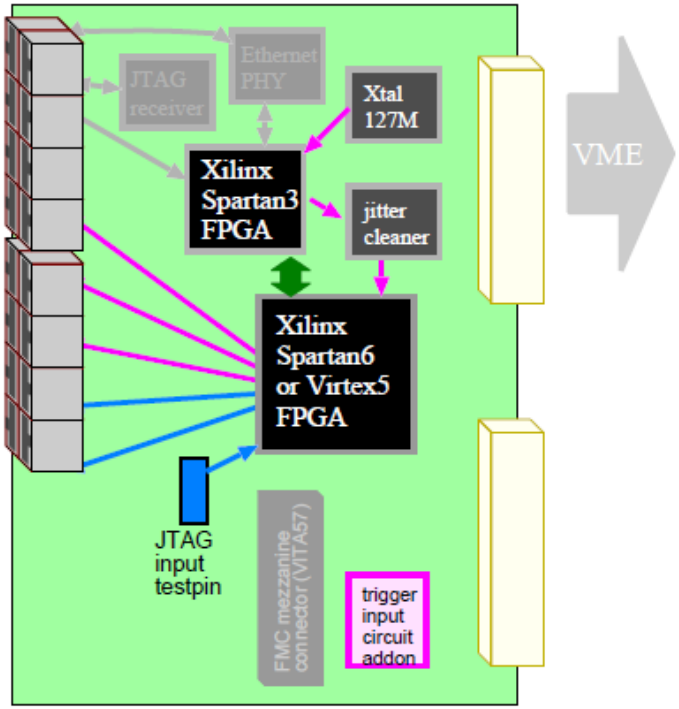
TCK ←
TMS ←
TDI ←
TDO →

Monitoring signals over a CAT7 cable

AUX port

trgin ←	copy of trigger input
trg21 ←	latched with 21MHz clock
trgpulse ←	trgin and (not trg21)
clk21 ←	21MHz clock

JTAG	LAN
IN	AUX
O1	O2
O3	O4
O5	O6
O7	O8
O9	O10
O11	O12



FTSW clock, trigger, programming

Micro-TCA

- Based upon advanced TeleCom standard, but a light version, preferred by particle physics community
- Designed for intensive signal processing/handling
- Engineered from the start for extremely high reliability and performance

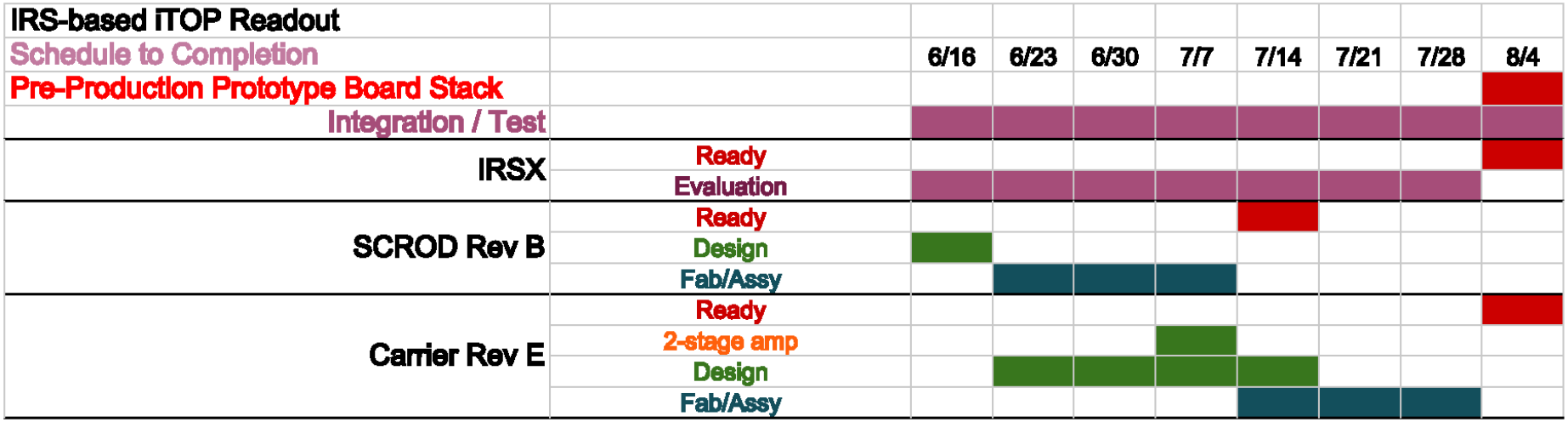
2U height, 19” rack-mount ($3,750)

mTC Hub Controller ($5,341)

CPU (Intex Xeon E3) ($3,360)

mTC Upgrade Schedule/Cost

- Production lot of packaged IRS3D should be available by ~mid-Sept (wafers back end of August)
- Example schedule showing Rev E Carrier Dev time



Costs:

- Carrier Fab: can get hard numbers from previous fab/assy runs
- Micro-TCA parts listed (still need to pick a RTM to handle the required # of fibers, but that is passive/inexpensive)
- CAJIPCI replacement few k$ at most. Probably take existing design, throw out clock jitter cleaners, and put down good clock source and low-jitter fanouts

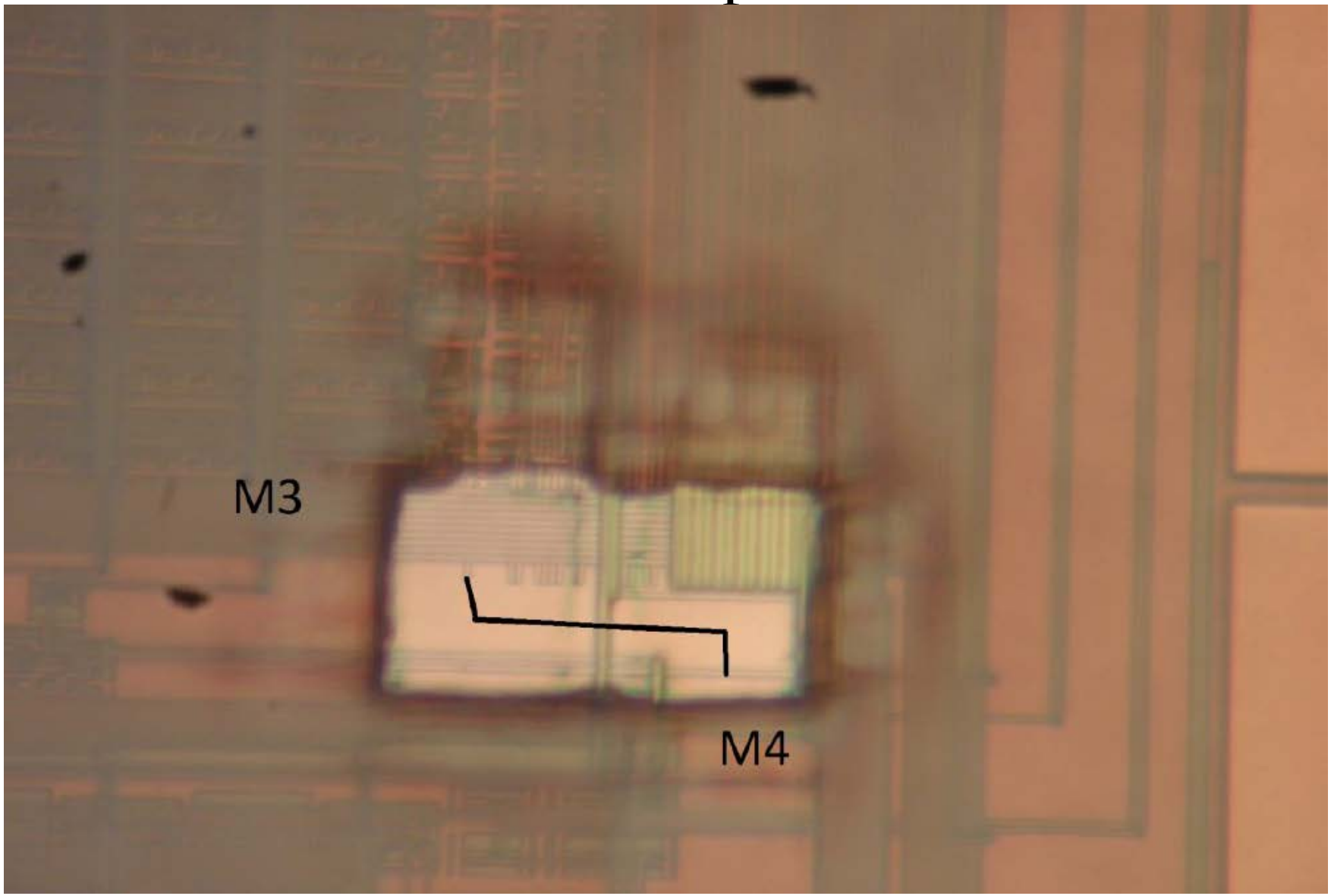
Summary

- mTC Development Status
  - **Stuck somewhere between Phase 1 and Phase 2**
  - **Hardware upgrades will short-circuit some of the development/education time required**
  - **Getting to Phase 3 will expedite getting the physics**

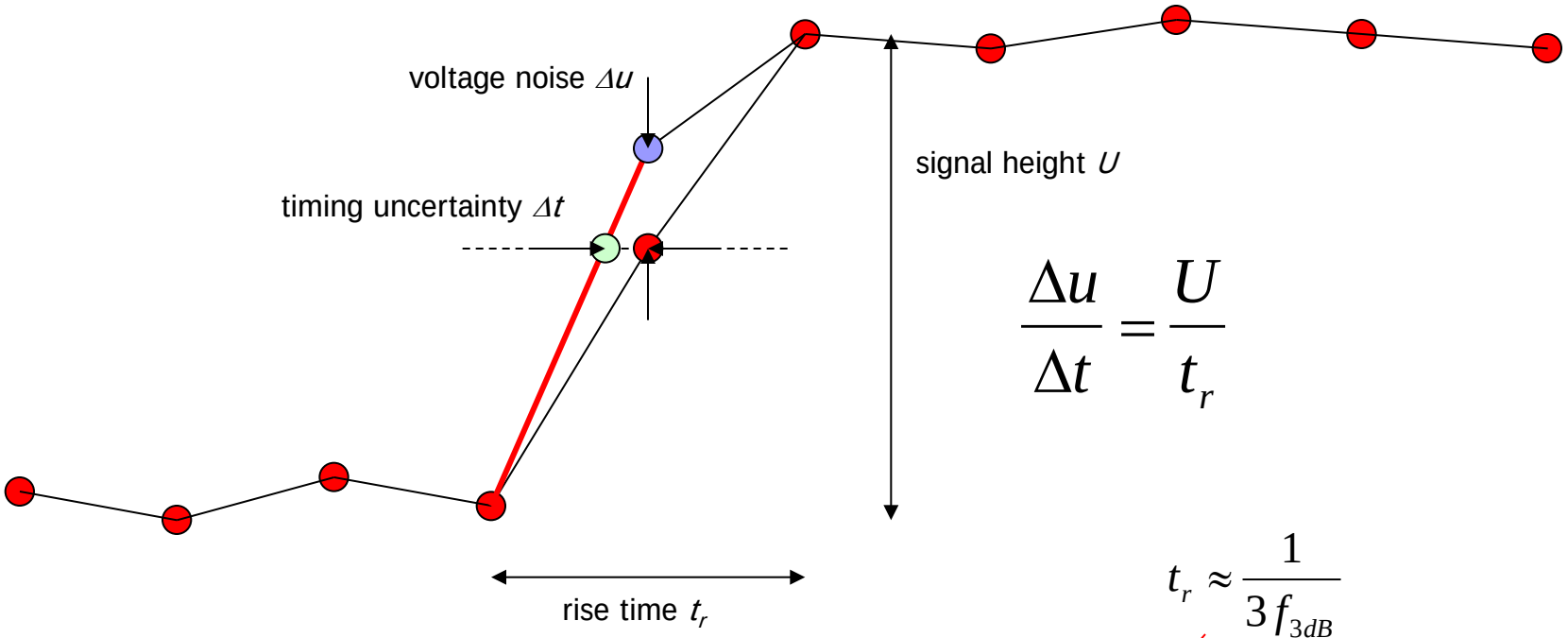
- **Specific Recommendations:**
  - **Upgrade Carrier cards to IRS3D and improved amplifier**
  - **Replace CAJIPCI with simplified module**
  - **Migrate from cPCI home-brew to enterprise micro-TCA DAQ platform**

- **Schedule and costs look reasonable. Leverage the knowledge and experience gained.**

Backup



Calibration and Sources of Timing Error



$$\frac{\Delta u}{\Delta t} = \frac{U}{t_r}$$

$$t_r \approx \frac{1}{3 f_{3dB}}$$

$$\Delta t = \frac{\Delta u}{U} \cdot t_r = \frac{\Delta u}{U\sqrt{n}} \cdot t_r = \frac{\Delta u}{U} \cdot \frac{t_r}{\sqrt{t_r \cdot f_s}} = \frac{\Delta u}{U} \cdot \frac{\sqrt{t_r}}{\sqrt{f_s}} = \frac{\Delta u}{U} \cdot \frac{1}{\sqrt{3 f_s \cdot f_{3dB}}}$$

*Diagram, formulas from Stefan Ritt

Calibration and Sources of Timing Error

Contributions to timing resolution:

- Voltage uncertainties
- Timing uncertainties

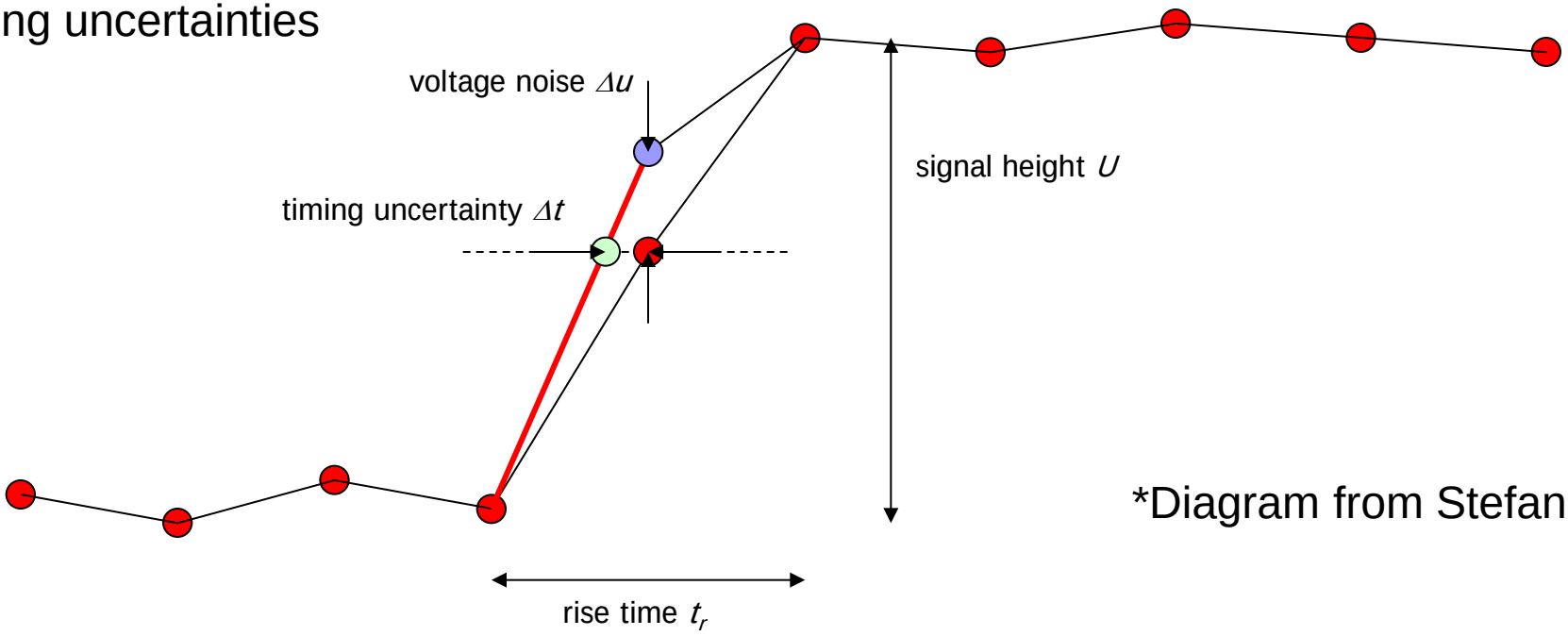


*Diagram from Stefan Ritt

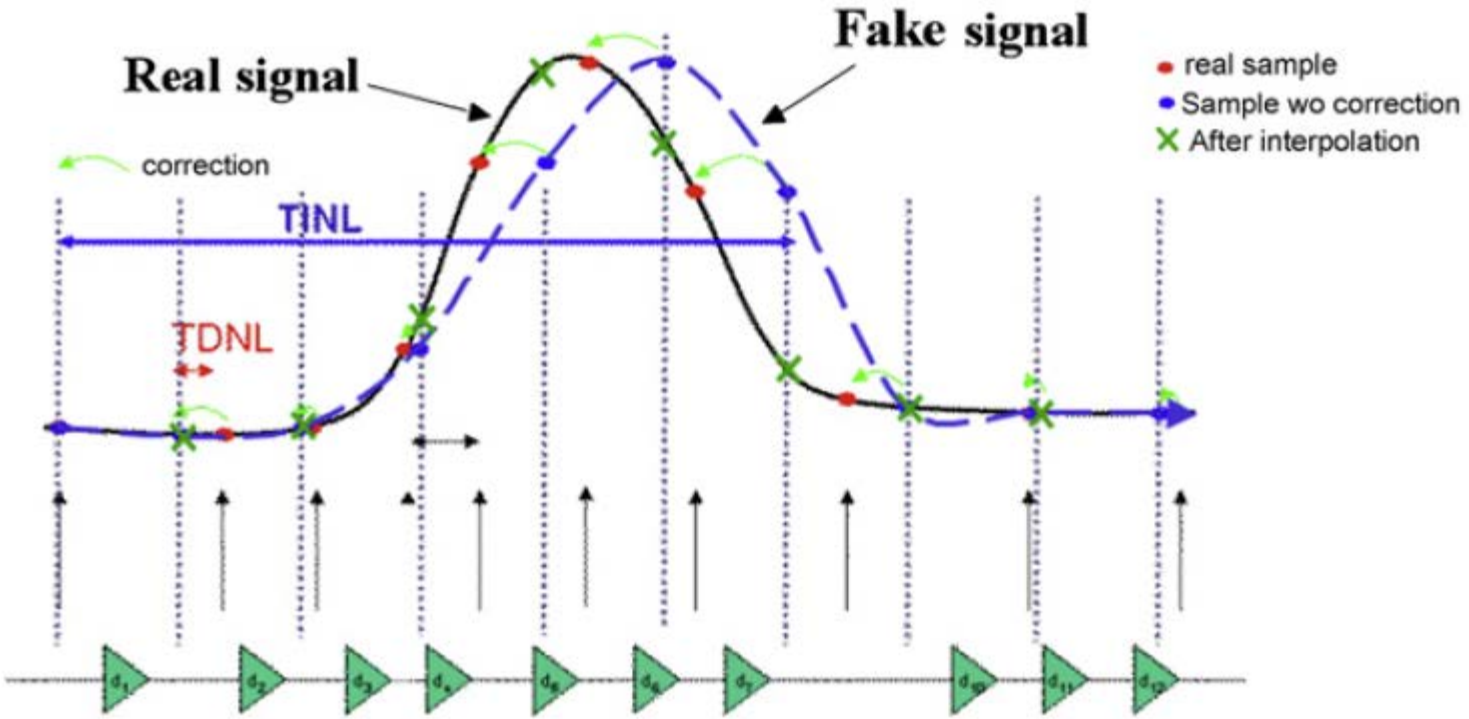
Of these contributions:

- Random – irreducible (without hardware redesign)
- Deterministic – **in principle** can be calibrated away.

Let's talk about where the deterministic pieces come from and what is or is not being done about them right now, and what might be desirable or necessary in the future.

Timing Uncertainties and Timing Calibration

- Time interval between delay line stages has intrinsic variation.
- Not accounting for this properly causes significant



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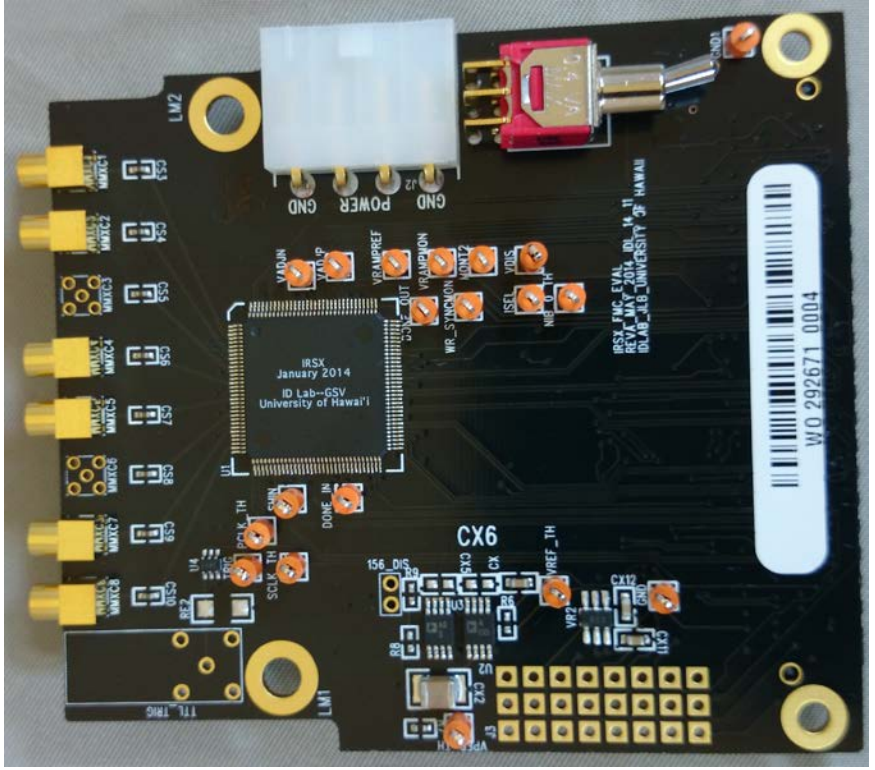
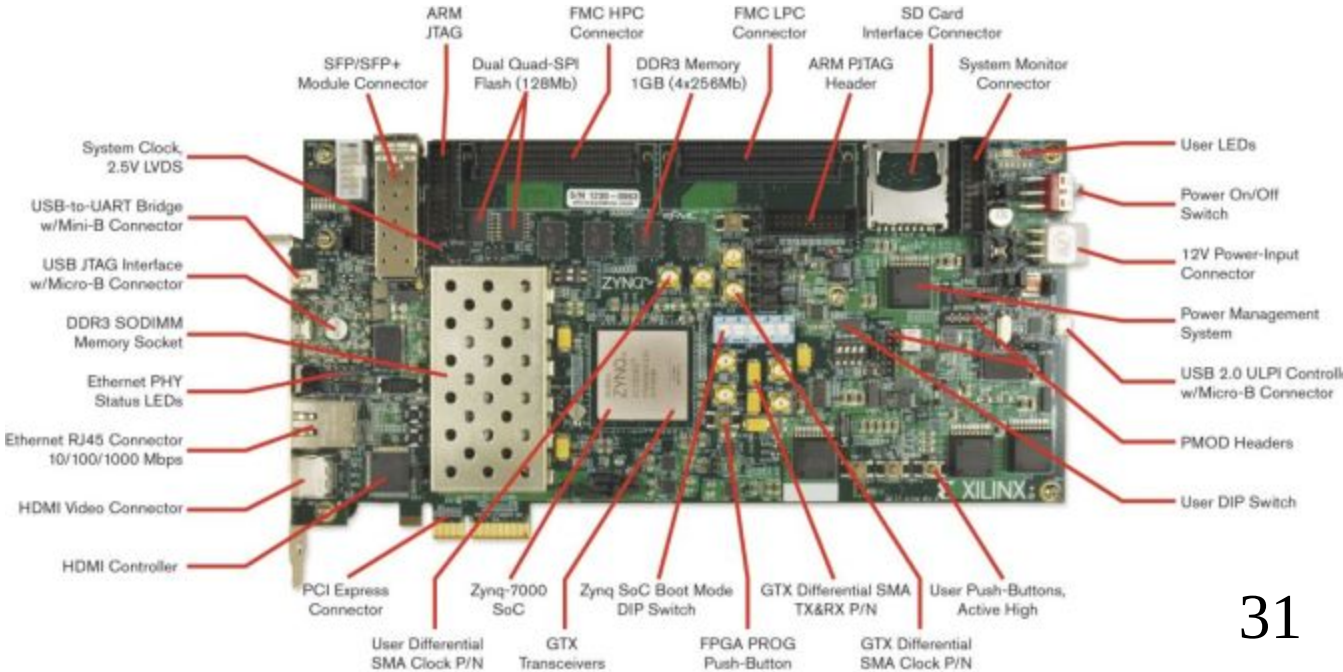
IRSX Eval board

- FMC test card format for Xilinx Zynq-7 (Zynq-706) Evaluation board





Cross-checking IRSX Improvements:
(features largely vetted on other ASICs, of similar/identical DNA)

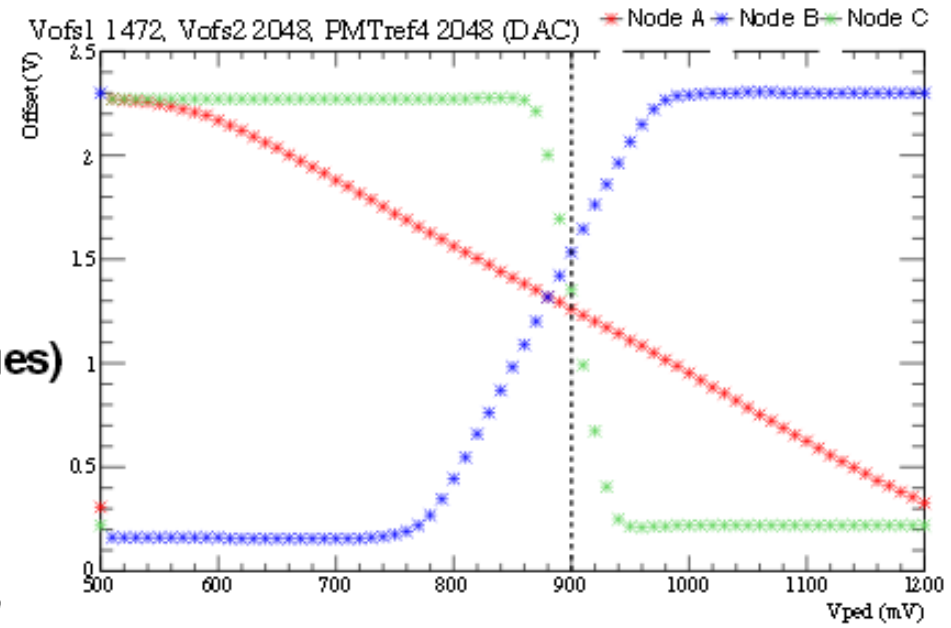
- Triggering
  - IRS3C has no gain in trigger path
  - Insufficient overdrive for small/fast+narrow MCP signals
  - IRSX adds selectable trigger gain path
- Improved dynamic range/linearity
  - Added 2nd stage, with tuning, to Wilkinson comparators, to extend dynamic range and reduce non-linearity
  - Modified Wilkinson registers for much lower power and critically reduced cross-talk

TARGET7 results courtesy Hiro Tajima (Nagoya) on triggering and Justin Vandenbroucke (Wisconsin) on improved dynamic range/linearity. Comparison with LAB4C ASIC provided by Hawaii ANITA3 collaborators

Trigger Gain (x1 [IRS3C], x4, x16)

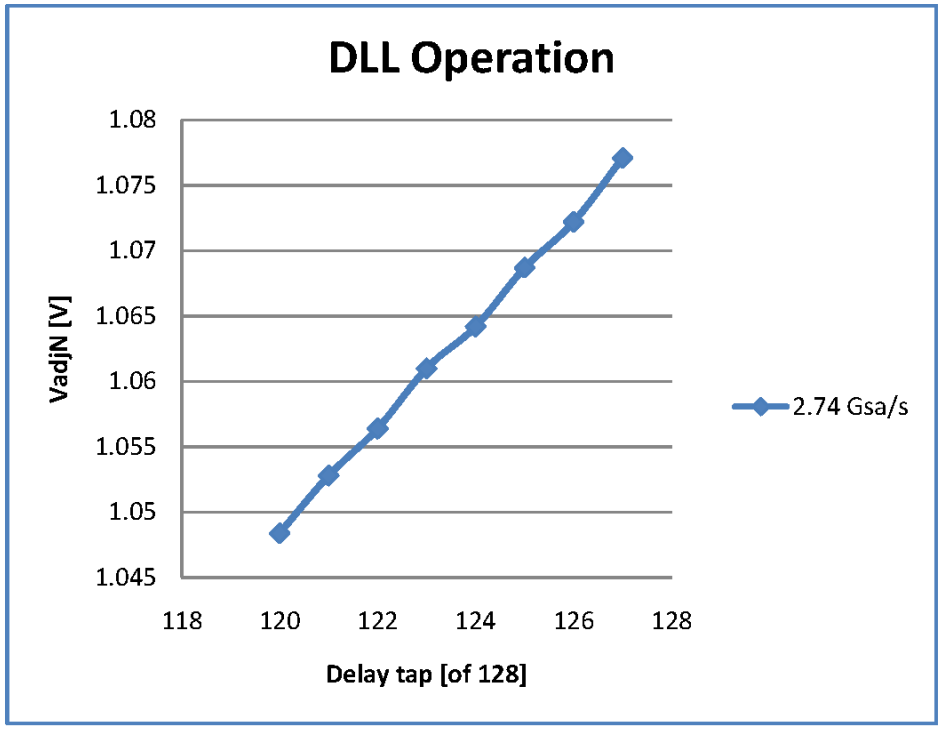
- Transfer slopes match simulated (designed) values well

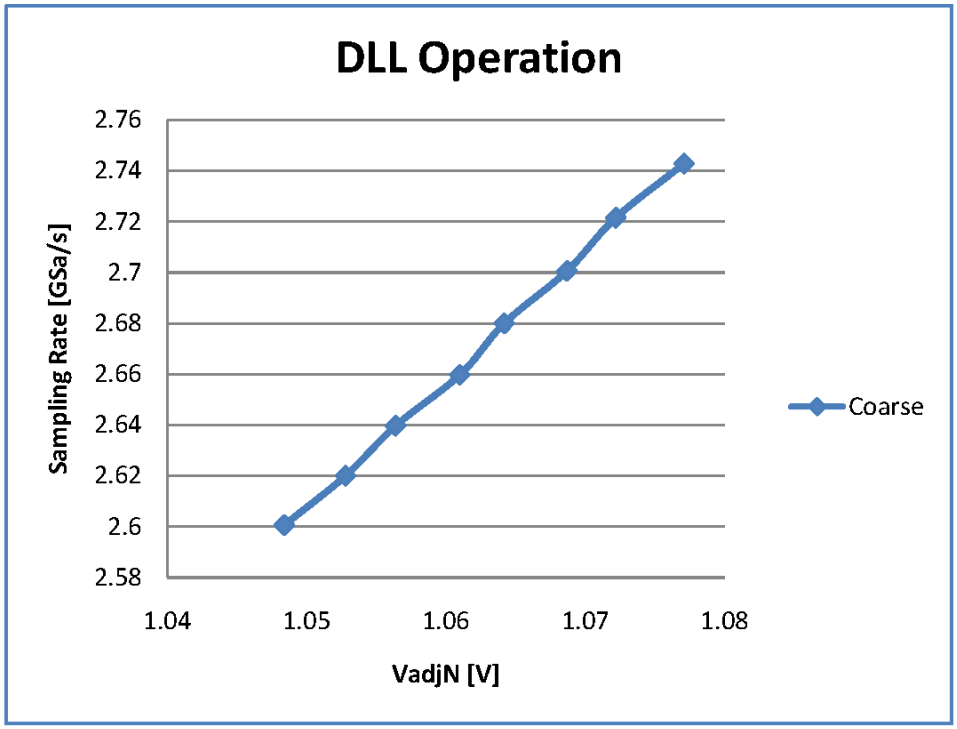
Settings (DAC values)
Vosf1: 1472
Vosf2: 2048
PMTref4: 2048
TRGGbias: 985
TRGsumbias: 1147



- Comparator threshold "overdrive" improved by factors of 3.2, 11.1
  Full efficiency S-curves are reported in next slide (these important internal probes represent something can't be done directly inside the IRSX [doesn't have these test structures]).

Timebase servo-locking (DLL)





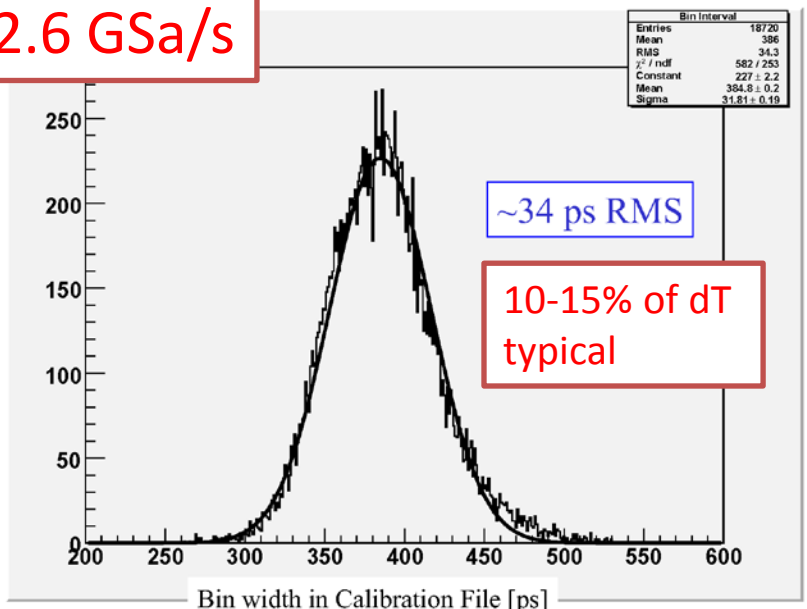
- Excellent stability visually on monTiming output
- VtrimT to fine-tune between coarse tap settings

(scatter from linear is dT values)

(indirect “RCO” feedback mechanism injects asynchronous noise into timebase generator, degrading timing performance – so this is a significant improvement)

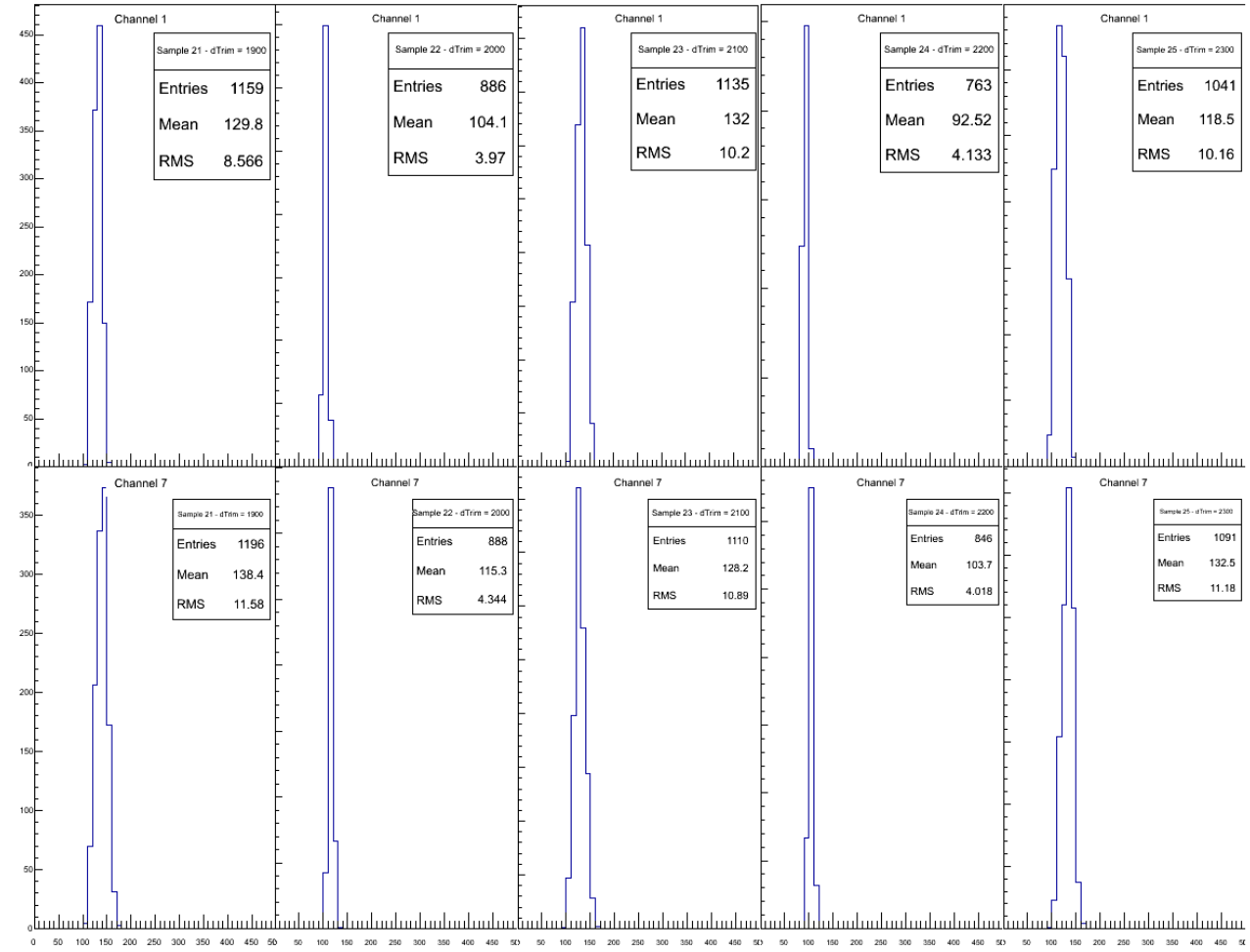
Time base non-uniformity…

2.6 GSa/s

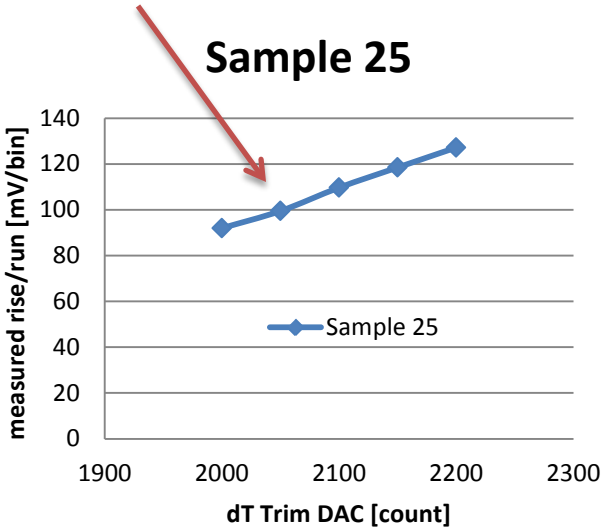


If can correct, reduces processing time dramatically, as this is the most computationally-intensive aspect of "fast feature extraction"

dT Correction Demo



Target operating point (as an example)

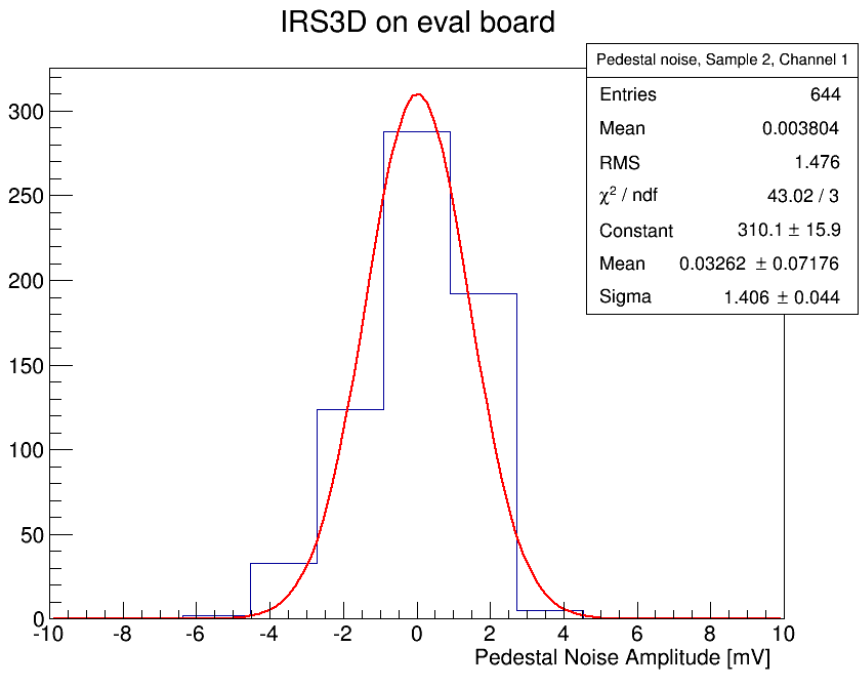


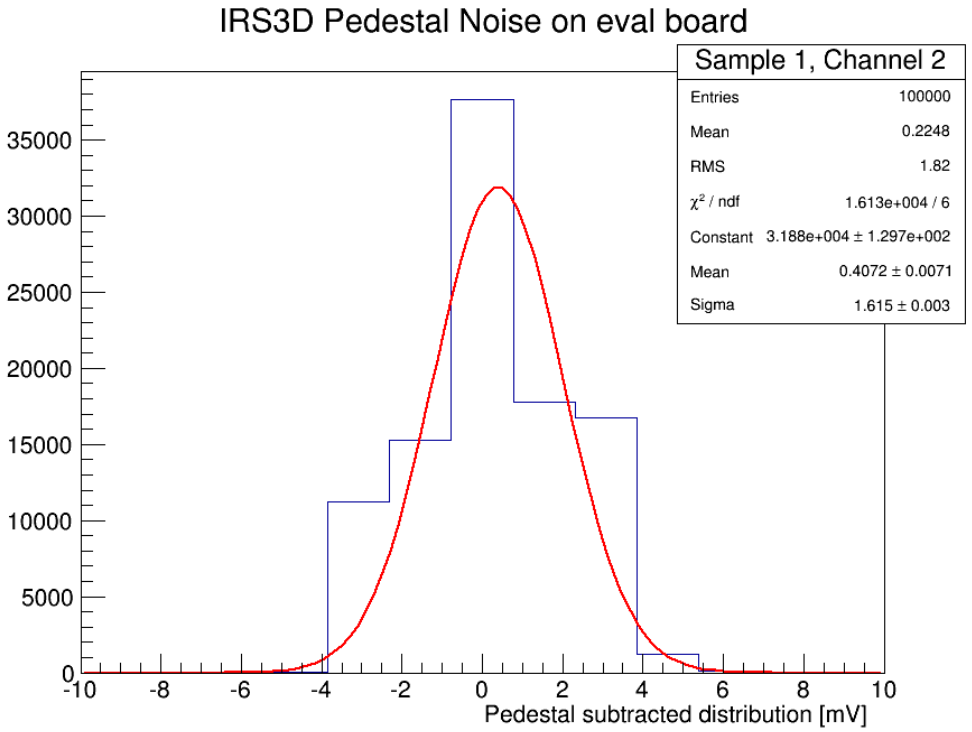
Only tricky part is that the DLL compensates to keep overall length, so need iterative solver for all samples simultaneously

Samples follow each other across channels

Calibrate once and subsequent corrections made in hardware

Observed IRSX (IRS3D) noise

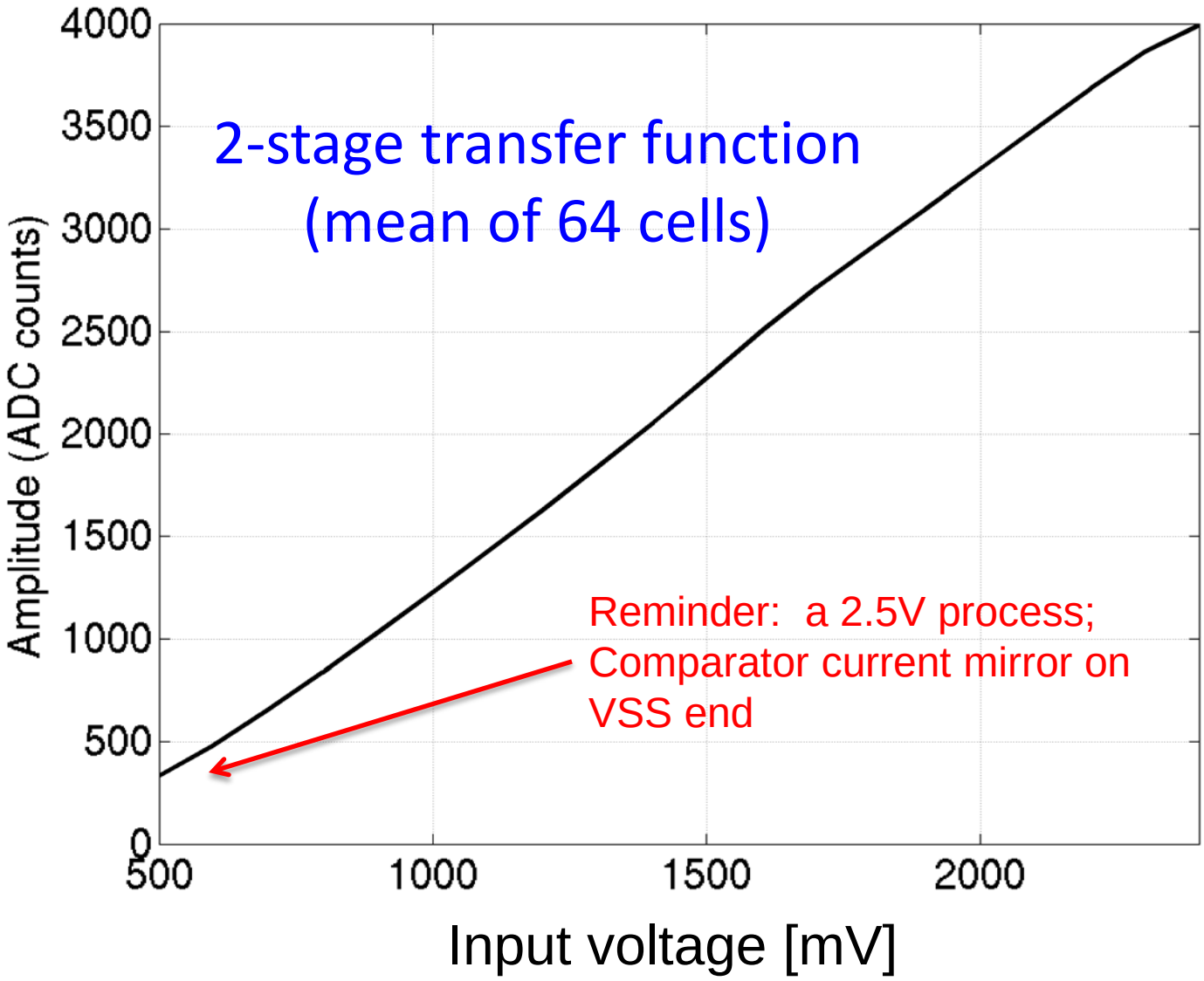




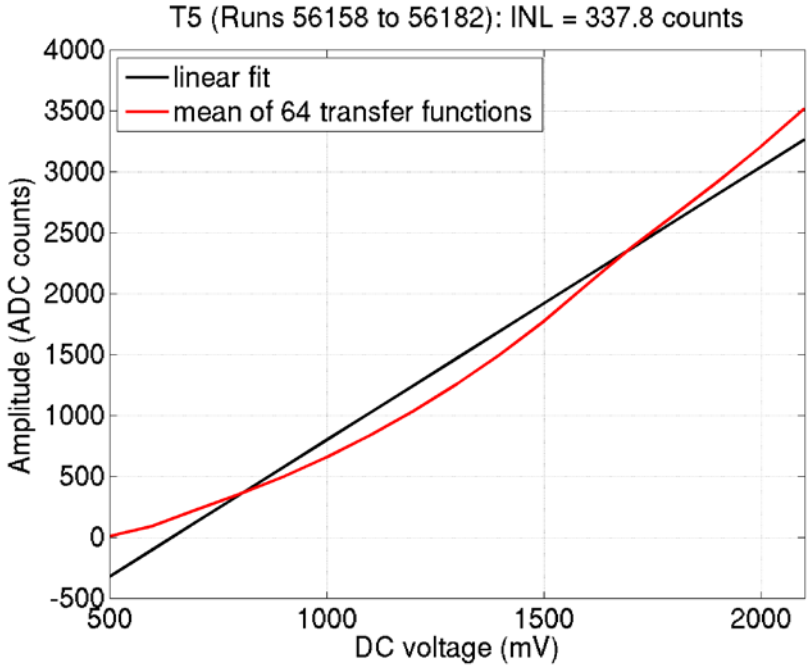
Non-gaussian distributions expected for small noise amplitude due to non-linearity in Gray-code least count

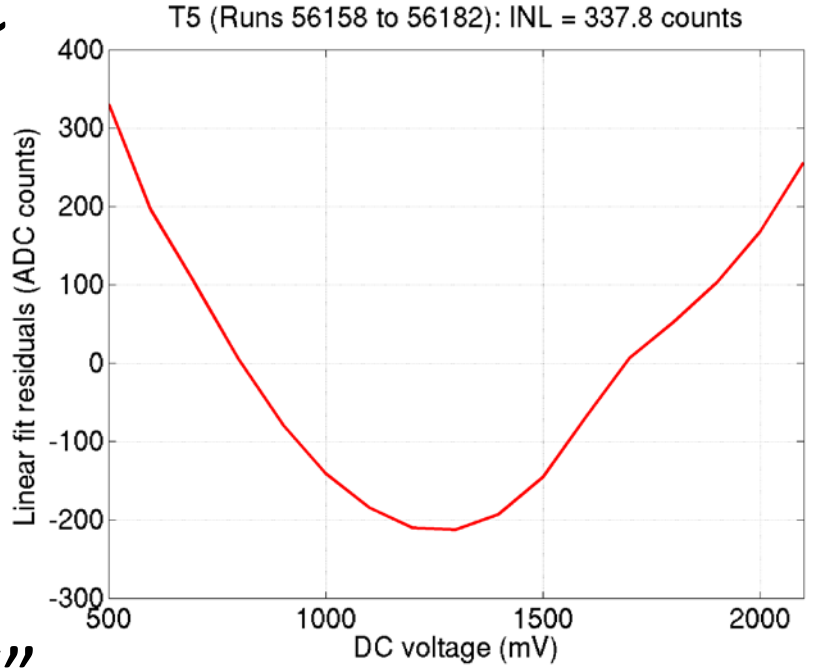
Take away message: noise is comparable, or better than IRS3B/C, and acquired while sampling continues to run

Improved Linearity [TARGET7/X]

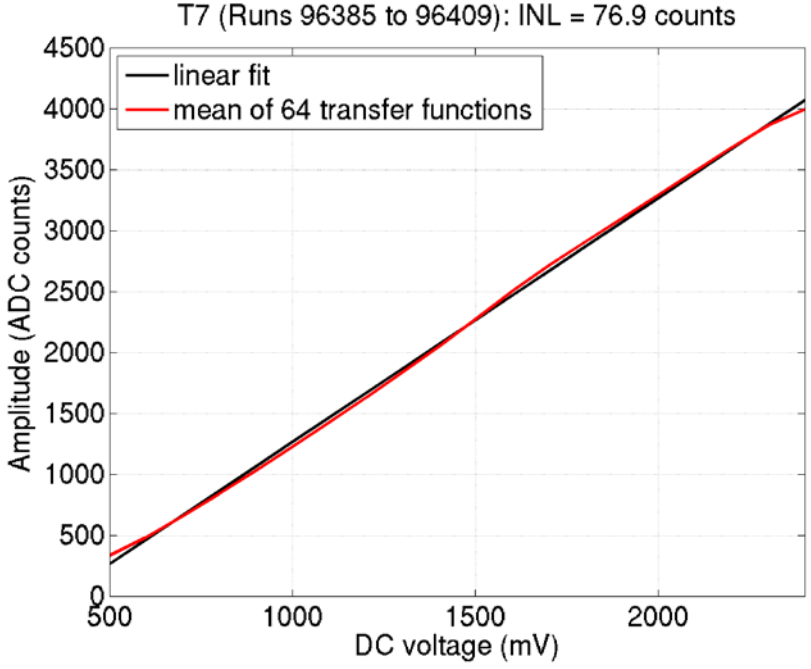


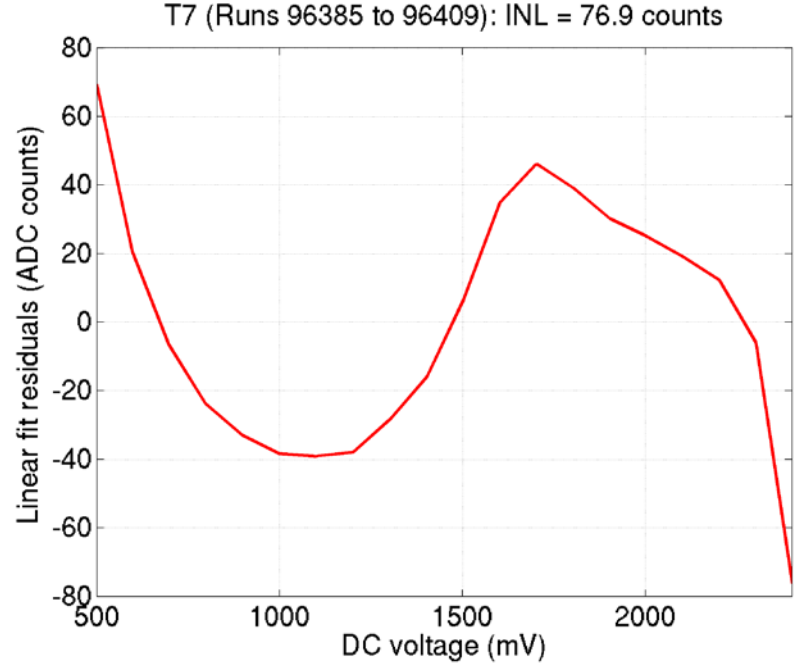
"IRS3C"


T5 (Runs 56158 to 56182): INL = 337.8 counts
linear fit
mean of 64 transfer functions
Amplitude (ADC counts)
DC voltage (mV)


T5 (Runs 56158 to 56182): INL = 337.8 counts
Linear fit residuals (ADC counts)
DC voltage (mV)

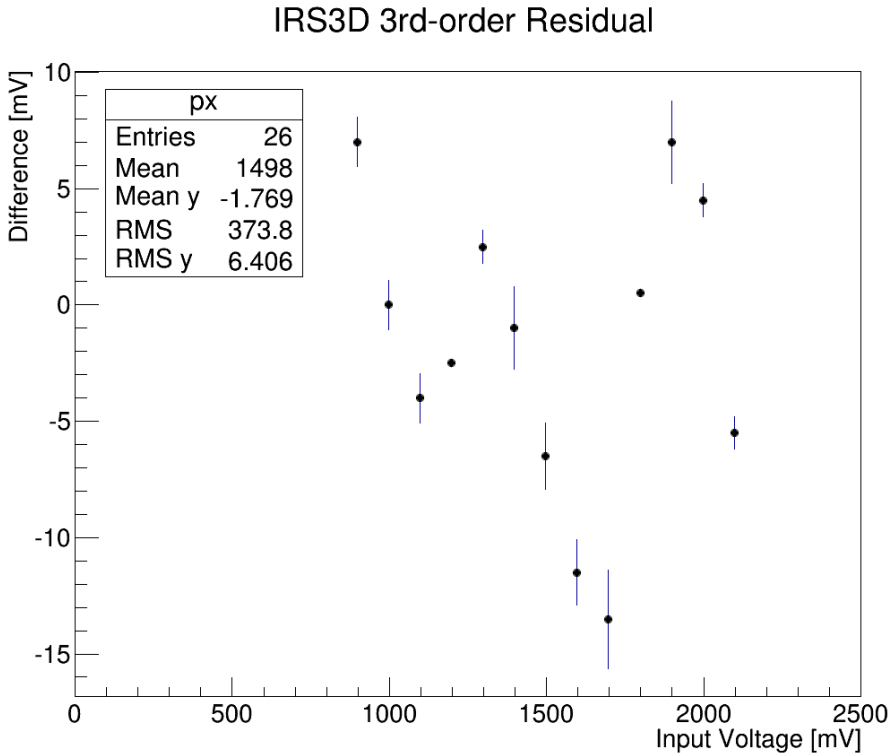
"IRSX"

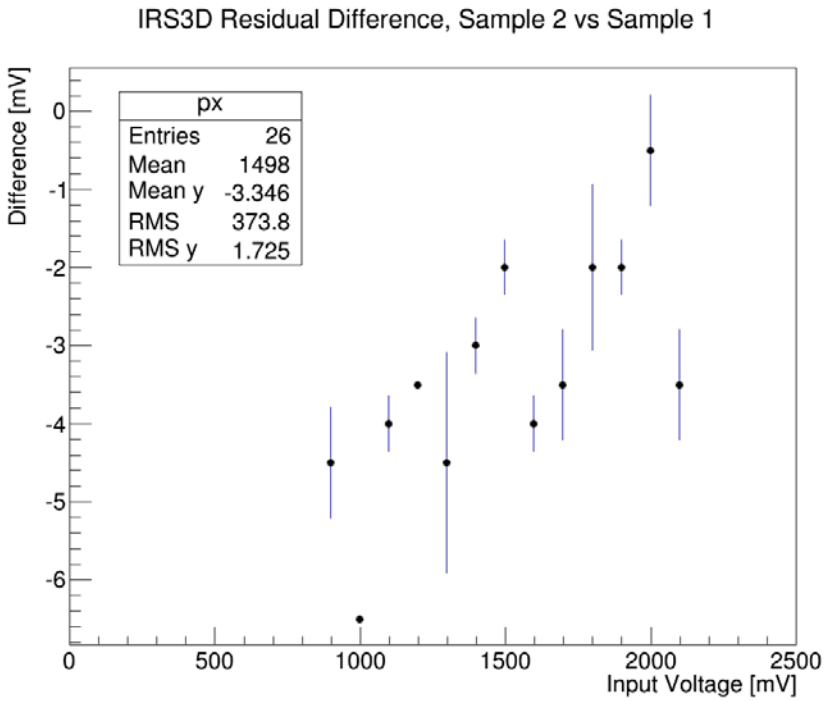

T7 (Runs 96385 to 96409): INL = 76.9 counts
linear fit
mean of 64 transfer functions
Amplitude (ADC counts)
DC voltage (mV)


T7 (Runs 96385 to 96409): INL = 76.9 counts
Linear fit residuals (ADC counts)
DC voltage (mV)

Improved Residuals, repeatability

Note: IRS3D -- no comparator bias tuning yet done

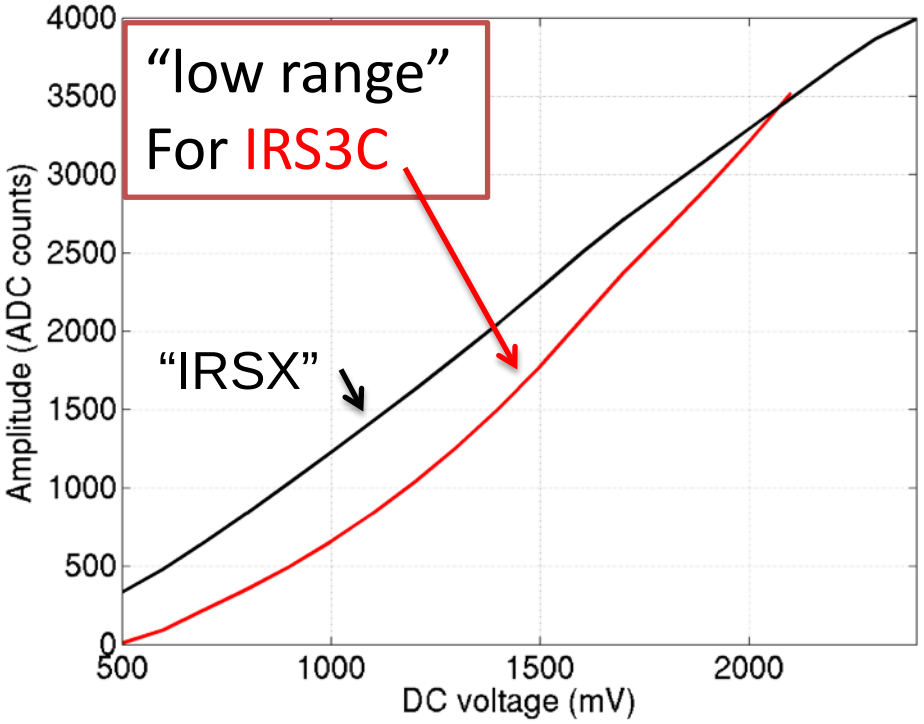


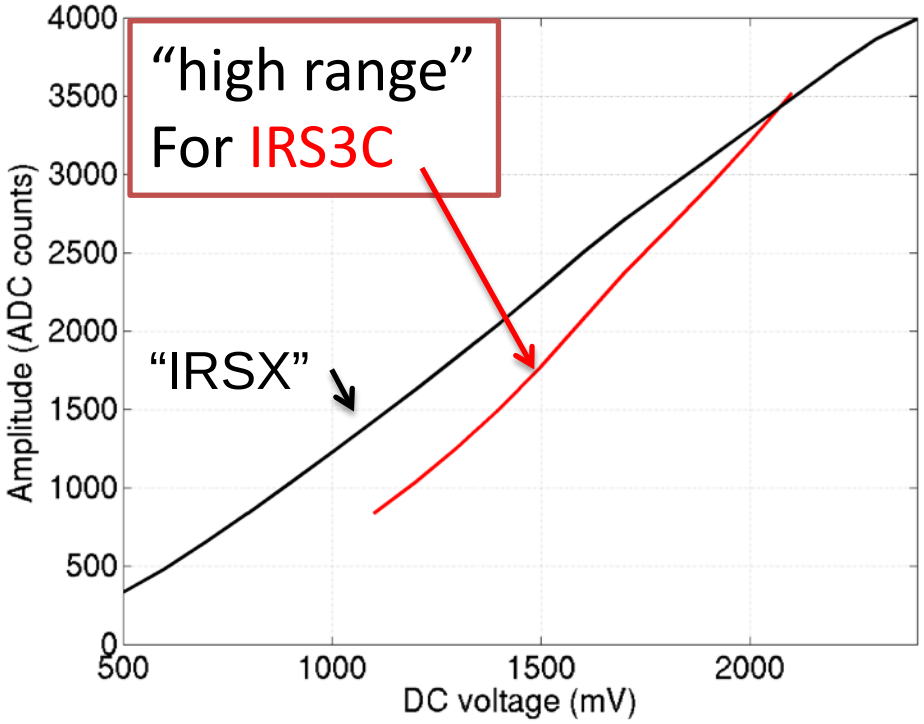


~1% Integral deviation from 3rd-order over key sensitivity range

Shape repeatable sample-sample (common lookup table, with only pedestal offset)

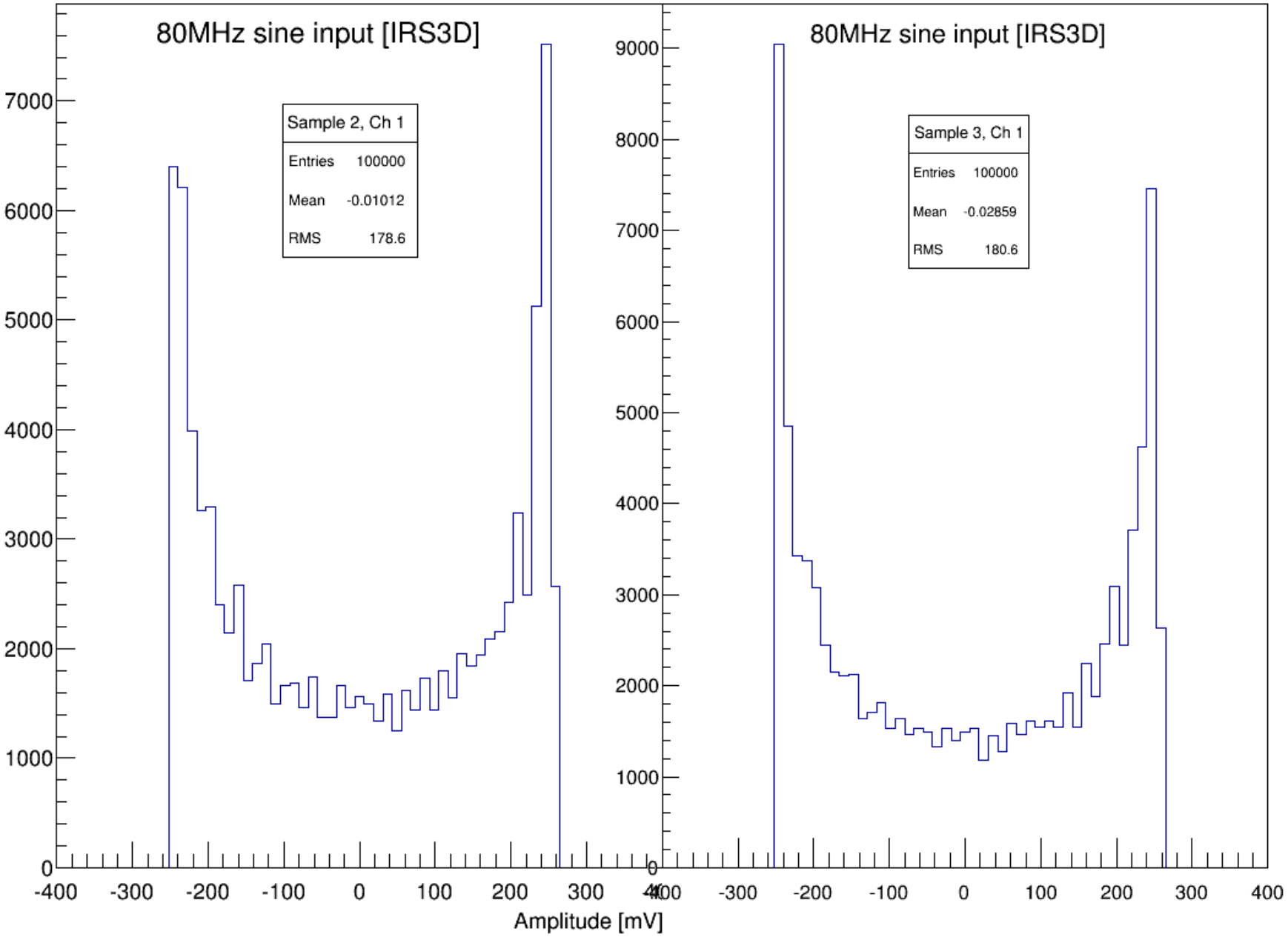
Improved dynamic range





- Could tune somewhat for desired range of operation in IRS3C, but still could not get much above about 2V (and large scatter in where comparators would stop working)

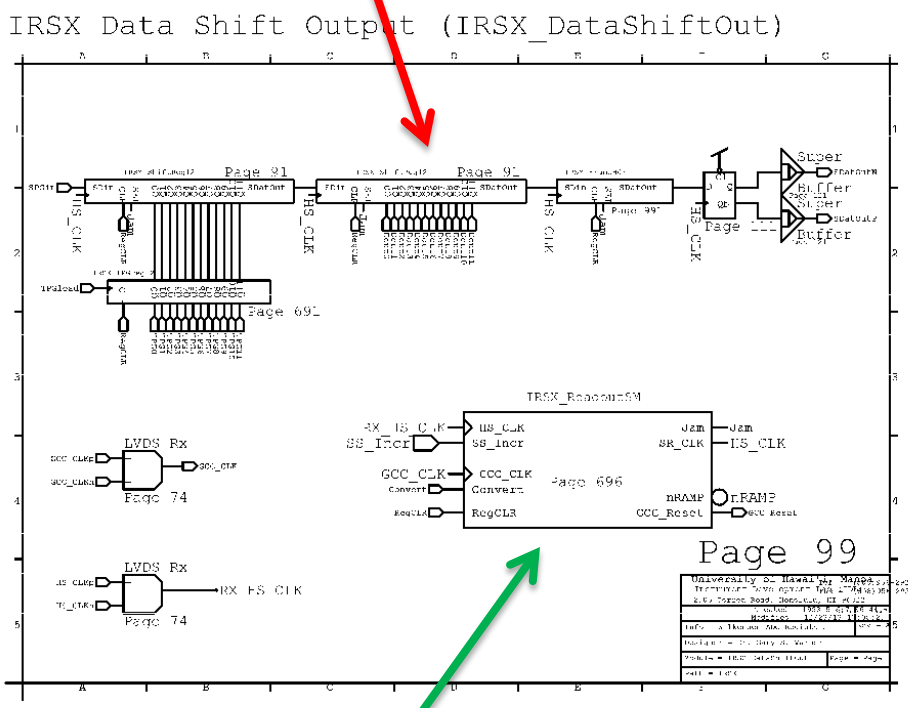
IRSX (IRS3D) 80 MHz sine response (2 adjacent samples)

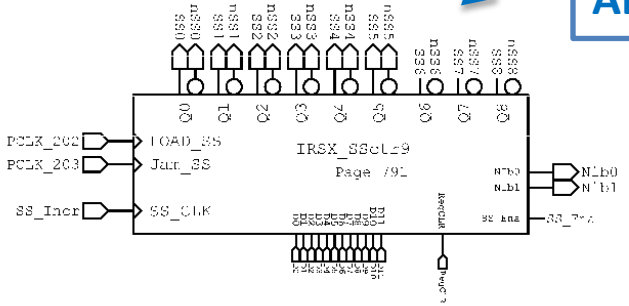


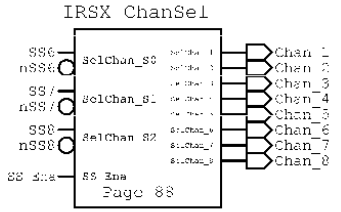
2x Fast LVDS Serial: Write Address, Readout

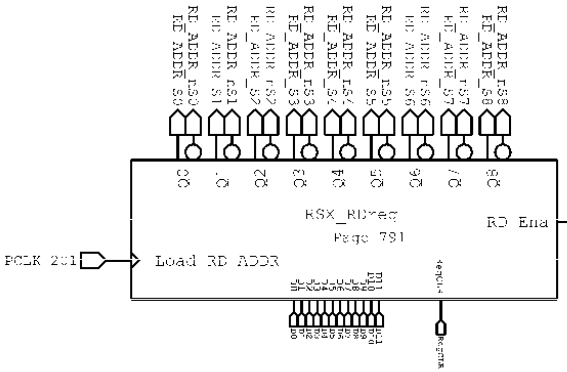
Primary Shift Register (increments on SR_CLK, loads on Jam)

Loadable, incrementable Sample+Channel ADDR









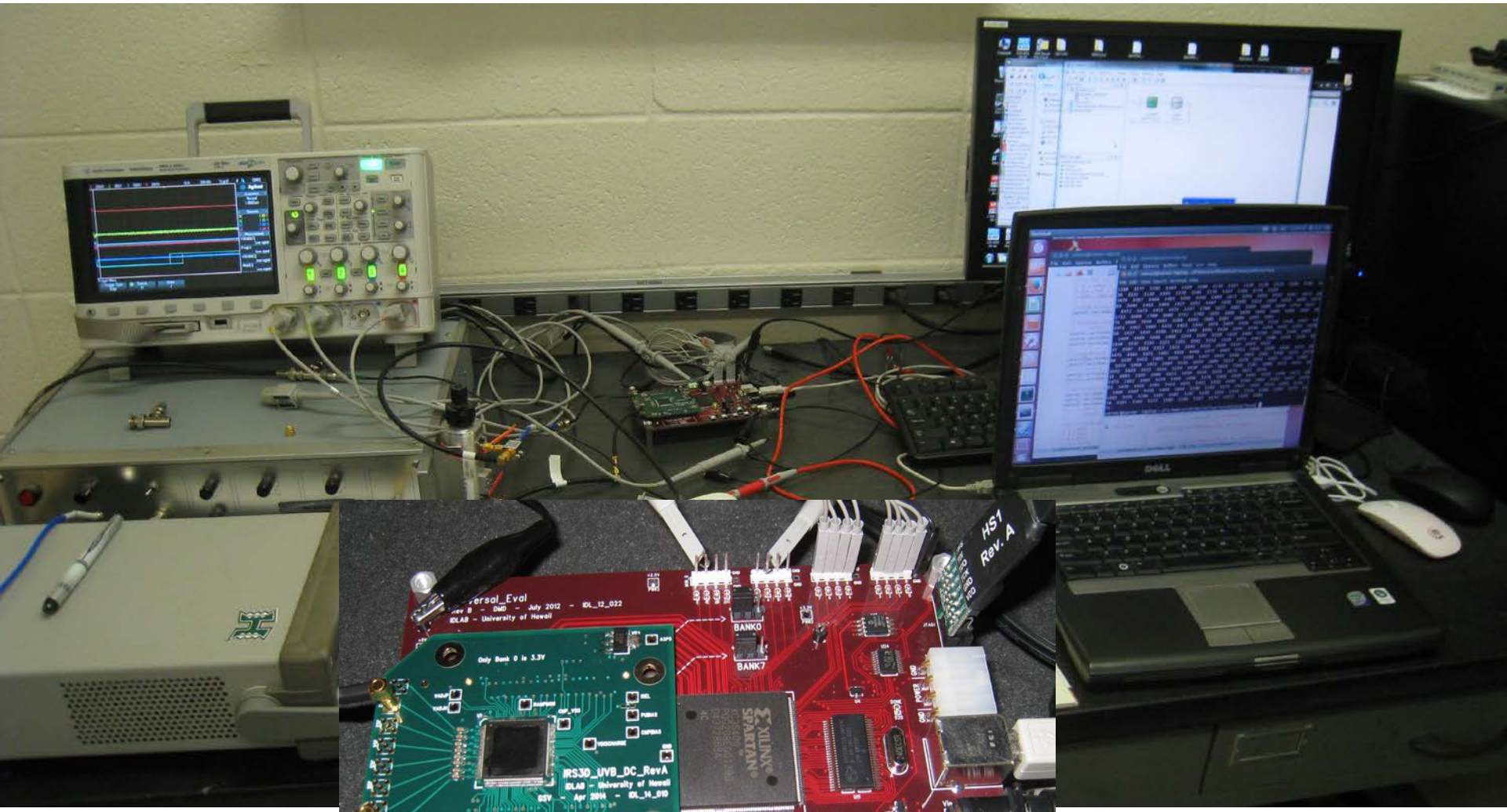
Simple Timing Generators

Write-only RD ADDR (+ RD_Ena bit)

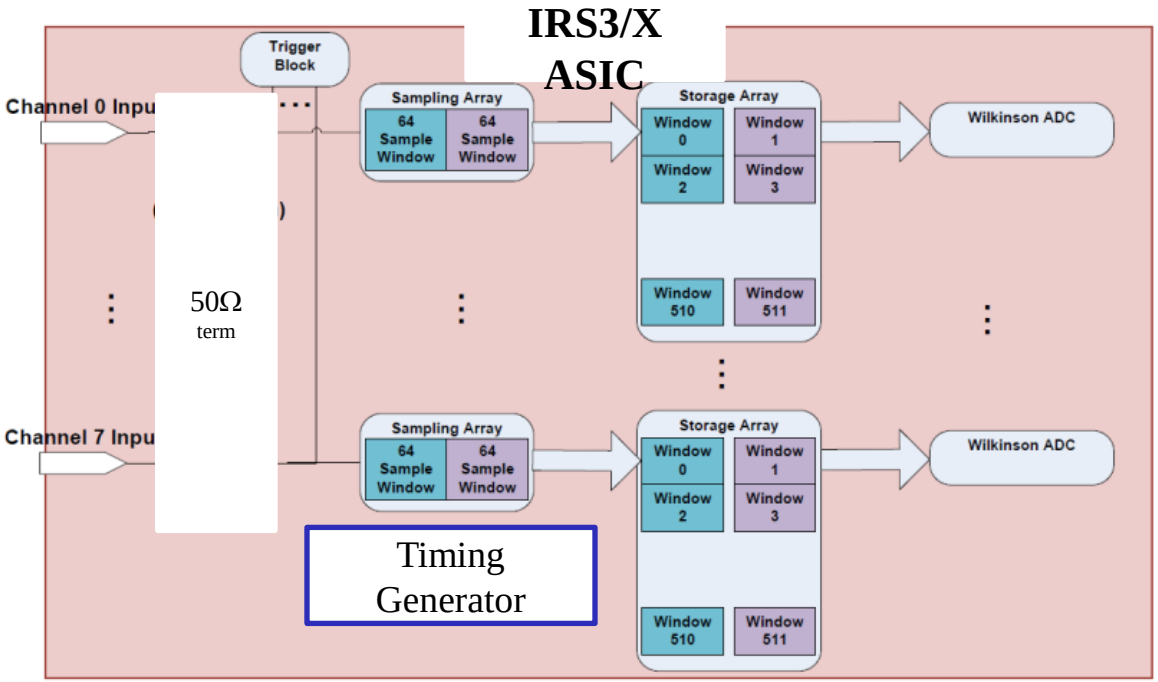
Simple Channel Address decoder (with SS_ena to switch sample to bus)

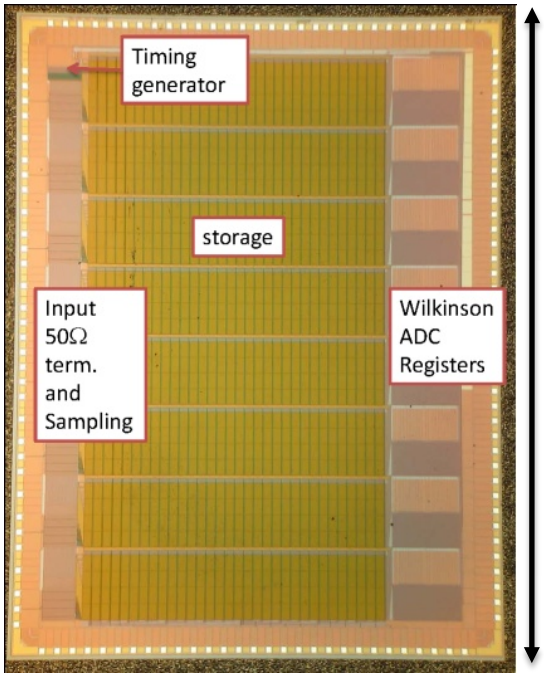
IRS3D Eval board

- Rather limited “universal eval” variant (Spartan-3 based);



Readout ASIC status: Design completed/reviewed, in fabrication

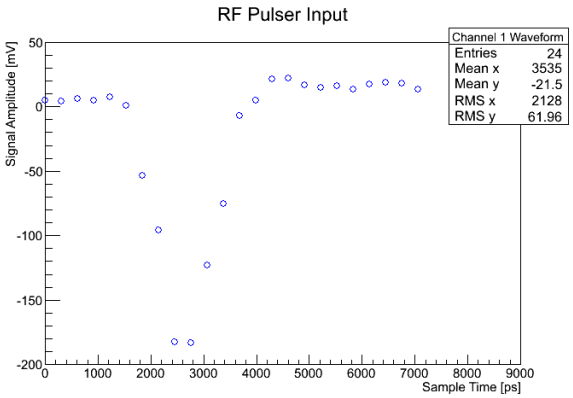




Die Photograph

- **8 channels per chip @ 2.7-4 GSa/s**
- **Samples stored, 12-bit digitized in groups of 64**
- **32k samples per channel (8us at 4GSa/s)**
- **IRS3C* (April 2013) usable for Belle II**
- **Increased performance margin ASICs in fab:**
  - **IRSX with high-speed serial interfaces**
  - **IRS3D with enhanced dynamic range, same I/O**

*** IRS3C = IRS3B with low power-on current, ext. dynamic range**



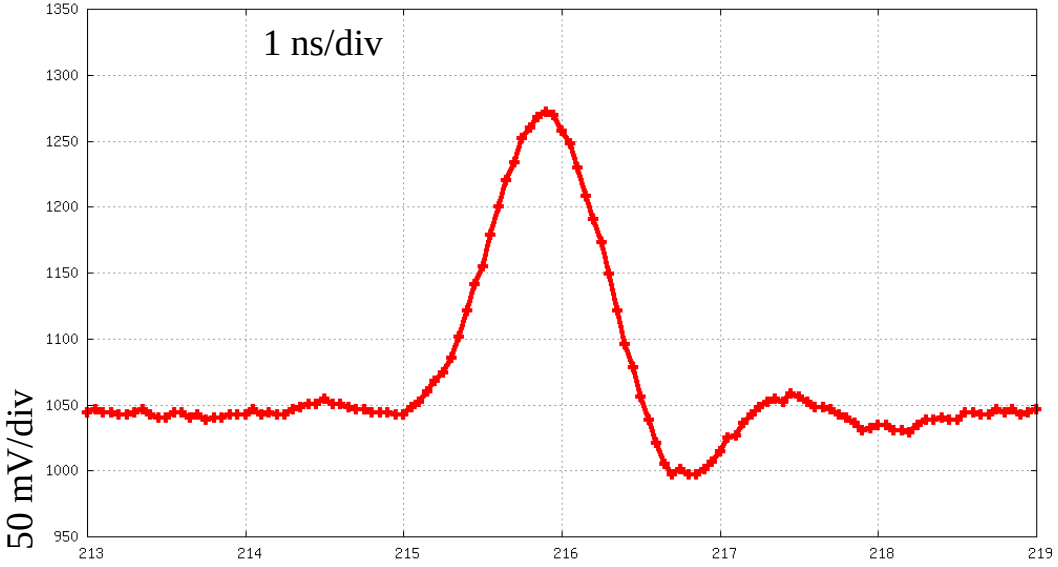
Pre-production Board Stack

- Amplifier and calibration signal path

Typical raw single-pe PMT pulse
HVB @ −3200 V
25 Ohm load
20 GS/s (RTO1044)
measured risetime: 140 ps

PMT gain ~ 5×10^5

Typ. amplified single-pe pulse
HVB @ −3200 V
Voltage on 10 pF load (IRSX eq.)
20 GS/s (RTO1044)
Measured risetime: 565 ps
[NOTE: different event & channel]



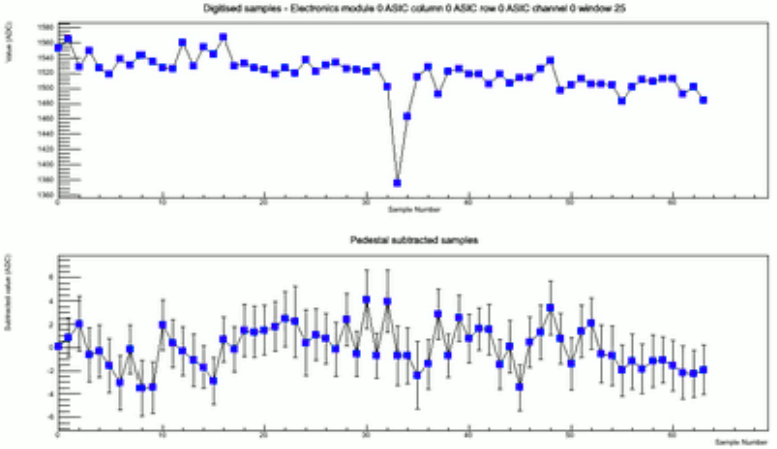
Calibration requirements

1. Subtract storage cell pedestal (avg. ~2000 ADC +/- 100's counts)
2. Linearity correction (optional)
3. Individual sample time offset correction

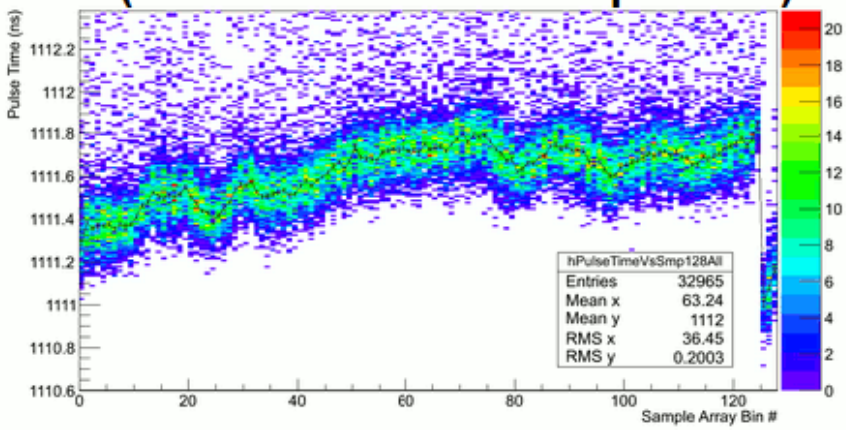
Three sets of calibration constants required:

- **Sample pedestal values**
  - (262144 samples/ASIC)
- **Sample time widths**
  - (128 values per ASIC)
- **Timewalk correction**
  - (~20 values per ASIC)

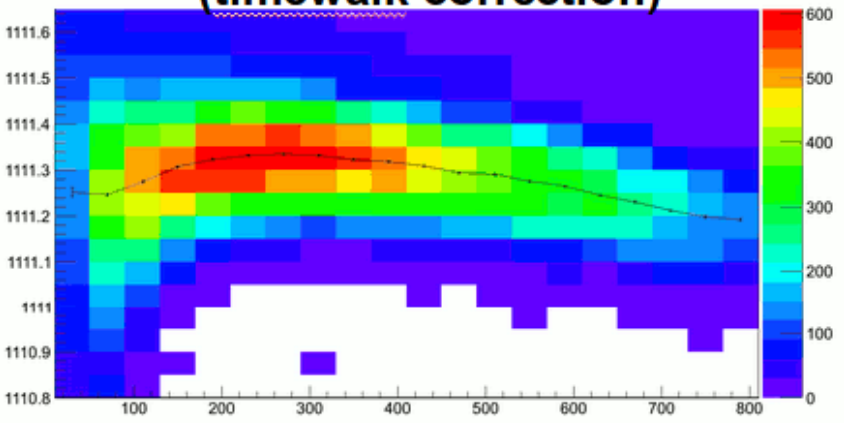
Waveform Pedestal Correction



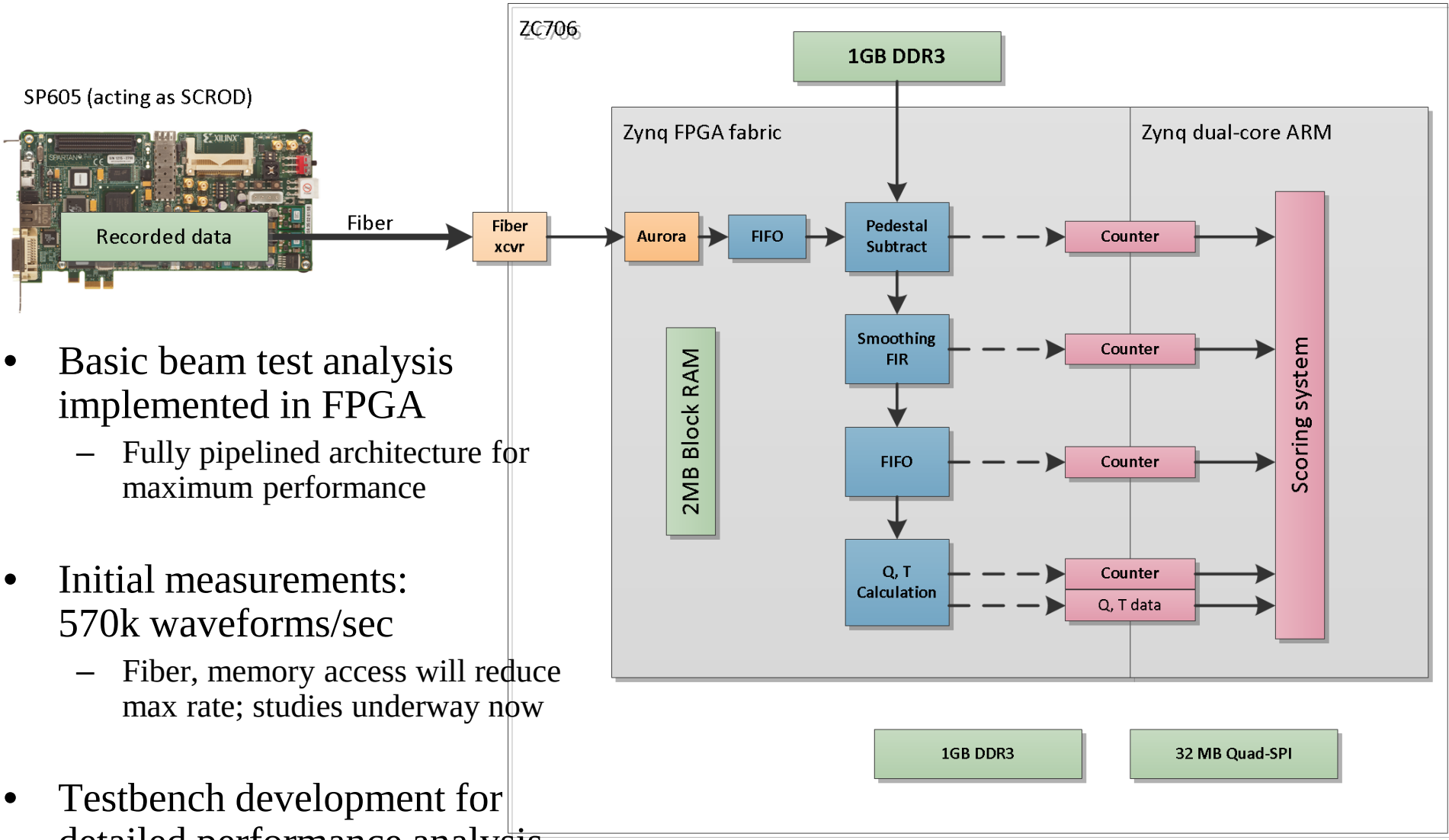
Pulse Time Vs Sample Array Bin # (used to measure Sample-DTs)



Pulse Time Vs Height (timewalk correction)

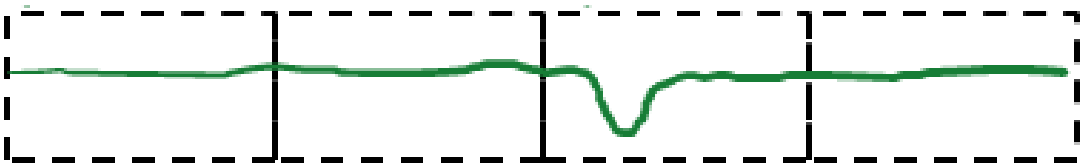


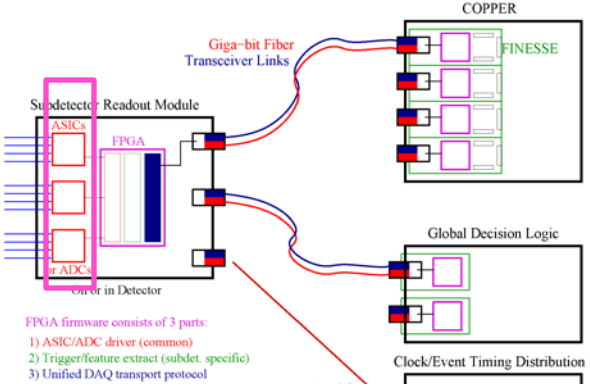
Data Analysis in Hardware

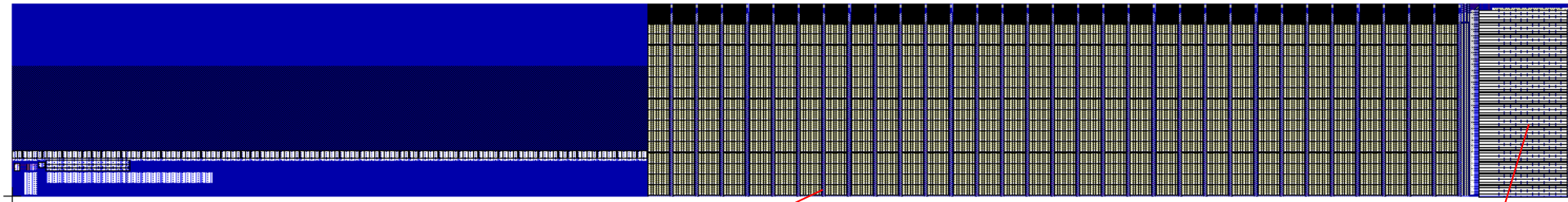


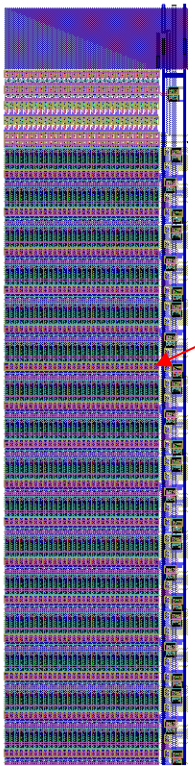
- Basic beam test analysis implemented in FPGA
  - Fully pipelined architecture for maximum performance
- Initial measurements: 570k waveforms/sec
  - Fiber, memory access will reduce max rate; studies underway now
- Testbench development for detailed performance analysis with replayed data underway

Event sampling









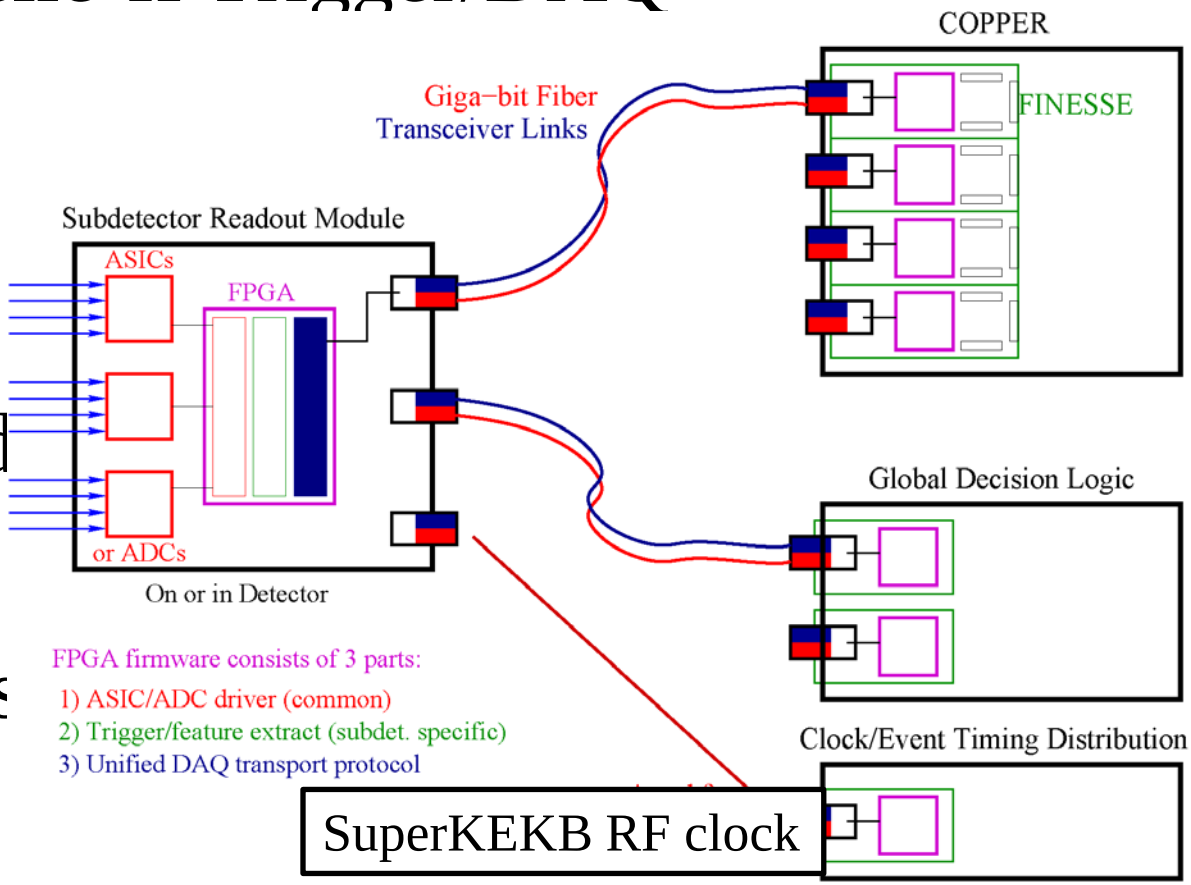
- Sampling: 128 (2x 64) separate transfer lanes

Recording in one set 64, transferring other ("ping-pong")

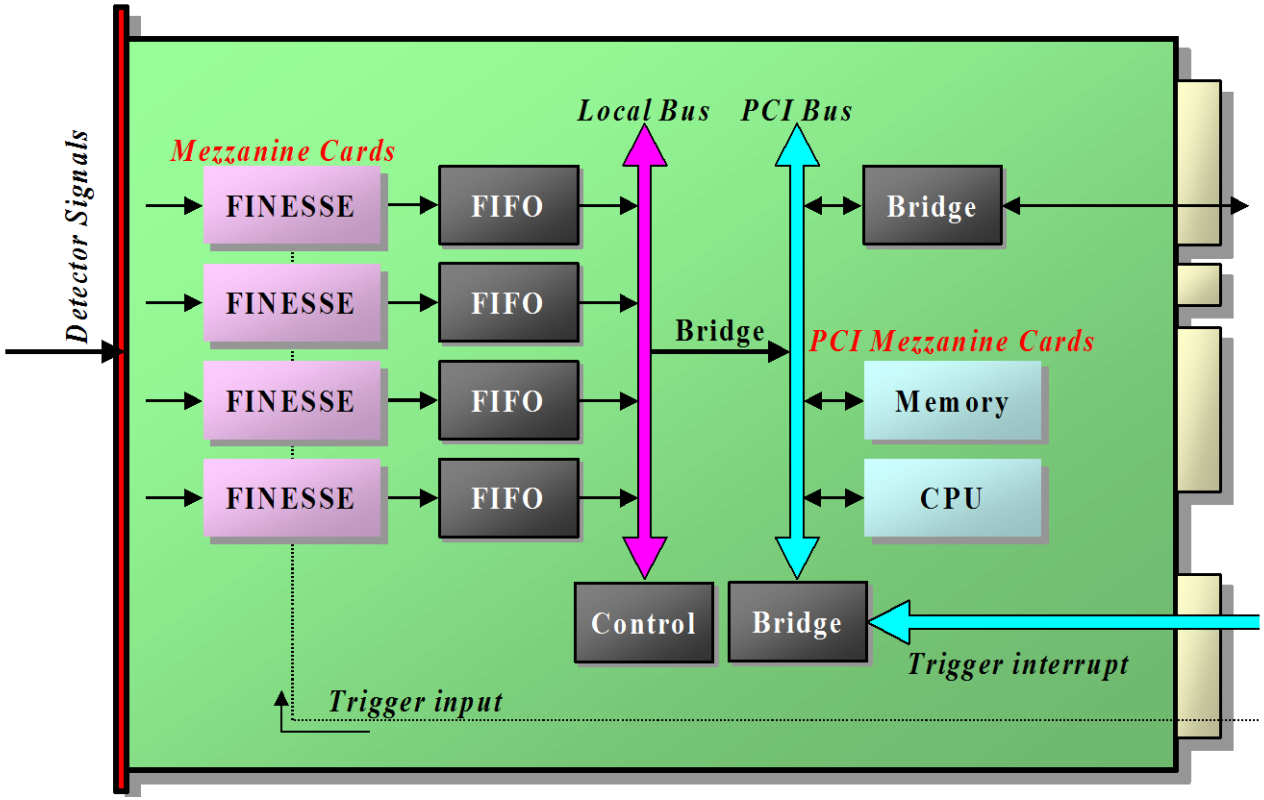
- Storage: 64 x 512 (32k per ch.)
  - Wilkinson ADC (64 at once)
  - 64 conv/channel (512 in parallel)

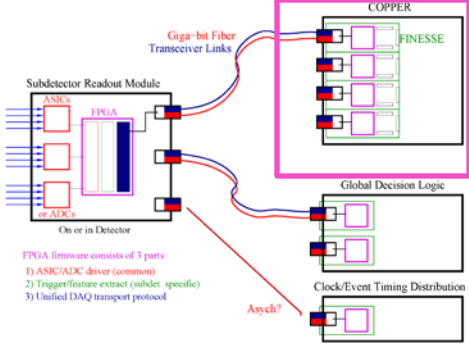
Readout Electronics -- requirements

- Operate within Belle-II Trigger/DAQ environment
- >= 30kHz L1 trig
- Gbps fiber Tx/Rx
- COPPER backend
- Timing trigger
- iTOP: 8k channels
- 16 iTOP modules
- 4x 128-channel SRM/iTOP module (64x total)



Belle II back-end

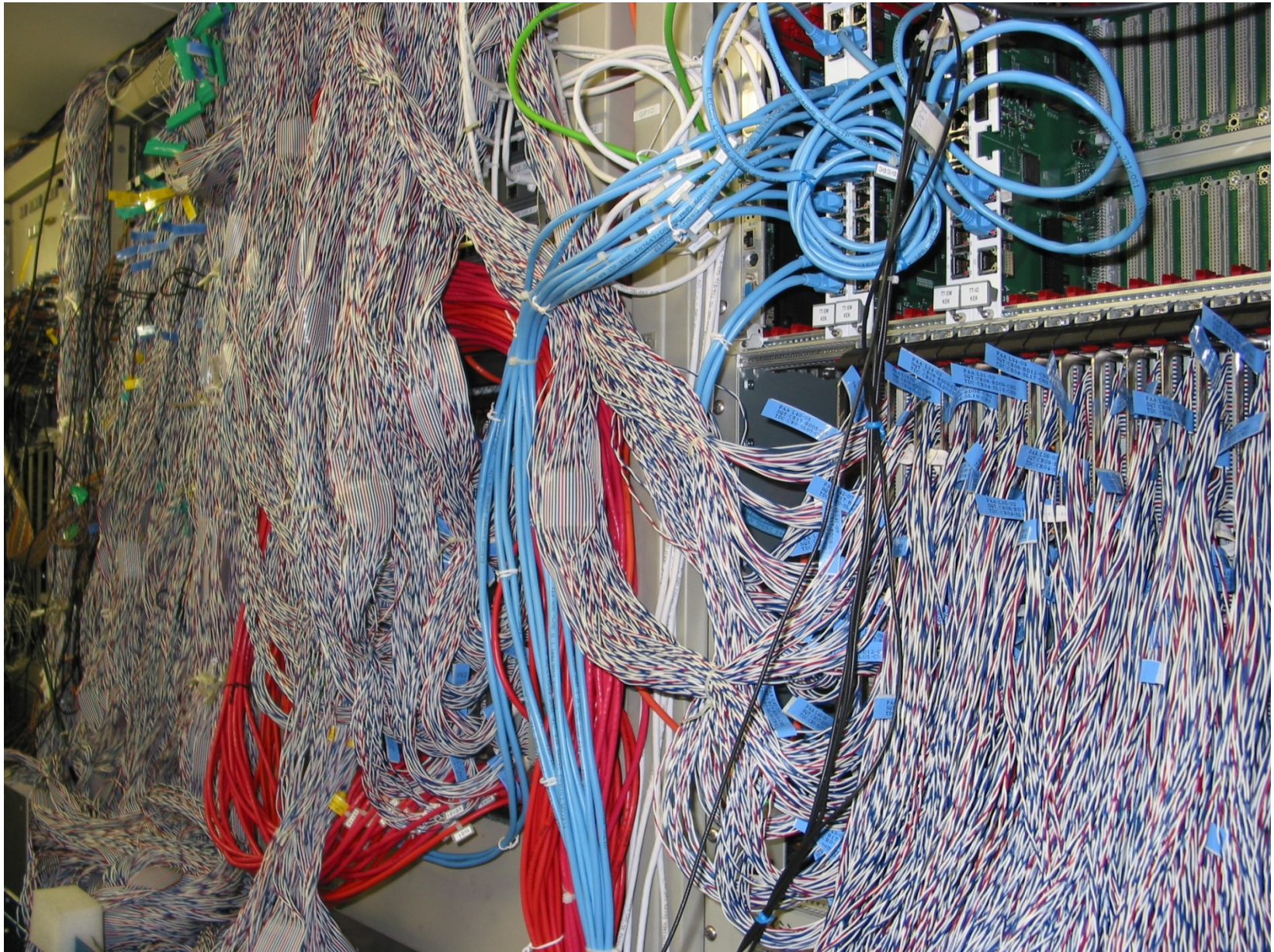




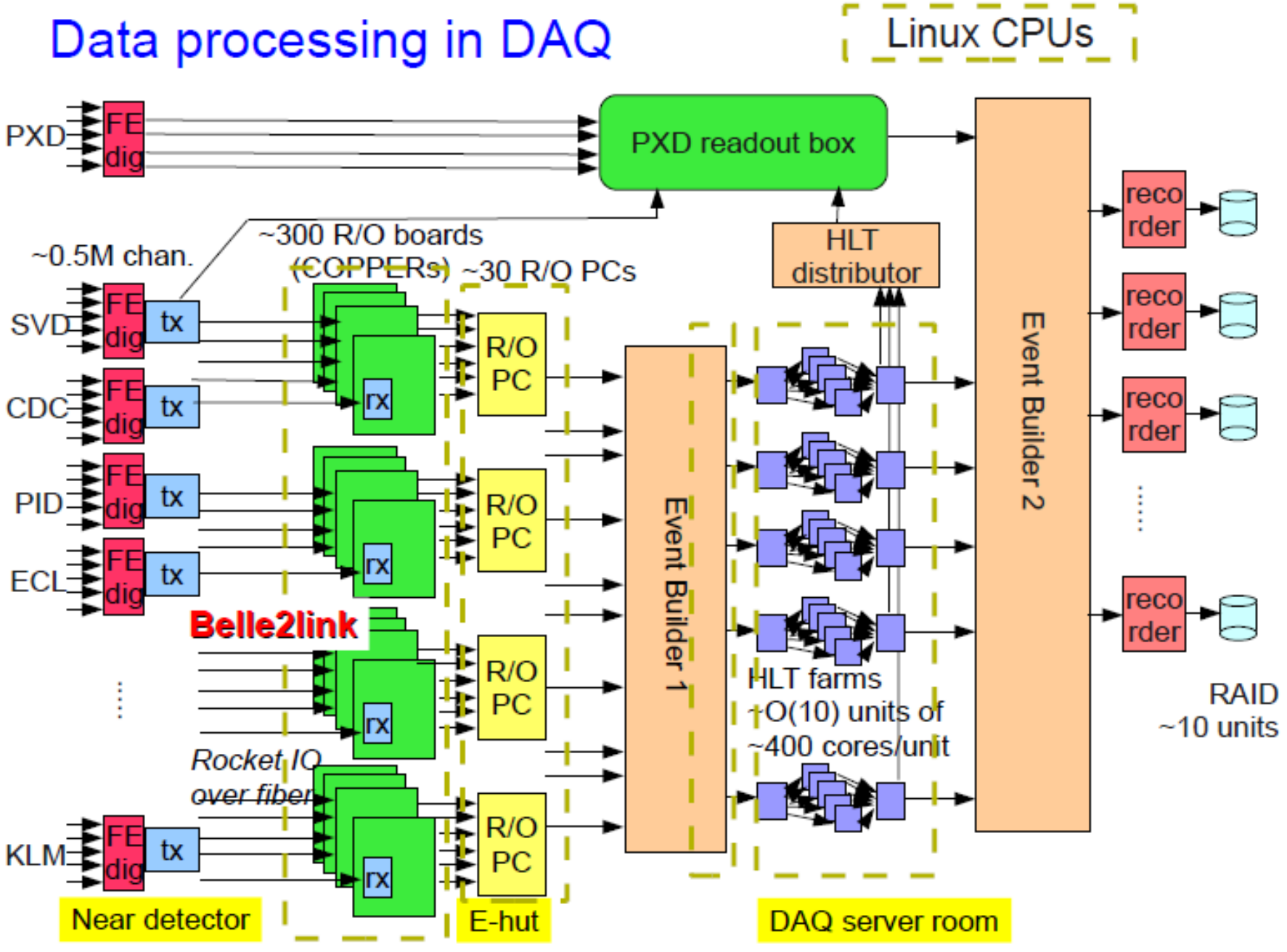
Upgraded for Belle II

- COPPER (COmmon Pipelined Platform for Electronics Readout)
- Used in Belle, J-PARC experiments
- FINESSE (Front-end Instrumentation Entity for Subdetector Specific Electronics)

Belle II DAQ: Got fiber?



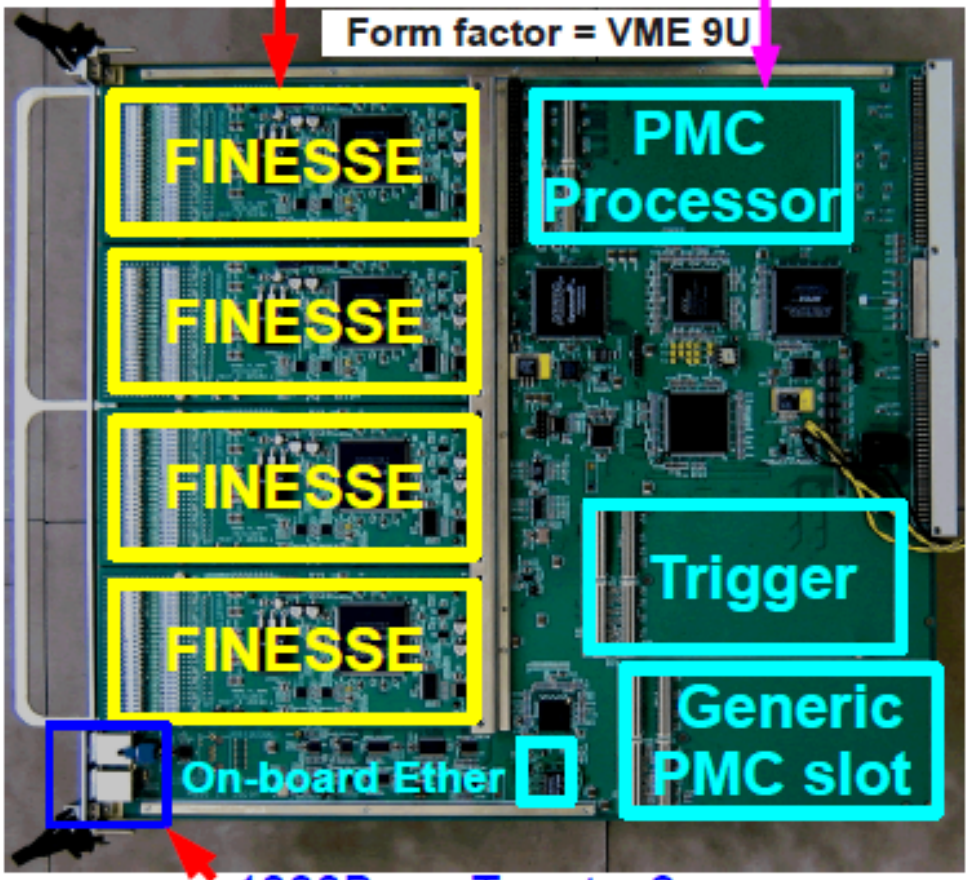
Data processing in DAQ

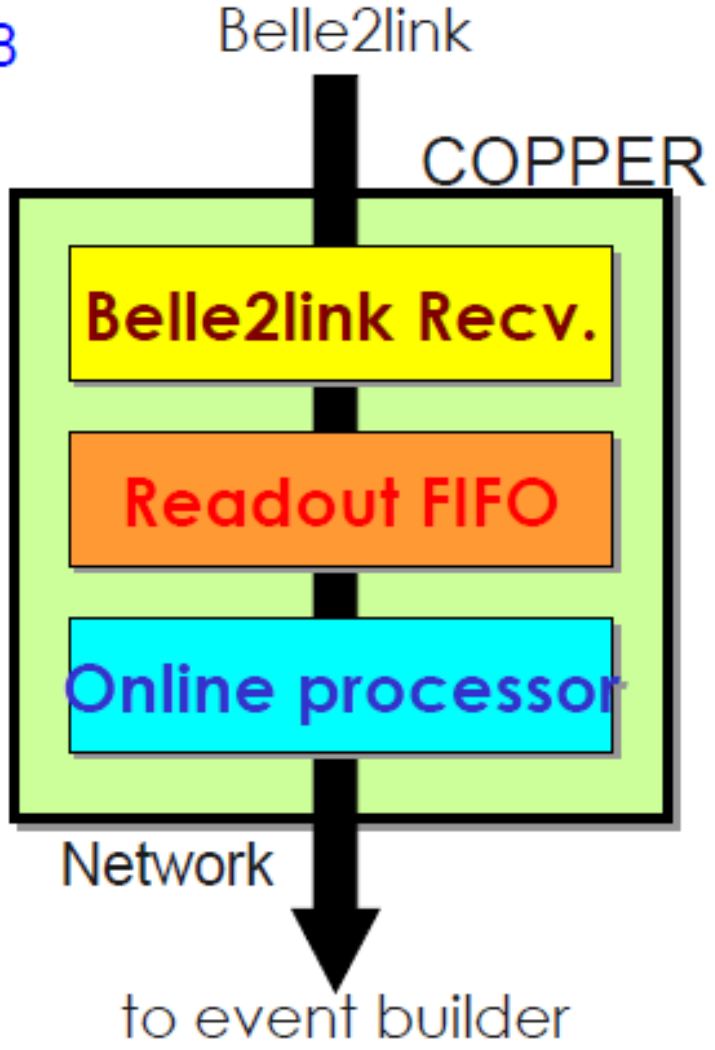


COPPER

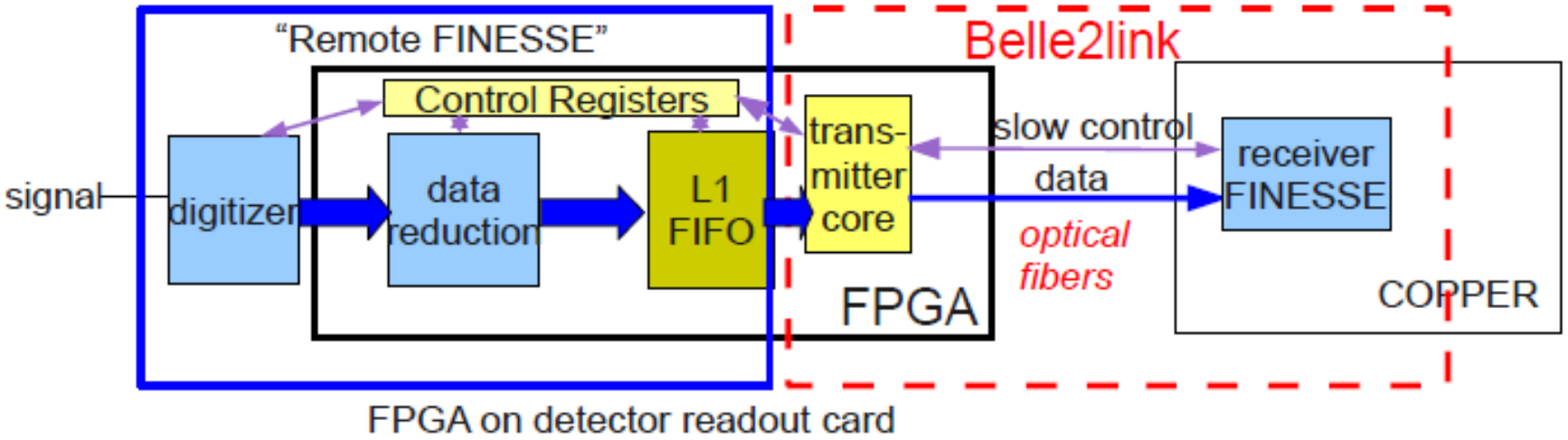
Digitizer cards
(Belle2link recv.)

CPU (Linux)
ATOM 1.6GHz
Memory : 512MB





Belle2link and “remote” FINESSE



- In the FPGA on detector front-end card, “virtual” FINESSE” is implemented, and it talks with “Belle2link transmitter core”.

- In COPPER, Belle2link receiver(HSLB) is implemented instead of digitizer FINESSE, and connected to front-end card via optical fibers.

- The receiver “remote controls” the “virtual FINESSE” (slow control) and receives the data stream via optical fibers as if the remote FINESSE is implemented on the COPPER.

Trigger/Timing Distribution (FTSW)

From Nakao-san's documentation:

20110805 version

Timing signals over CAT7 cables

7 ports, O1 to O7

ACK →	ACK: 254 Mbps serialized, unused
TRG ←	TRG: 254 Mbps serialized
RSV ←	RSV: pulled down to GND
CLK ←	CLK: 127 Mhz

JTAG signals over CAT7 cables

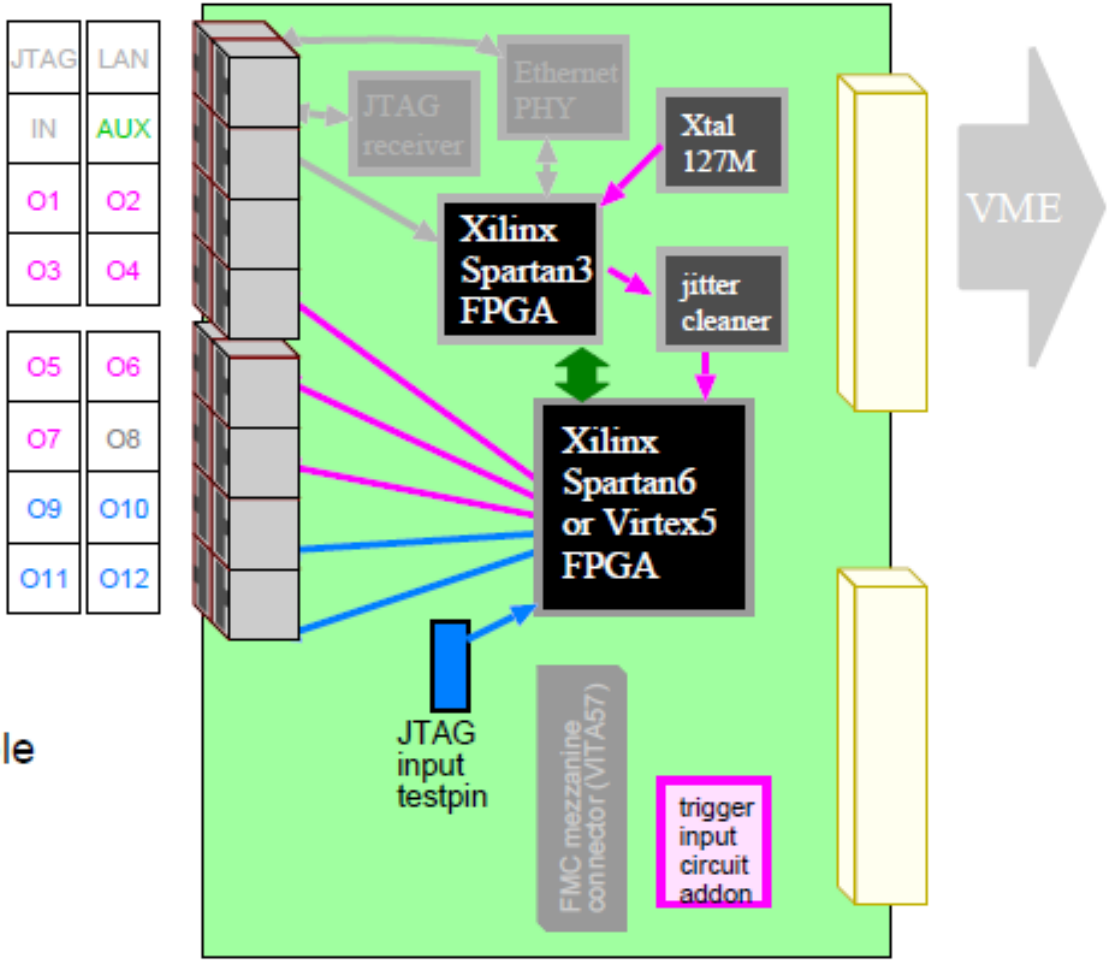
4 ports, O9 to O12

TCK ←
TMS ←
TDI ←
TDO →

Monitoring signals over a CAT7 cable

AUX port

trgin ←	copy of trigger input
trg21 ←	latched with 21MHz clock
trgpulse ←	trgin and (not trg21)
clk21 ←	21MHz clock



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JTAG	LAN
IN	AUX
O1	O2
O3	O4
O5	O6
O7	O8
O9	O10
O11	O12

JTAG signals over CAT7 cables

4 ports, O9 to O12

TCK	←
TMS	←
TDI	←
TDO	→

Monitoring signals over a CAT7 cable

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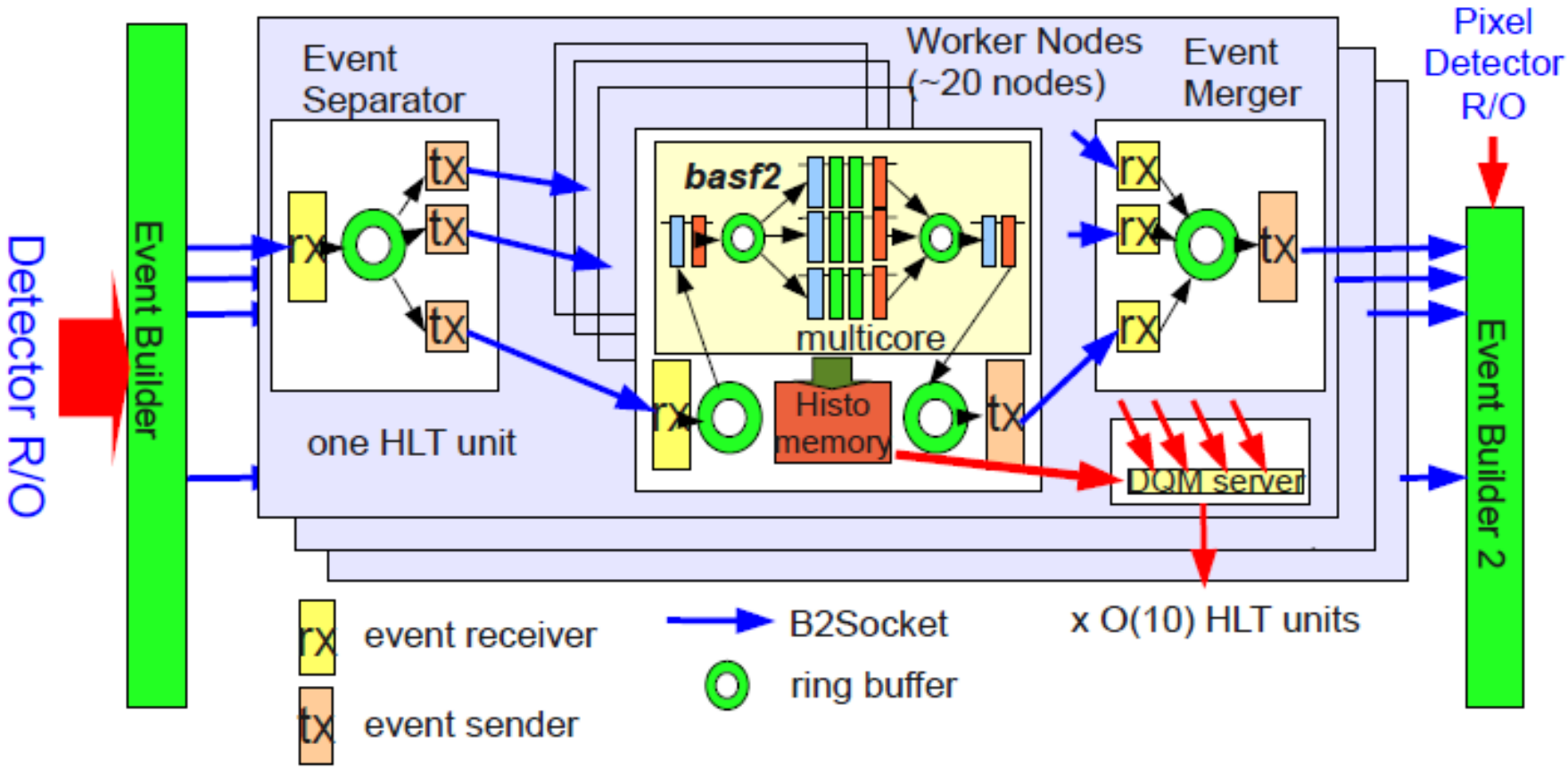
VME

High Level Trigger (HLT)

- Unit structure (O(10))
  - * to reduce the number of output port of event builder
  - * to keep up with the gradial luminosity increase
  - * fault-tolerant : each unit is completely independent
- Based on the parallel processing technology developed for basf2



Belle II Throughput

Estimated event size and bandwidth

Assumed L1 rate = 30kHz (maximum of average)

	#ch	occ [%]	#link	/link [B/s]	FNS	#CPR	ch sz [B]	ev sz [B]	total [B/s]	/CPR [B/s]
PXD	8M	2	40	455M	—	—	4	800k	18.2G	—
SVD	243456	1.9	40	13.8M	HSLB	40	4	18.5k	555M	13.8M
CDC	14336	10	302	0.6M	HSLB	75	4	6k	175M	2.3M
BPID	8192	2.5	128	7.5M	DSP	16	16	4k	120M	8M
EPID	65664	1.5	78	1.1M	HSLB	20	2.8	2.8k	84M	4.2M
ECL	8736	33	52	7.7M	HSLB	26	4	12k	360M	15M
BKLM	19008	1	16	9.7M	HSLB	6	8	2K	60M	10M
EKLM	16800	2	66	19.5M	HSLB	to be fixed	4	1.4k	42M	5.3M
TRG					HSLB	10				

Expected data rate/size reduction for L1 trigger rate=30kHz with loose HLT trigger + Final trigger at PromptReco