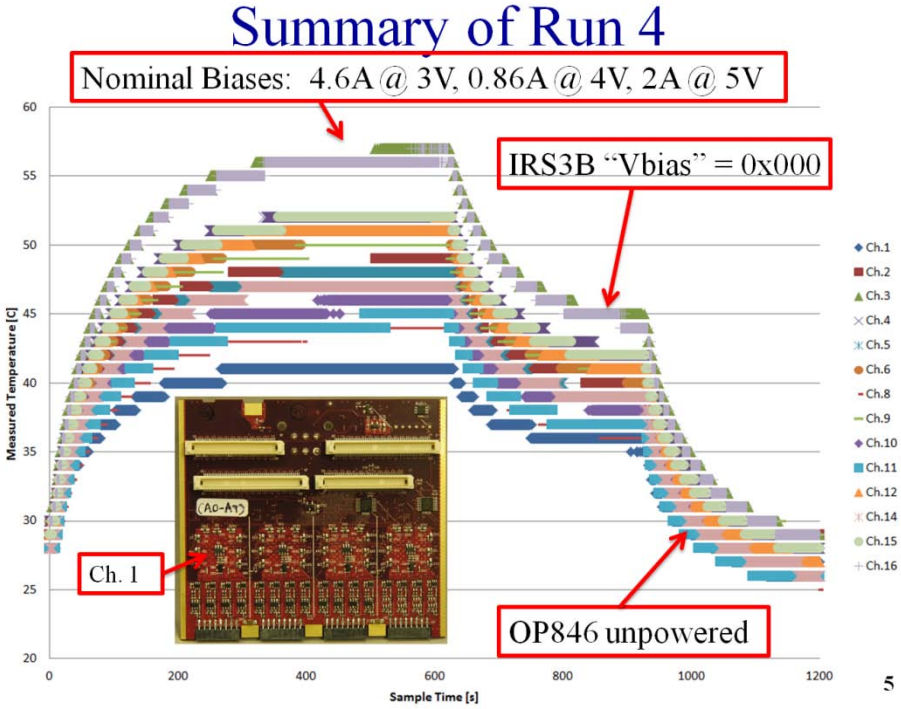
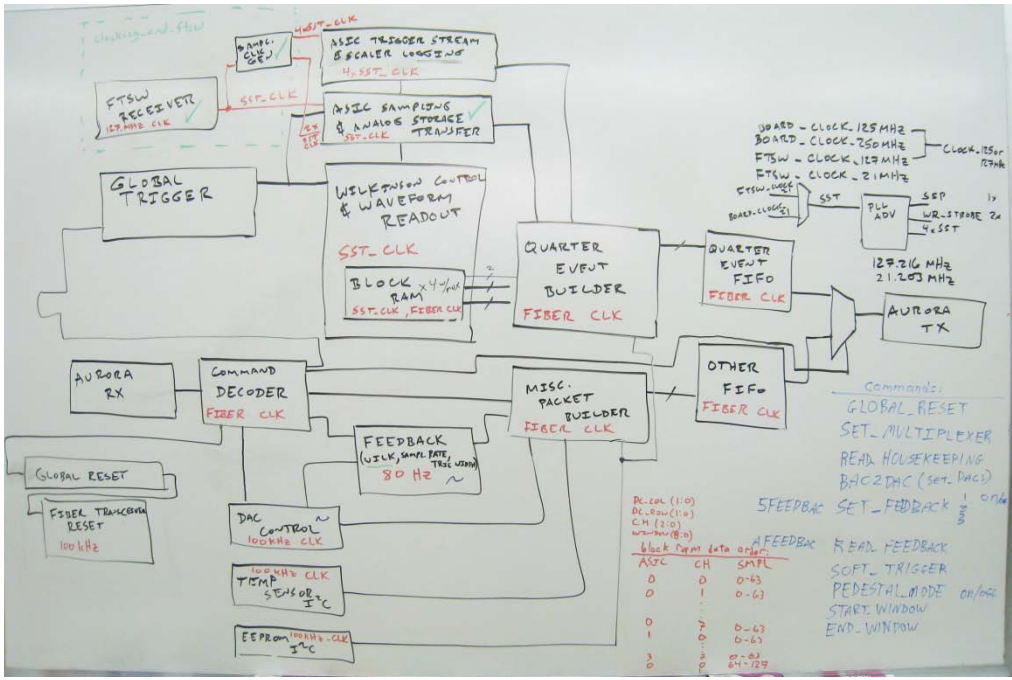
Understanding IRS3B, board-stack and mTC operation/calibration





Gary S. Varner

1 JUL 2014

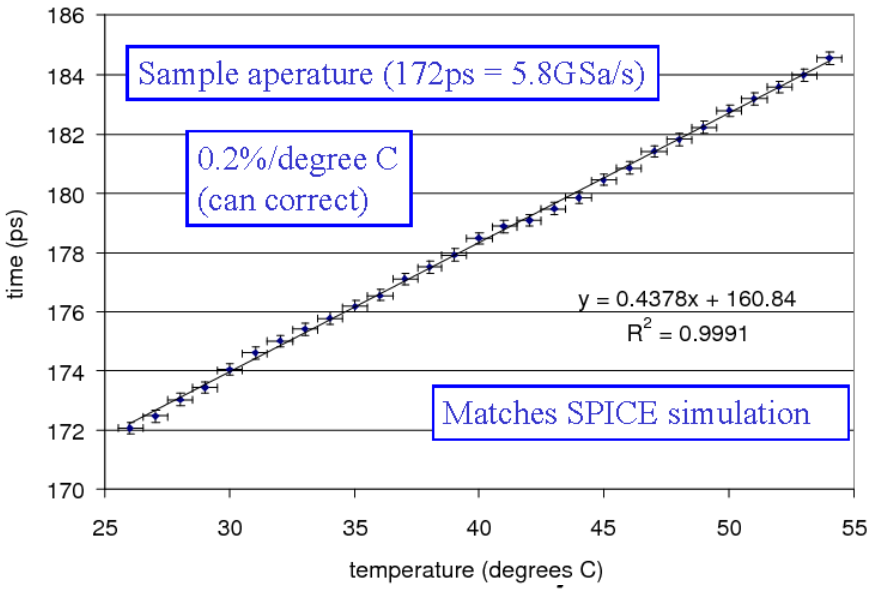
mTC Training Session #2

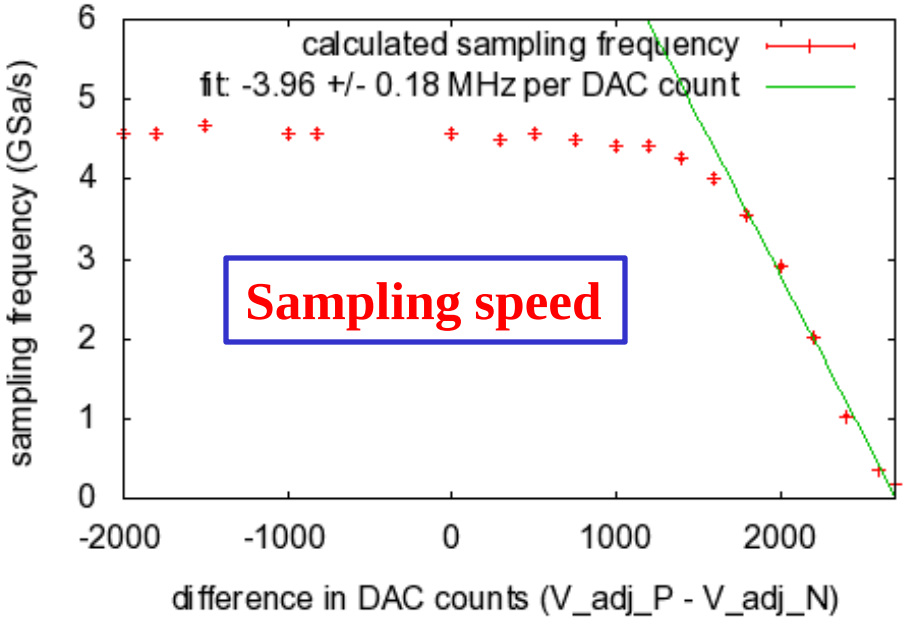
Roadmap

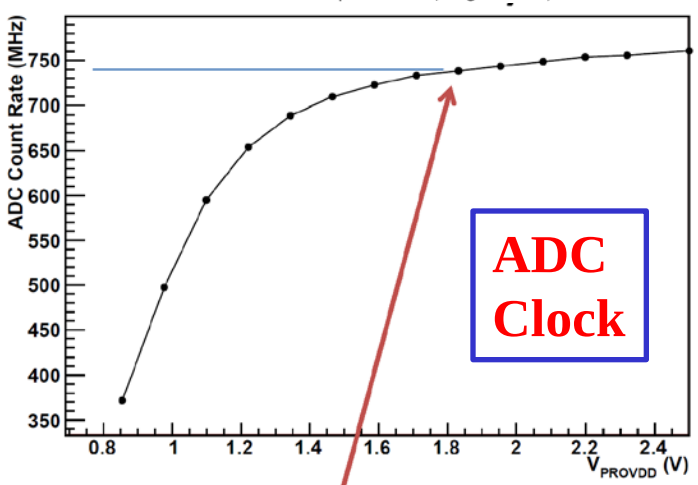
- mTC Readout
  - Currently at about Phase 1.5
  - You can get us to Phase 2.5
- Specifically
  - Operators need to understand Hardware/Firmware/Software
  - Develop real-time Data Quality Monitoring
- What I hope to convey:
  1. Details of the hardware: ASIC + boardstack
  2. Firmware and Configuration/Operating parameters
  3. Understand how to read and comprehend documentation and ask meaningful questions (“it doesn’t work” notably not amongst them)

Servo-controls (3 parameters)

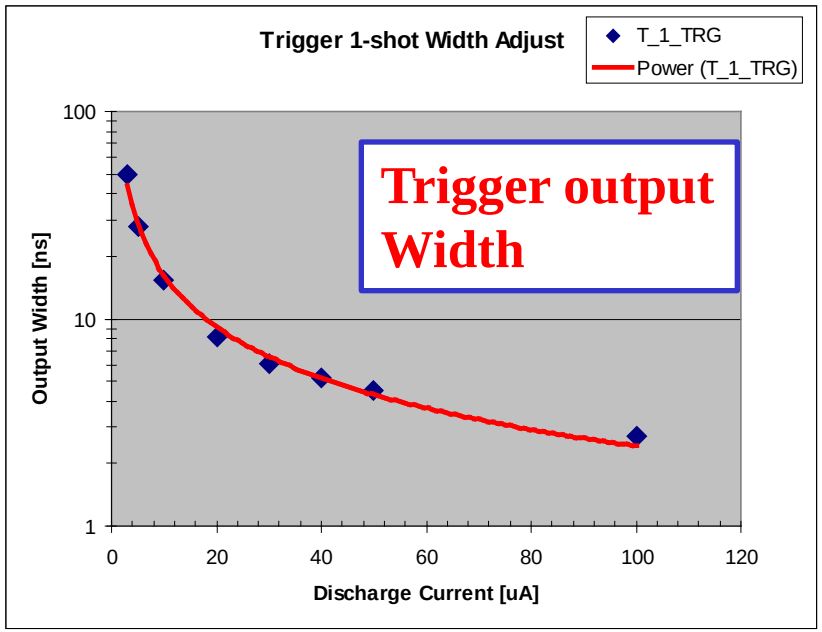
Temperature Dependence





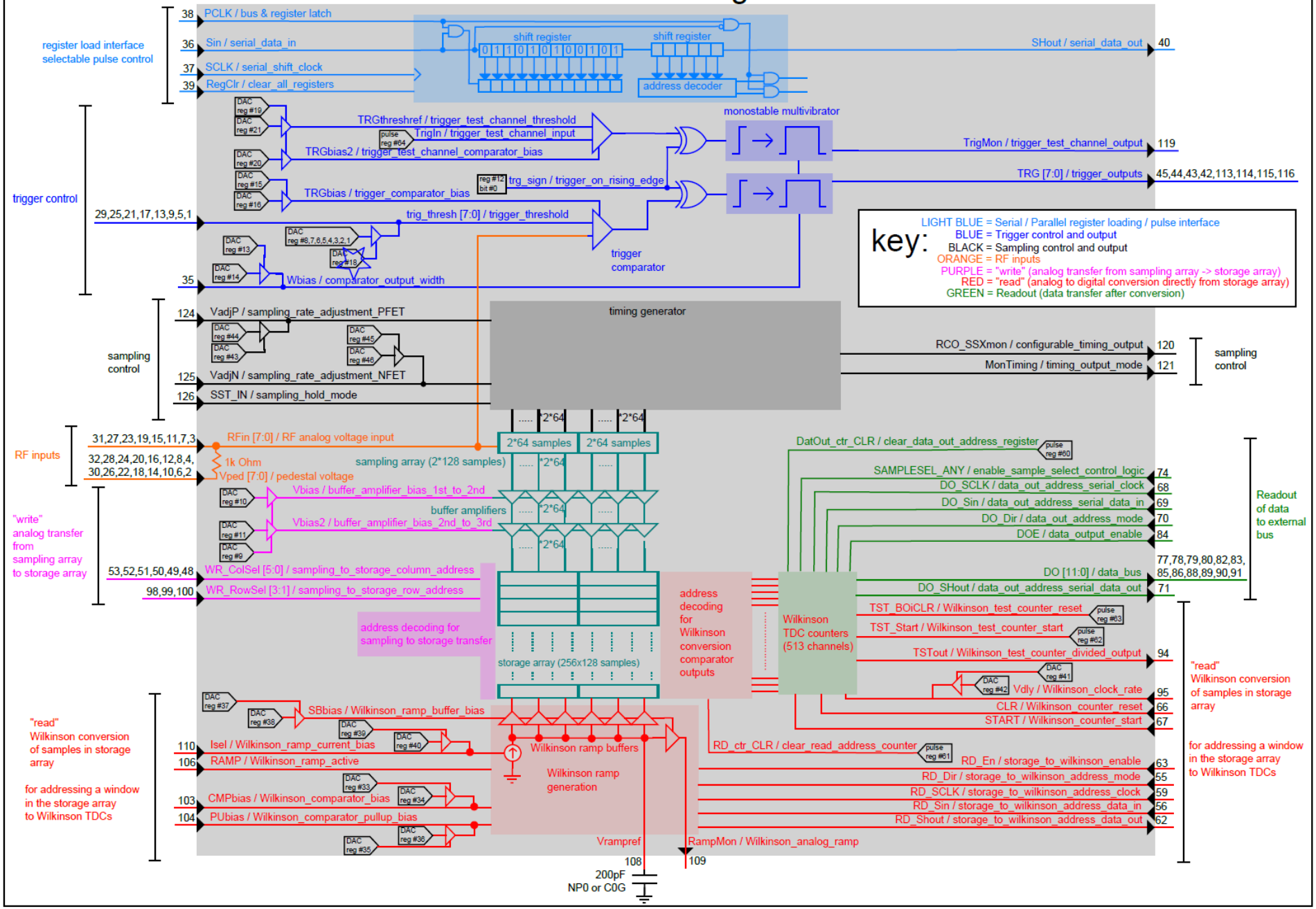


This is the Wilkinson clock adjustment



IRS3B block diagram

2012-10-23



http://www.phys.hawaii.edu/~mza/ASIC/IRS2-BLAB3A/index.html

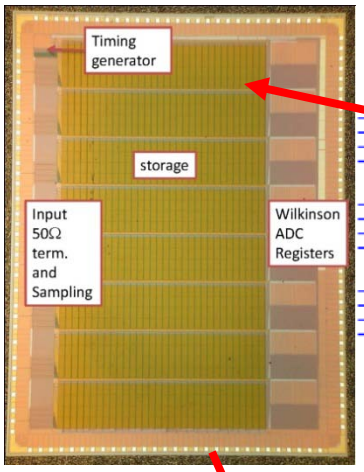
"PCLK #"	Register/Value	Default value	# bits		
1	Threshold Ch. 1	TBD (0x000)	12	scan required	
2	Threshold Ch. 2	TBD (0x000)	12		
3	Threshold Ch. 3	TBD (0x000)	12		
4	Threshold Ch. 4	TBD (0x000)	12		
5	Threshold Ch. 5	TBD (0x000)	12		
6	Threshold Ch. 6	TBD (0x000)	12		
7	Threshold Ch. 7	TBD (0x000)	12		
8	Threshold Ch. 8	TBD (0x000)	12		
9	VBDbias	0x400	12	DAC buff bias for Vbias, Vbias2	
10	Vbias	0x380	12	Buff amp bias -- initial sample	
11	Vbias2	0x370	12	Buff amp bias -- transfer samples	
12	Misc Reg (incl. SGN)	0x000	8		
13	WBDbias	0x400	12	DAC buff bias for Wbias	
14	Wbias	0x3D7	12	Trigger Width adjust (Wbias)	
15	TCBbias	0x400	12	DAC buff bias for Trigger Comparator	
16	TRGbias	0x350	12	Trigger Comparator bias	
17	THDbias	0x400	12	DAC buff bias for Trigger Thresholds	
18	Tbbias	0x400	12	Internal Trigger Threshold buffer bias	(disable for external drive)
19	TRGDbias	0x400	12	DAC buff bias for TRGbias2, TRGthref	
20	TRGbias2	0x350	12	TRGbias for reference channel	
21	TRGthref	0x800	12	Trigger threshold for reference channel	
22	Leading Edge SSPin	0x060	8	Timing Gen: SSPin	
23	Trailing Edge SSPin	0x010	8		
24	Leading Edge S1	0x028	8	Timing Gen: S1	
25	Trailing Edge S1	0x058	8		
26	Leading Edge S2	0x068	8	Timing Gen: S2	
27	Trailing Edge S2	0x018	8		
28	Leading Edge PHASE	0x018	8	Timing Gen: PHASE	
29	Trailing Edge PHASE	0x030	8		
30	Leading Edge WR_STRB	0x040	8	Timing Gen: WR_STRB	NOTE: WR_ADDR phase CRITICAL
31	Trailing Edge WR_STRB	0x070	8		
32	Timing Generator Reg	0x***	8	Select Timing signals viewed, Phase clear, RCO running	decode for
33	PDDbias	0x400	12	DAC buff bias for CMPbias	
34	CMPbias	0x500	12	Storage Cell Comparators (Pull-Down) bias	
35	PUDbias	0x400	12	DAC buff bias for CMPbias	
36	PUbias	0xBF0	12	Storage Column Comparators (Pull-Up) bias	
37	SBDbias	0x400	12	DAC buff bias for Super Buffer bias	
38	Sbbias	0x400	12	Super Buffer bias	
39	ISDbias	0x400	12	DAC buff bias for ISEL	
40	ISEL	0x900	12	Voltage Ramp Current	Initial config required
41	VDDbias	0x400	12	DAC buff bias for Vdly	
42	Vdly	0xB54	12	Wilkinson counter adj voltage	Servo-lock target value
43	VAPDbias	0x600	12	DAC buff bias for VadjP	
44	VadjP	0x5E8	12	Timing Generator delay adjust PMOS	Initial config required
45	VANDbias	0x600	12	DAC buff bias for VadjN	
46	VadjN	0xAD0	12	Timing Generator delay adjust NMOS	Servo-lock target value
60	DatOut_ctr_CLR	AddrMode	ADDR_M	Clear Data Output Address Registers	
61	RD_ctr_CLR	AddrMode	ADDR_M	Clear Read Address Registers	
62	Start_WilkMon	AddrMode	ADDR_M	Start Wilkinson Reference counter	
63	Boin_CLR	AddrMode	ADDR_M	Stop/Clear Wilkinson Reference counter	
64	Trig_In	AddrMode	ADDR_M	Pulse Trigger test circuit	

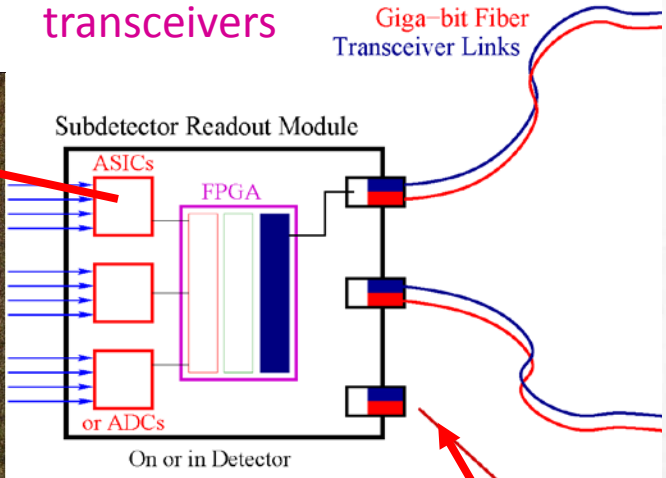
Hopefully, these will start to make sense in terms of how these settings map onto operational parameters of the IRS3B ASIC

mTC Readout

IRS3B sampling ASIC

12 DAQ fiber transceivers





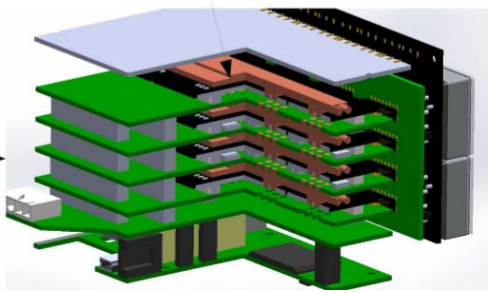
FPGA firmware consists of 3 parts:

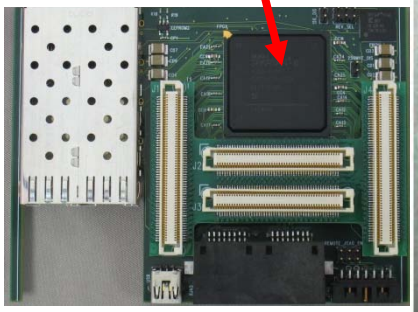
1) ASIC/ADC driver (common)
2) Trigger/feature extract (subdet. specific)
3) Unified DAQ transport protocol

1,536 channels

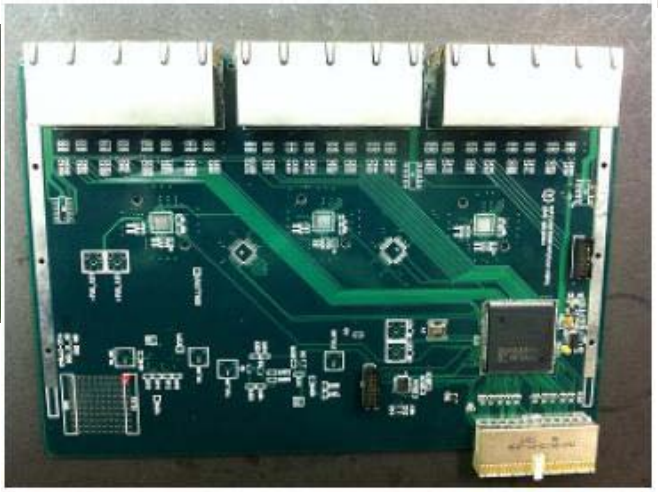
192 8-ch. ASICs

12 SRM "board stacks"



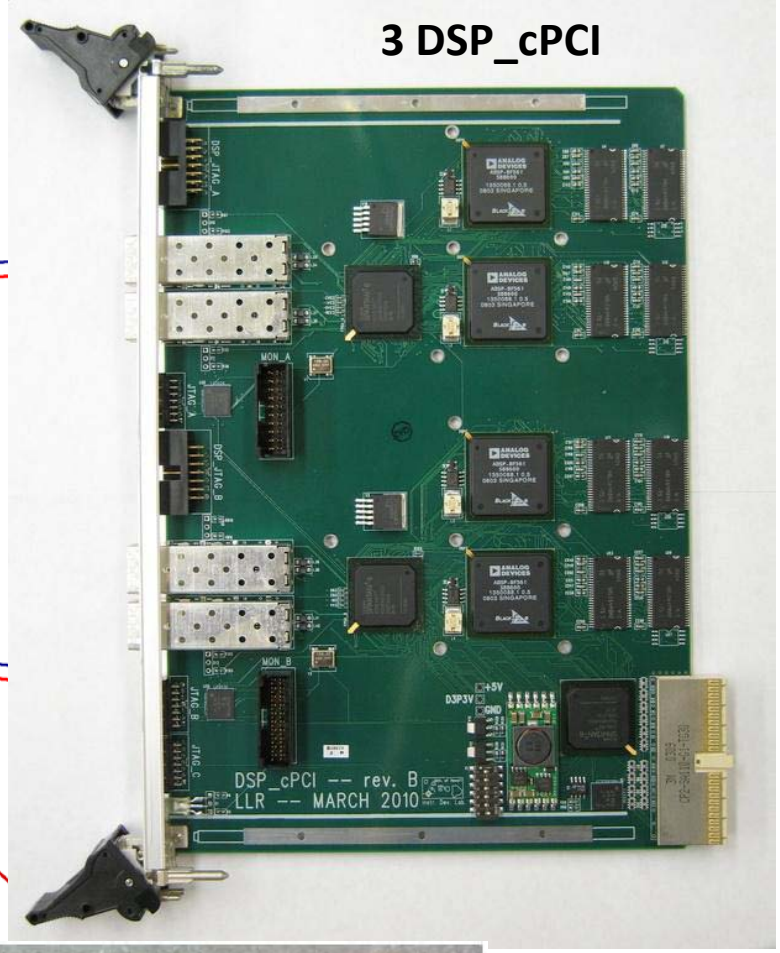


12 SCROD

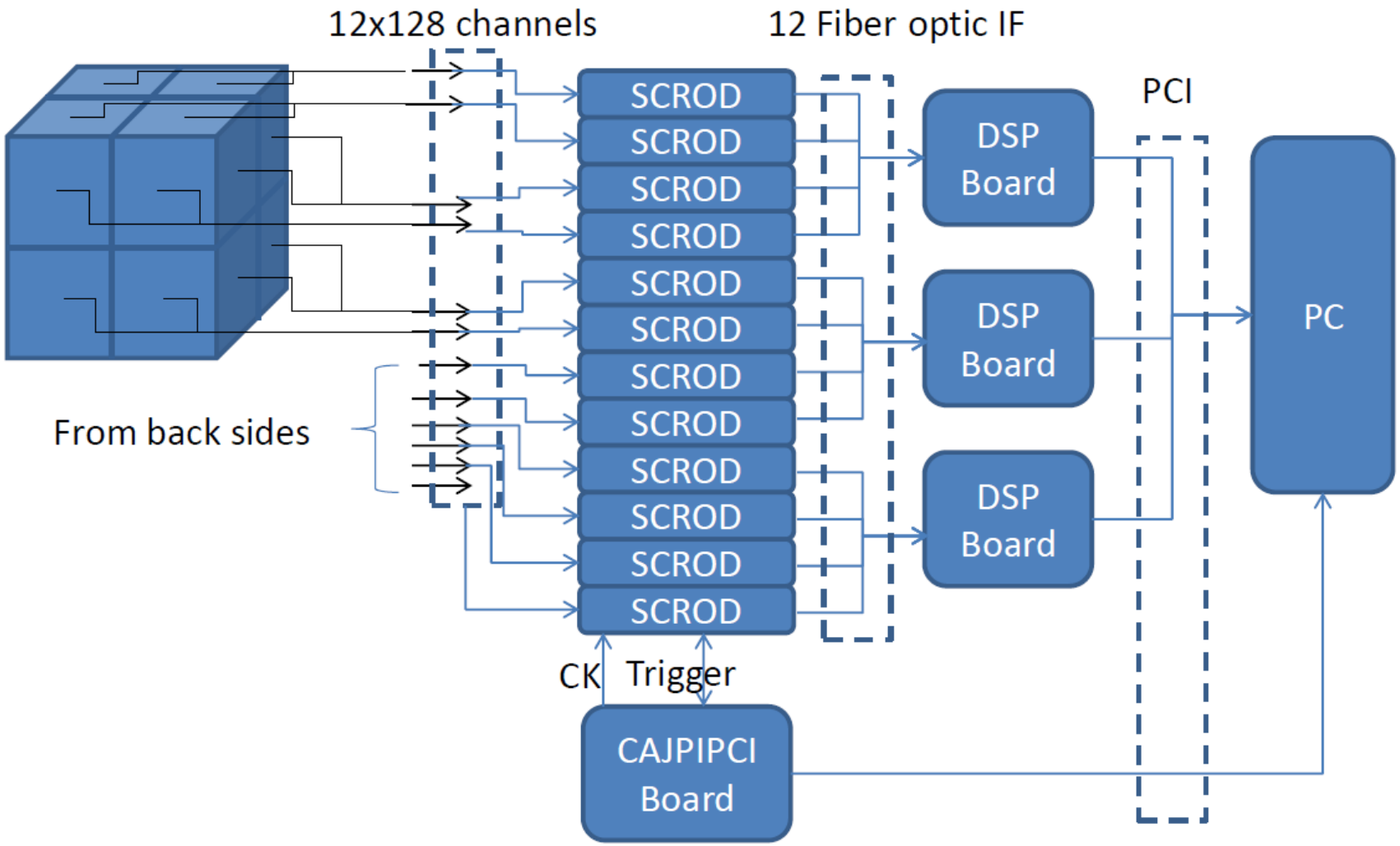


CAJIPCI clock, trigger, programming

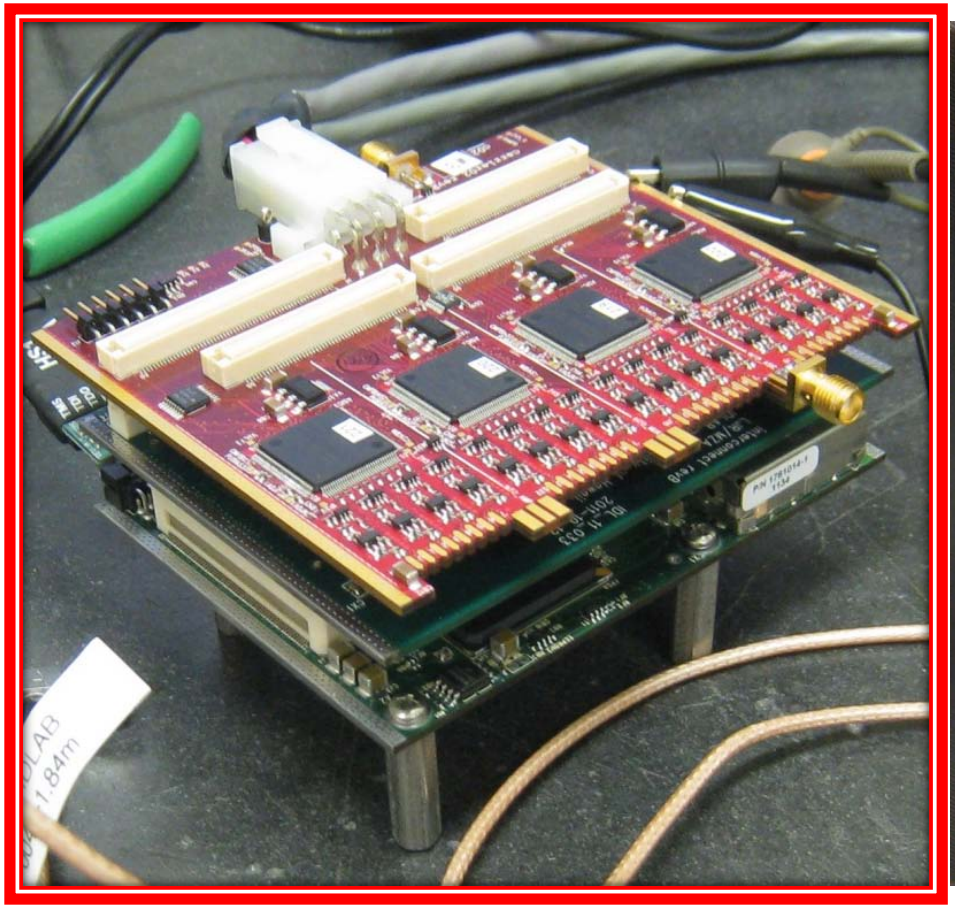
3 DSP_cPCI



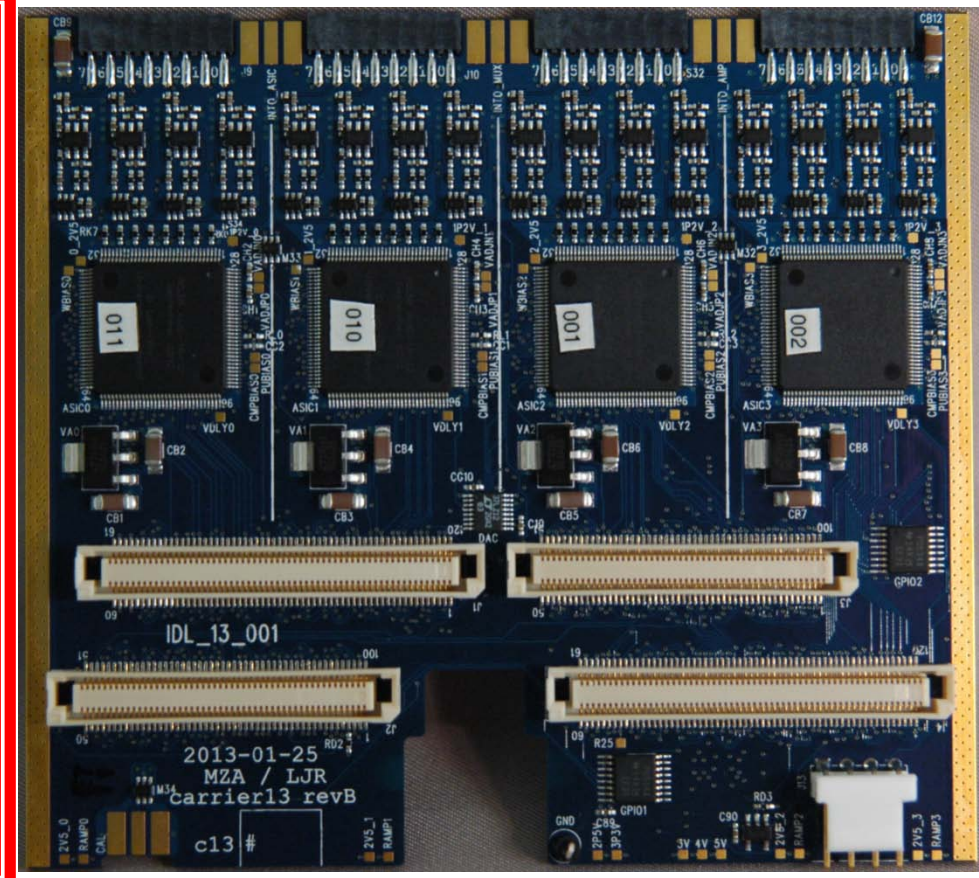
mTC electronics system



Carrier cards

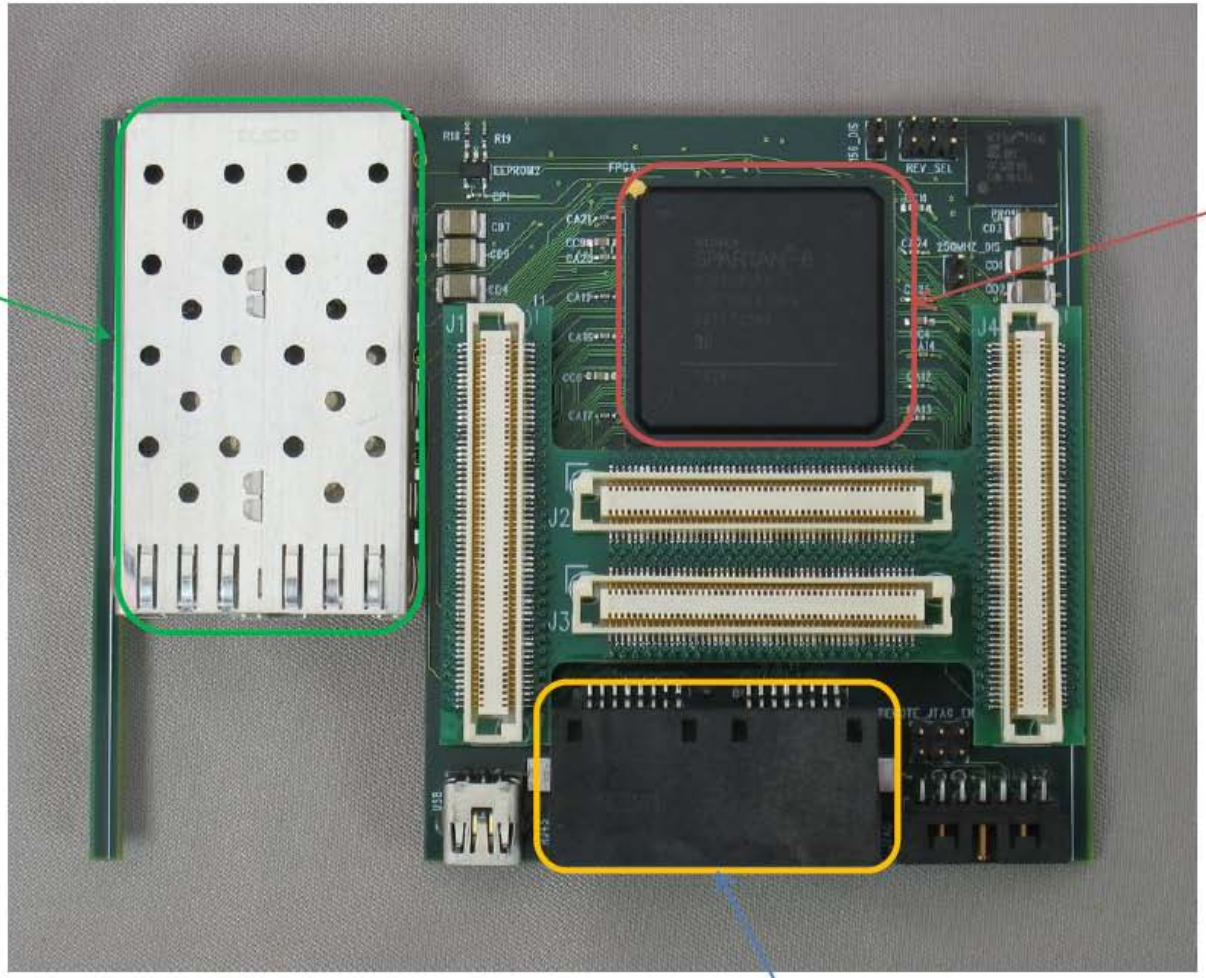


Carrier 0 or 2 (c02)

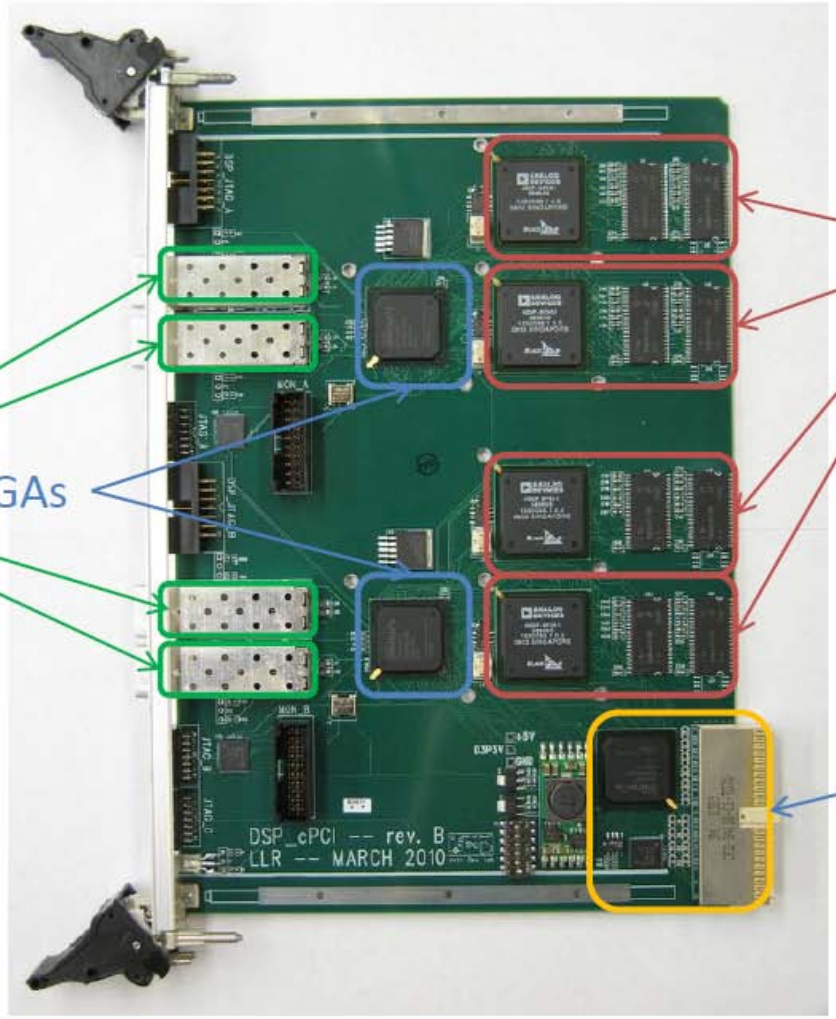


Carrier 1 or 3 (c13)

SCROD



DSP_cPCI



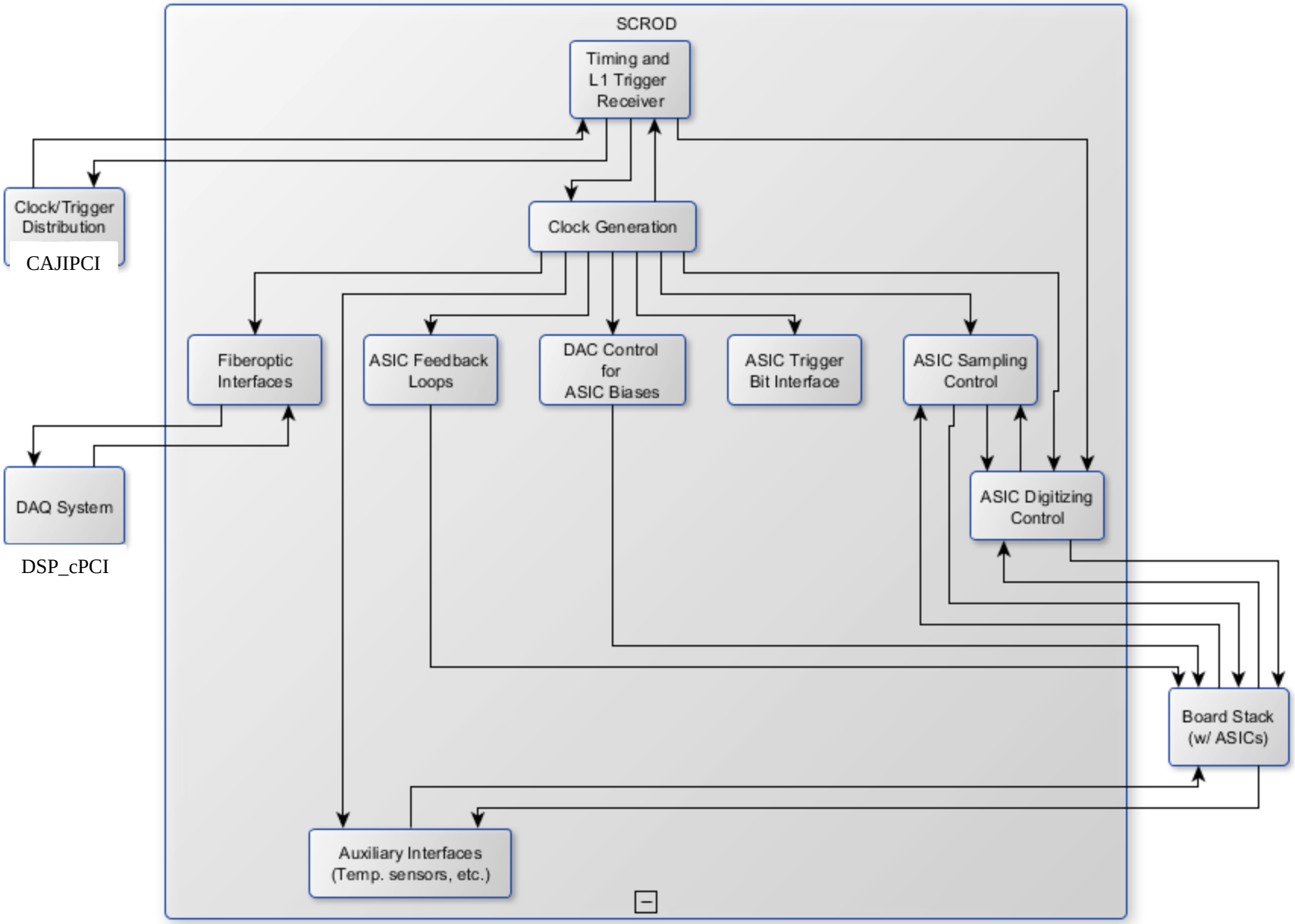
4 Fiber Optic Interfaces

2 FPGAs

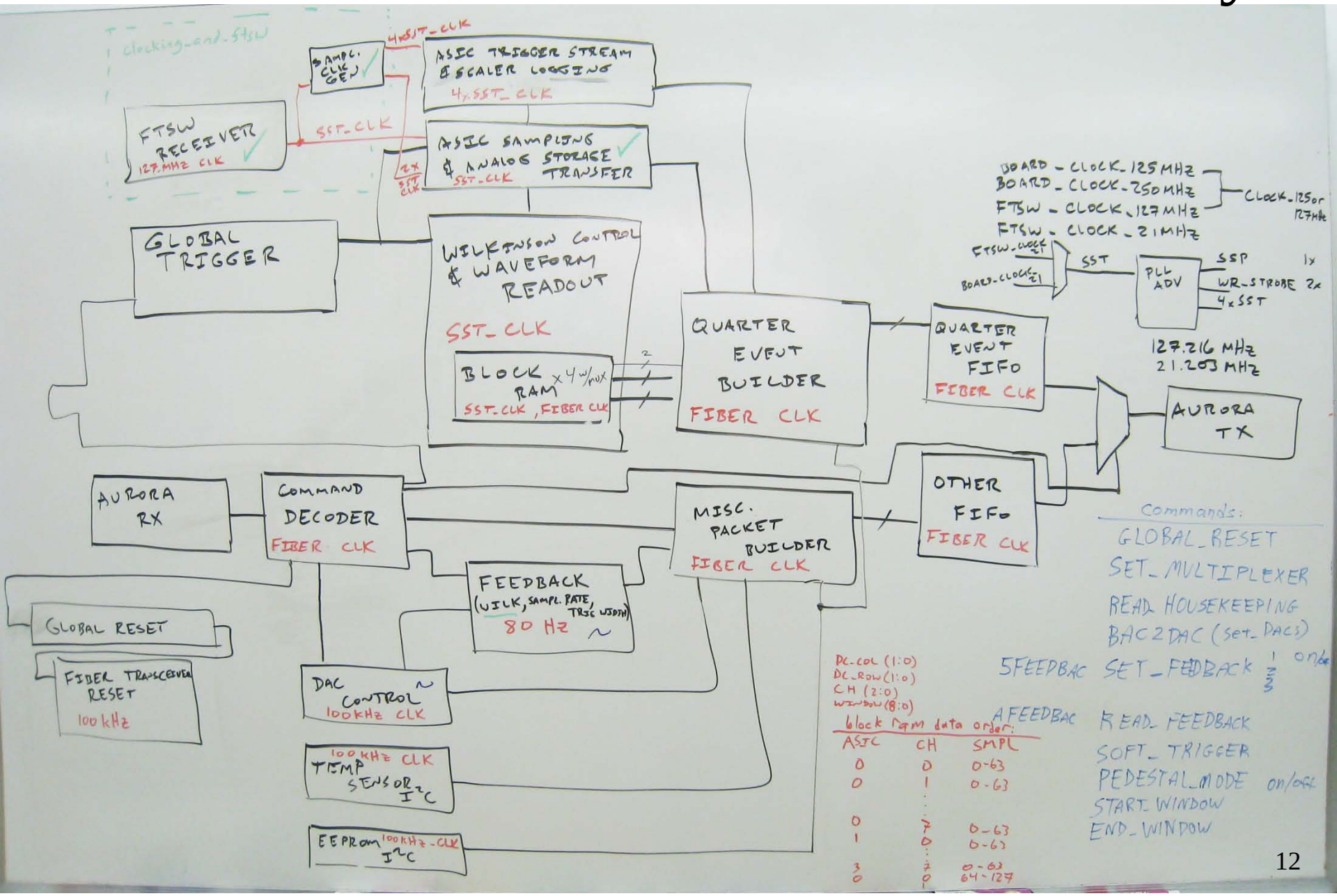
4 DSP + RAM

FPGA – PCI interface

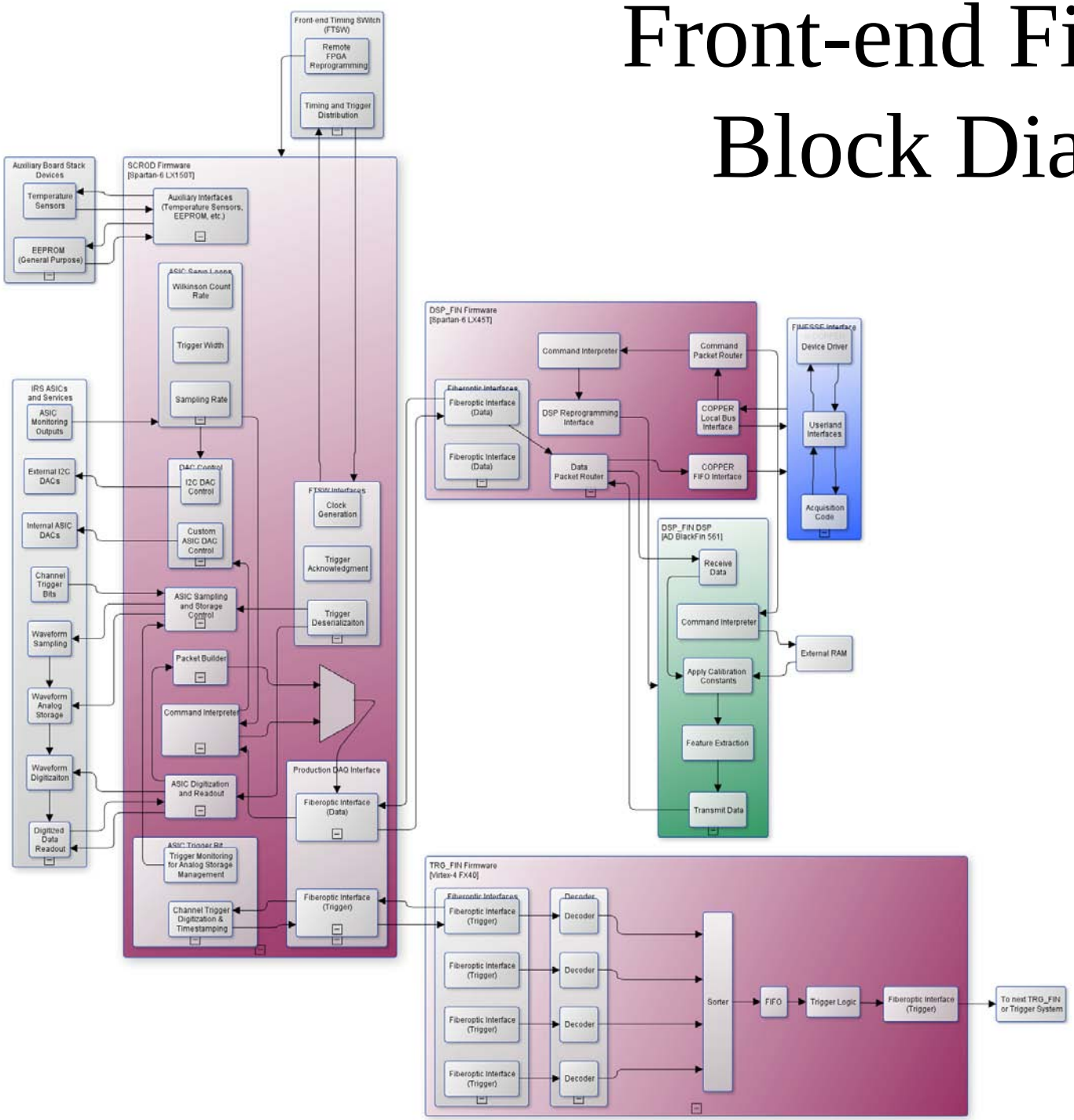
Front-end Firmware Block Diagram



Reality


clocking_end_ftsw
SAMPL. CLK GEN
4xSST_CLK
ASIC TRIGGER STREAM & SCALER LOGGING
4x SST_CLK
FTSW RECEIVER
127 MHz CLK
SST_CLK
ASIC SAMPLING & ANALOG STORAGE TRANSFER
SST_CLK
2x SST CLK
GLOBAL TRIGGER
WILKINSON CONTROL & WAVEFORM READOUT
SST_CLK
BLOCK RAM x4 w/mux
SST_CLK, FIBER CLK
QUARTER EVENT BUILDER
FIBER CLK
QUARTER EVENT FIFO
FIBER CLK
AURORA TX
BOARD_CLOCK_125MHz
BOARD_CLOCK_250MHz
FTSW_CLOCK_127MHz
FTSW_CLOCK_21MHz
CLOCK_125or127MHz
FTSW_CLOCK/21
BOARD_CLOCK/21
SST
PLL ADV
SSP
WR_STROBE 2x
4xSST
1x
127.216 MHz
21.203 MHz
AURORA RX
COMMAND DECODER
FIBER CLK
MISC. PACKET BUILDER
FIBER CLK
OTHER FIFO
FIBER CLK
FEEDBACK (WILK, SAMPL. RATE, TRIG WIDTH)
80 Hz
GLOBAL RESET
FIBER TRANSCEIVER RESET
100kHz
DAC CONTROL
100kHz CLK
TEMP SENSOR I2C
100kHz CLK
EEPROM I2C
100kHz_CLK
DC_COL (1:0)
DC_ROW (1:0)
CH (2:0)
WINDOW (8:0)
block ram data order:
ASIC CH SMPL
0 0 0-63
0 1 0-63
0 7
1 0 0-63
1 0 0-63
3 7
3 0 0-63 64-127
Commands:
GLOBAL_RESET
SET_MULTIPLEXER
READ_HOUSEKEEPING
DAC2DAC (set_DACs)
5FEEDBAC SET_FEEDBACK 1 or 0
AFEEDBAC READ_FEEDBACK
SOFT_TRIGGER
PEDESTAL_MODE on/off
START_WINDOW
END_WINDOW

Front-end Firmware Block Diagram



Resources (where to find more)

- Hardware:
  - IRS3B webpage:
    http://www.phys.hawaii.edu/~idlab/taskAndSchedule/ASIC/IRS3B/IRS3B_homepage.html
  - Board stack schematics:
    http://www.phys.hawaii.edu/~mza/PCB/iTOP/carriers/index.html
    http://www.phys.hawaii.edu/~mza/PCB/iTOP/index.html (Interconnect)
    http://www.phys.hawaii.edu/~mza/PCB/SCROD/index.html
- Firmware:
  - References link:
    http://www.phys.hawaii.edu/~idlab/taskAndSchedule/ASIC/Firmware/Firmware_homepage.html
  - Repositories: http://idlab-scrod.googlecode.com/svn/SCROD-boardstack/iTOP/IRS3B_CRT/
    https://code.google.com/p/idlab-general/source/browse/#svn%2Funiversal_eval%2FIRS3B_DC-stand-alone-firmware%2Fsrc
- Software:
  - Will talk about next time: https://www.phys.hawaii.edu/elog/
    https://www.phys.hawaii.edu/elog/mtc/152

Summary – Day 2

A lot more detailed information presented

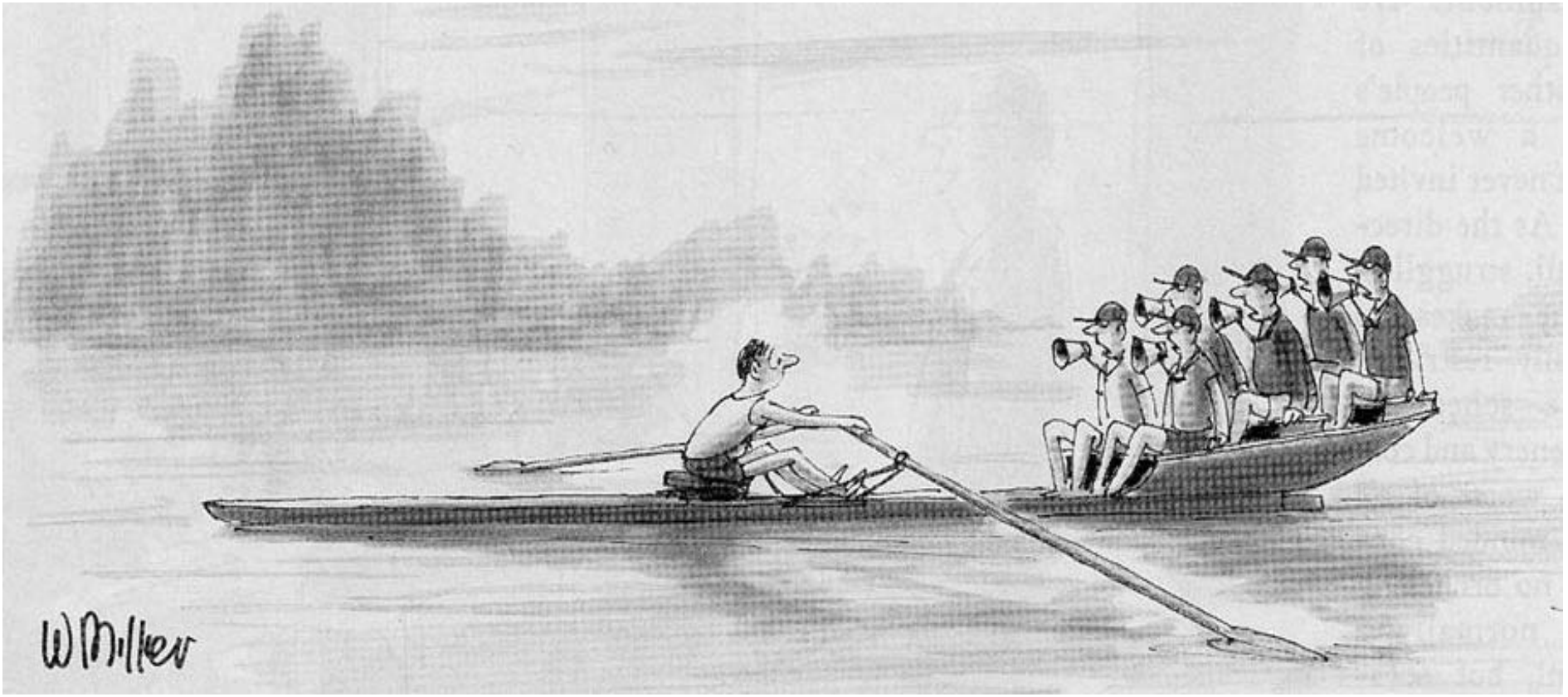
- **Please review and return with questions next time (if you don't, I will quiz you)**
- **Primary issues to be addressed for quality mTC data-taking:**
  - **Are register configurations/feedbacks being set properly ?**
  - **Diagnostic/meaningful DQM tools ?**
  - **Understanding what is being done ?**
- **All of these concepts are straightforward, though many to be assimilated all at once (rounds 2 & 3)**
- **Typically 3+ times through needed to 'get it'**

Thoughts on Day 3

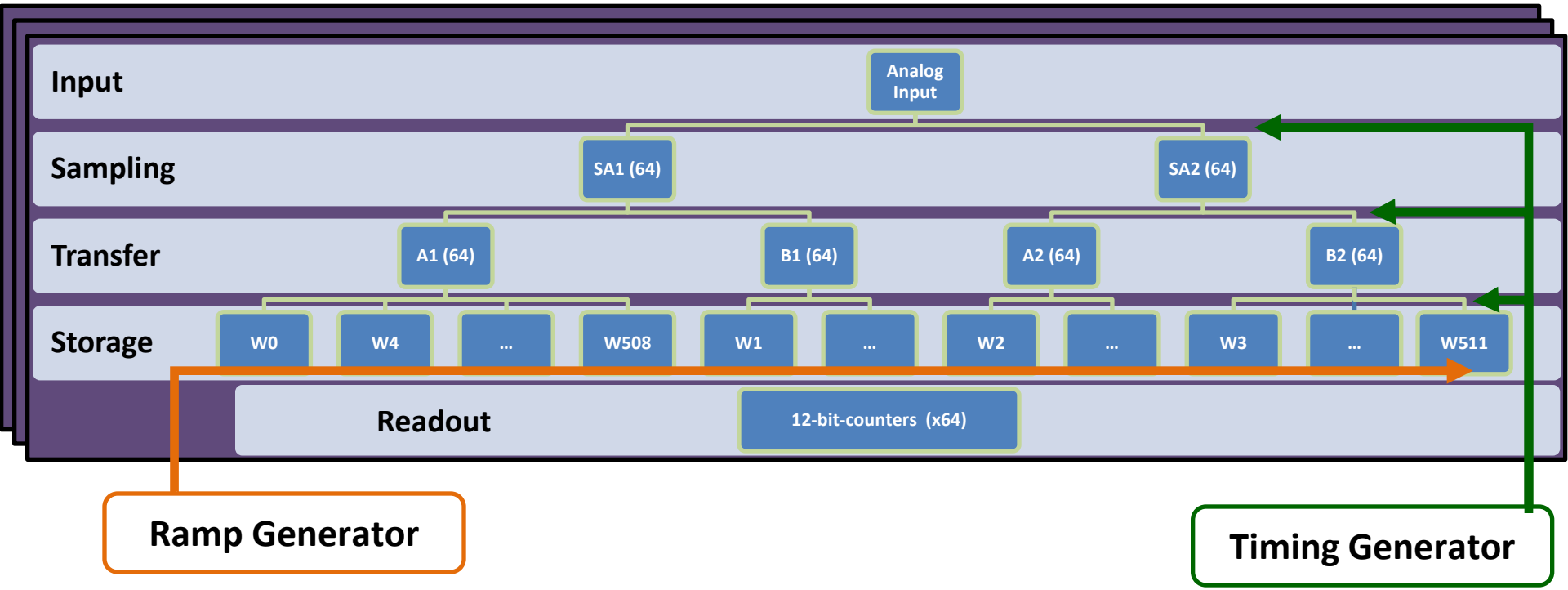
Software, Calibration and Advanced Topics

- **Key control issues:**
  - **Acquisition and Readout State Machines**
  - **Wilkinson counter and timebase feedback loops**
  - **Digitization and readout**
- **Key operational issues:**
  - **Parameter initialization**
  - **Trigger threshold and coincidence level setting**
  - **Buffer window management**

Back-up slides



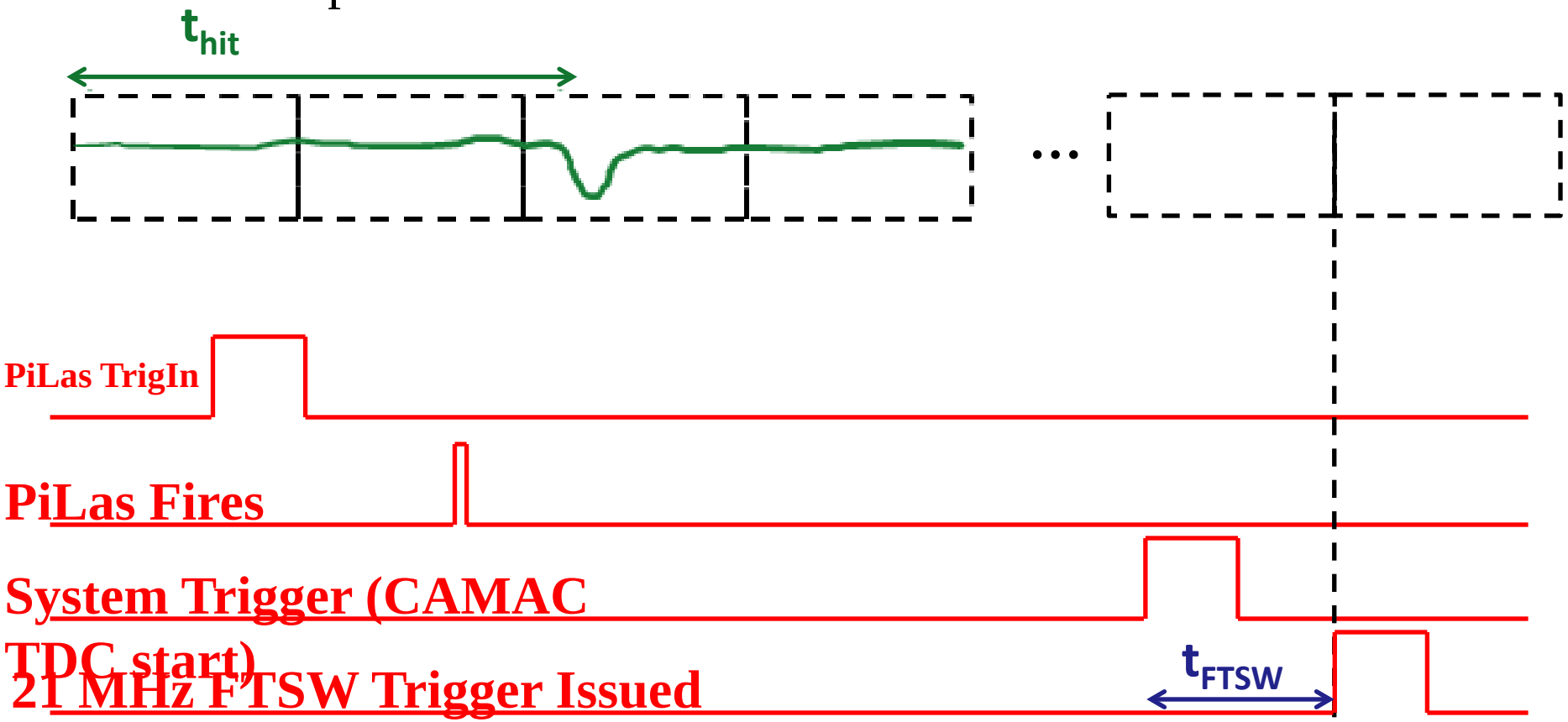
Simplified IRS3B Block Diagram



- Per channel:
  - Single input line
  - 128 sampling cells/capacitors
  - 256 transfer cells/capacitors
  - 32,768 storage cells/capacitors
  - 64 counters used to digitize 64-samples in parallel
- Common to all channels:
  - Timing generator
  - Ramp generator

Example window buffer mgmt

- Laser fired randomly with respect to FTSW clock…
  - …but at a fixed time relative to the global trigger.
  - Example 1:



Smaller t_{hit} ➔ larger t_{FTSW}