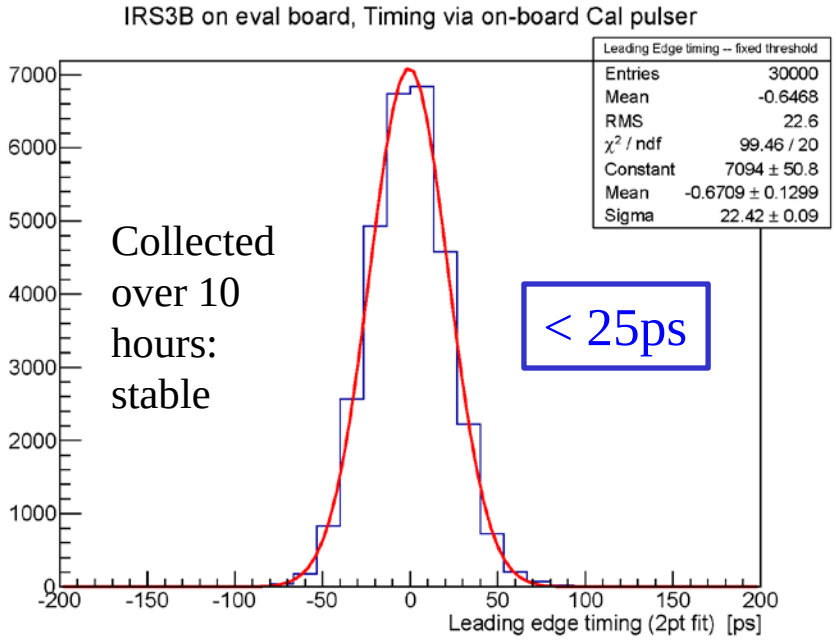
Understanding IRS3B, board-stack and mTC operation/calibration



Gary S. Varner

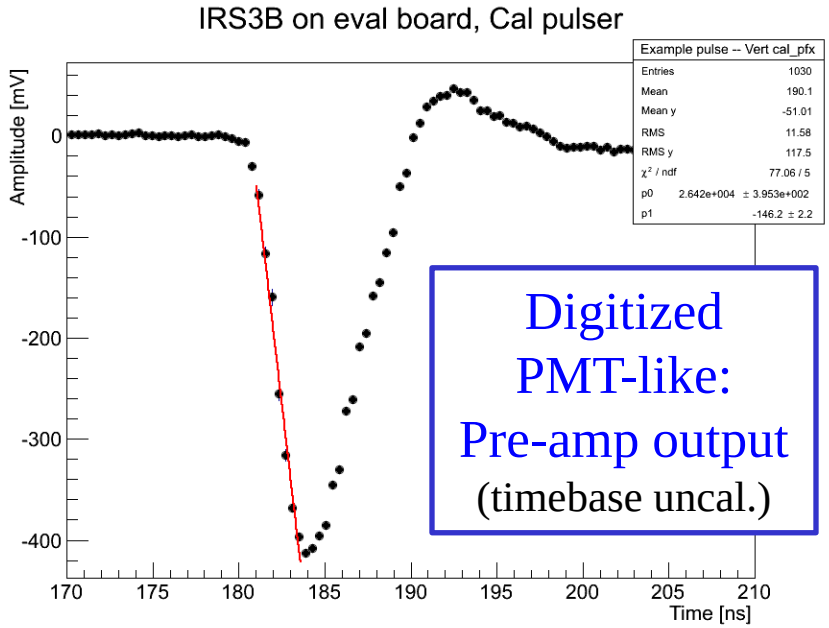
10 JUL 2014

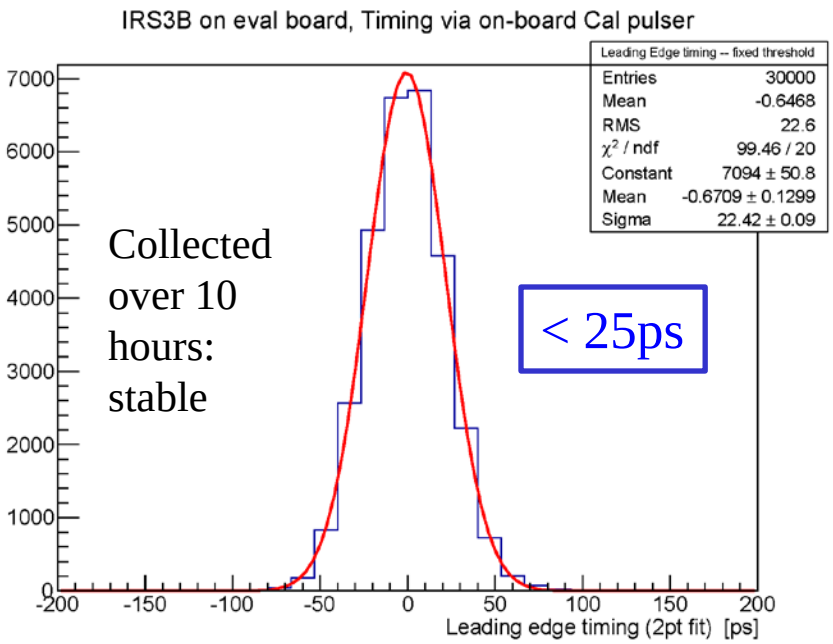
mTC Training Session #5

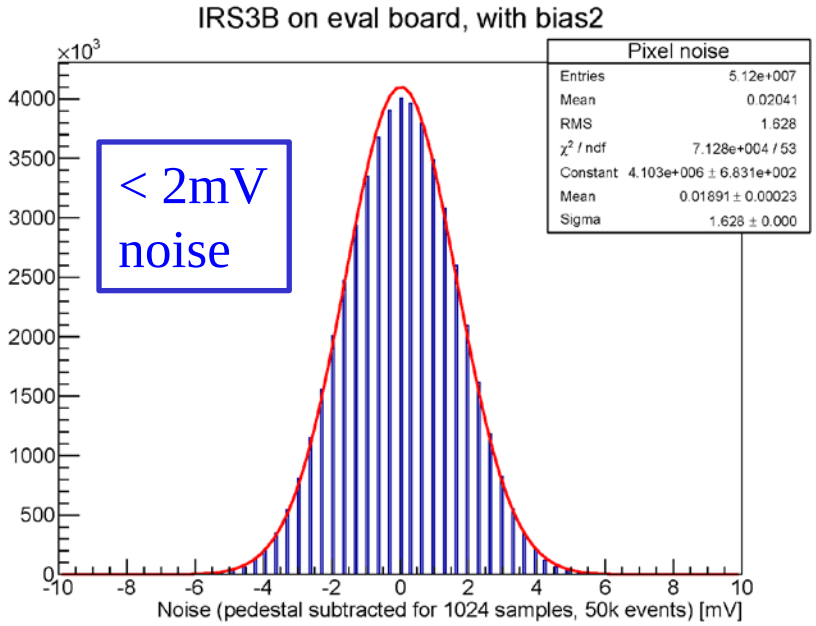
Roadmap

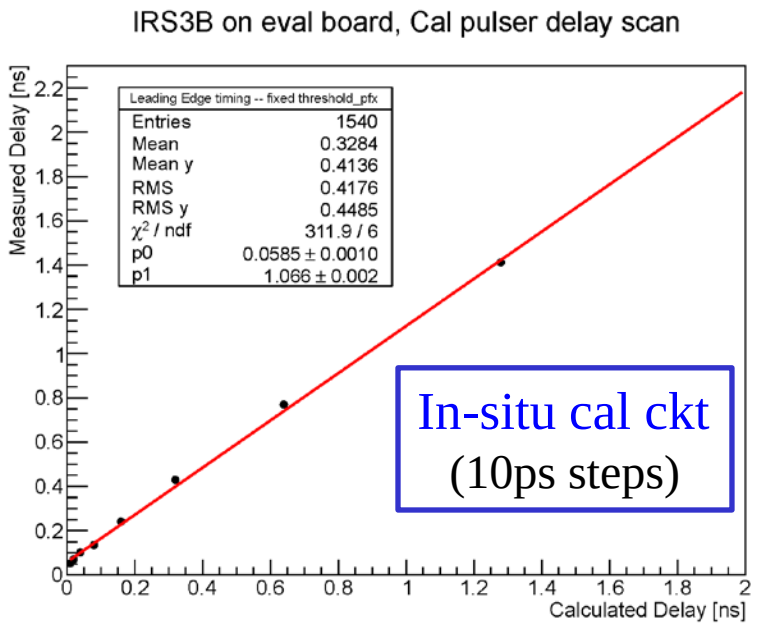
- mTC Readout
  - Currently at about Phase 1.5
  - You can get us to Phase 2.5
- Specifically
  - Operators need to understand Hardware/Firmware/Software
  - **Develop real-time Data Quality Monitoring**
- What I hope to convey:
  1. Details of the hardware: ASIC + boardstack
  2. Firmware and Configuration/Operating parameters
  3. Understand how to read and comprehend documentation and ask meaningful questions (“it doesn’t work” notably not amongst them)

Reminder: IRS3B not so bad



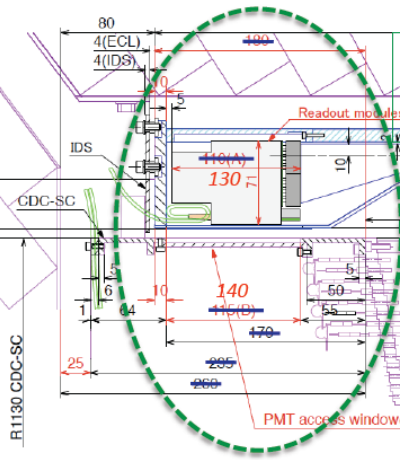


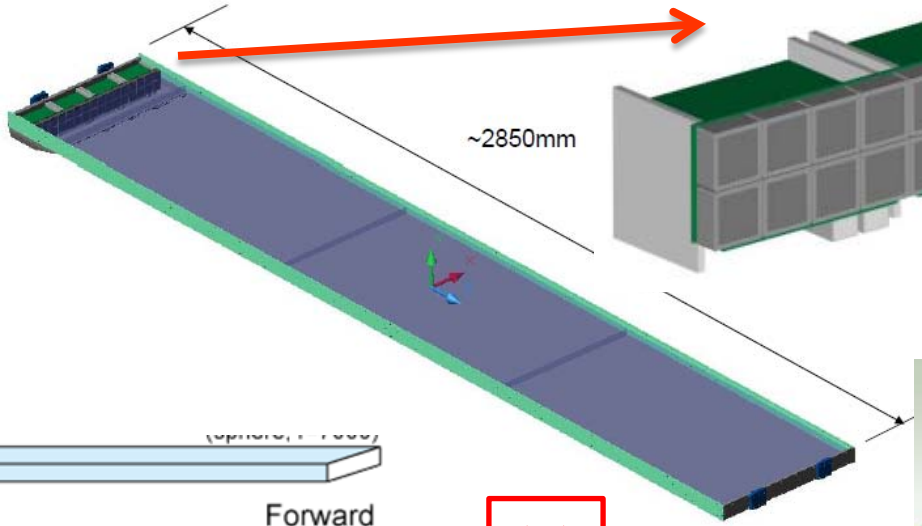




Belle II iTOP Counter

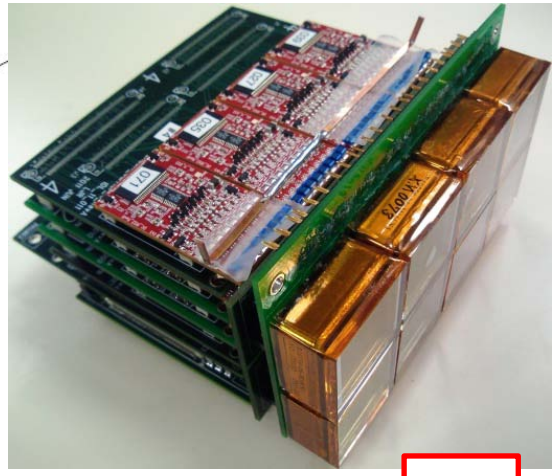
- 3 key elements: quartz radiator, micro-channel plate PMT array, integrated readout electronics



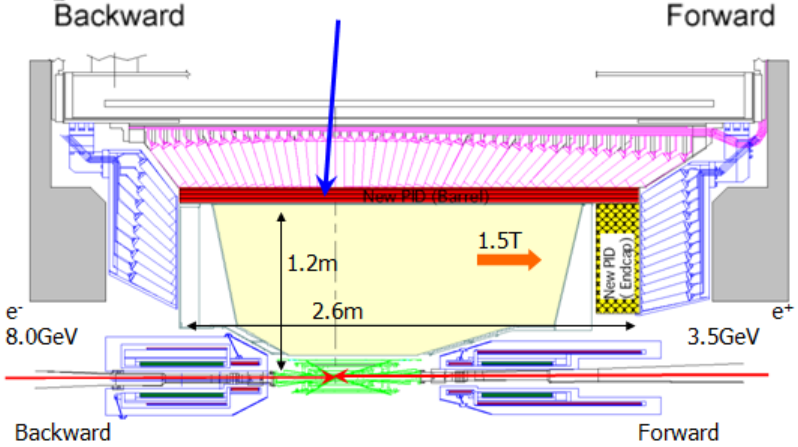


(1)

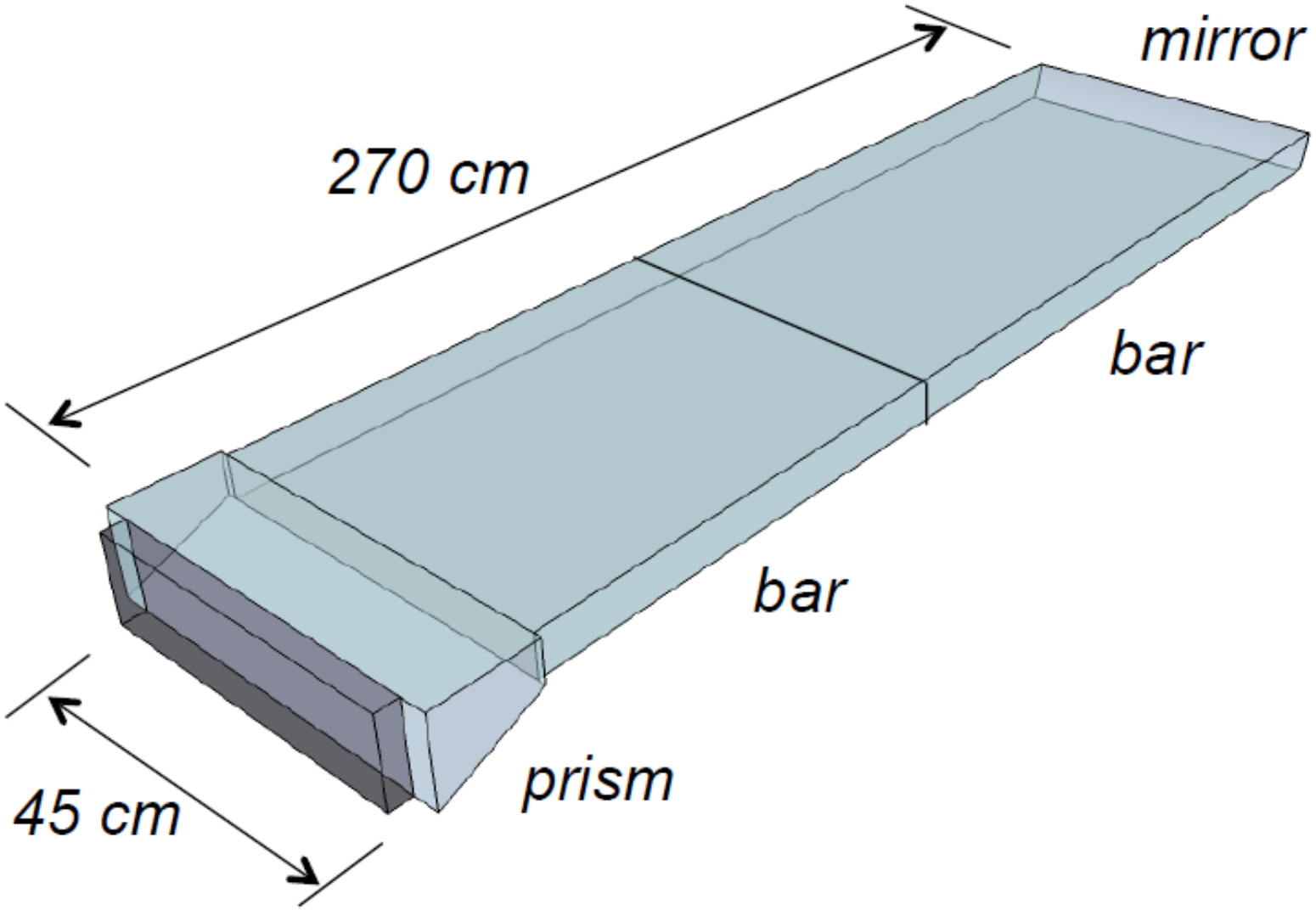
(2)



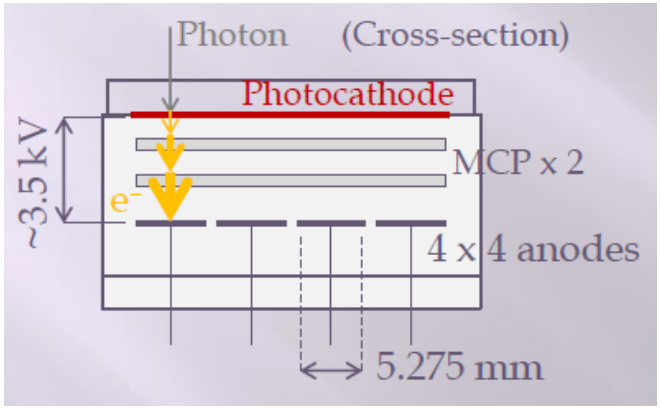
(3)

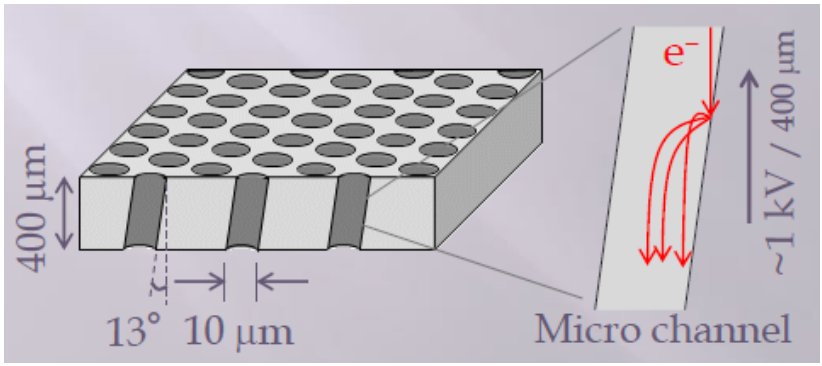


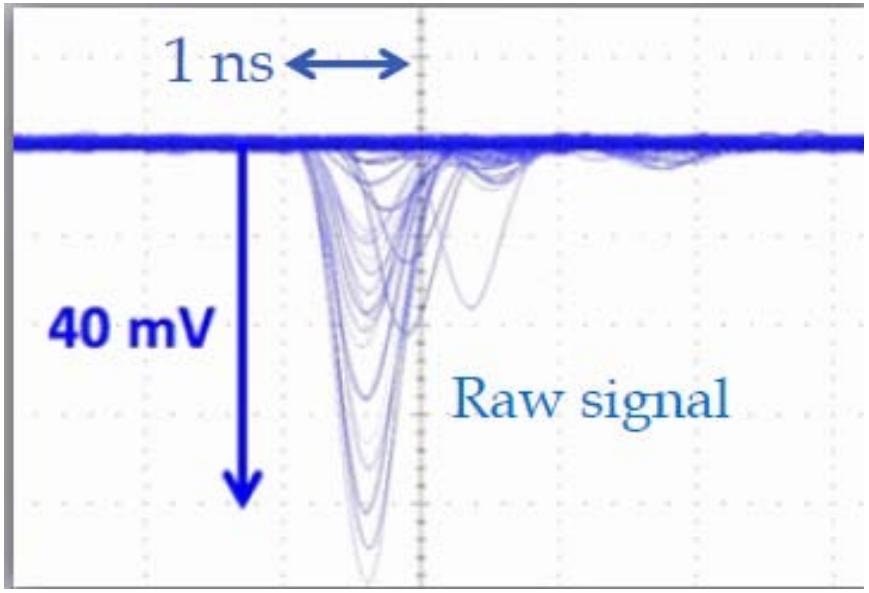
1) Quartz Radiator, Optics, Coupling

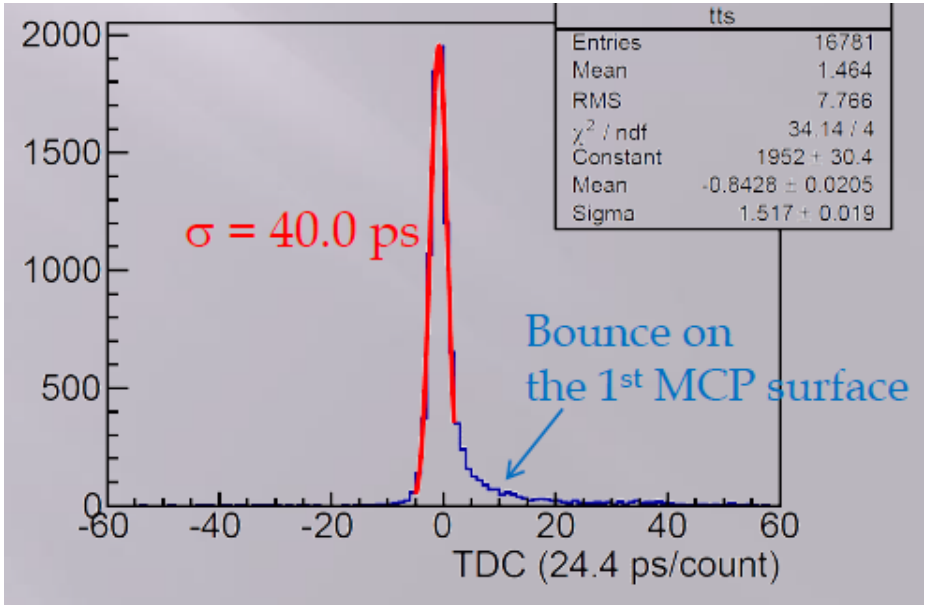


2) Micro-Channel Plate PMT (HPK SL-10)







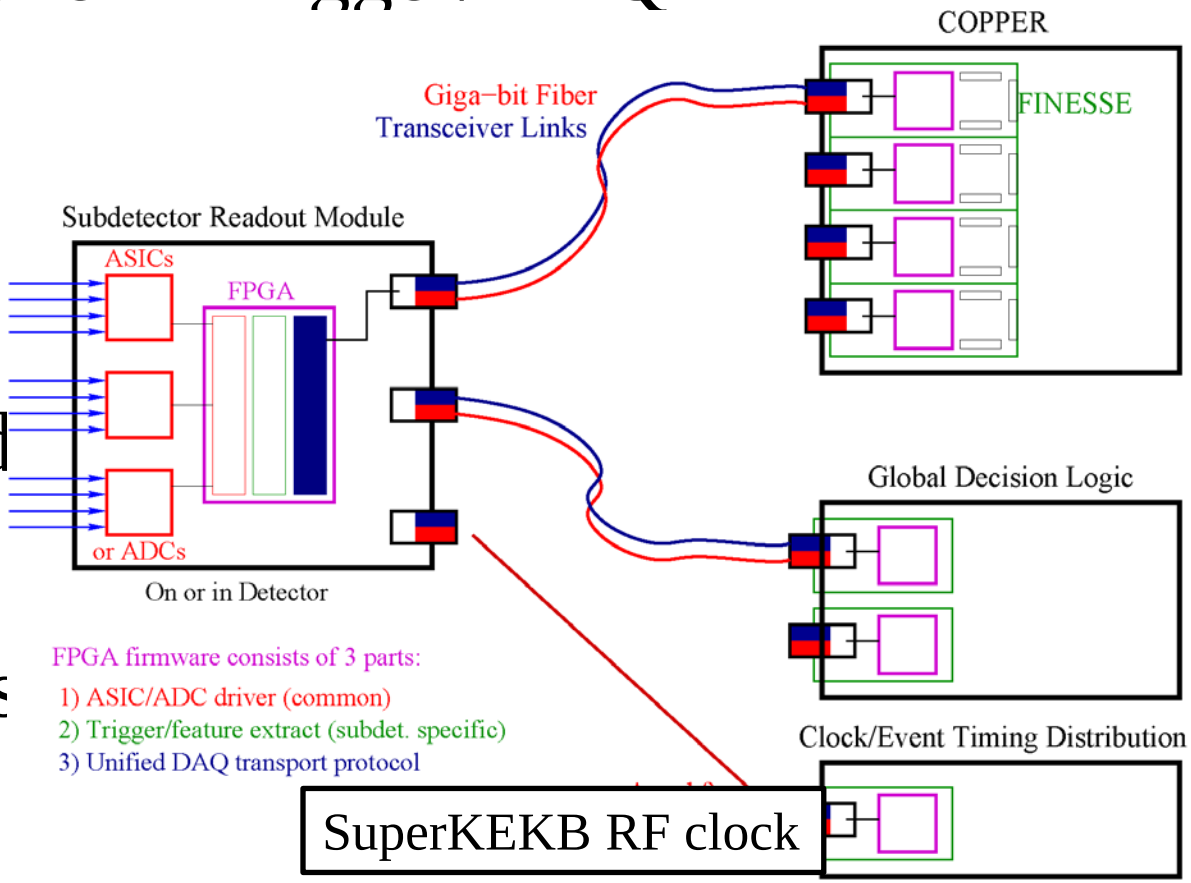


Works in 1.5T B-field

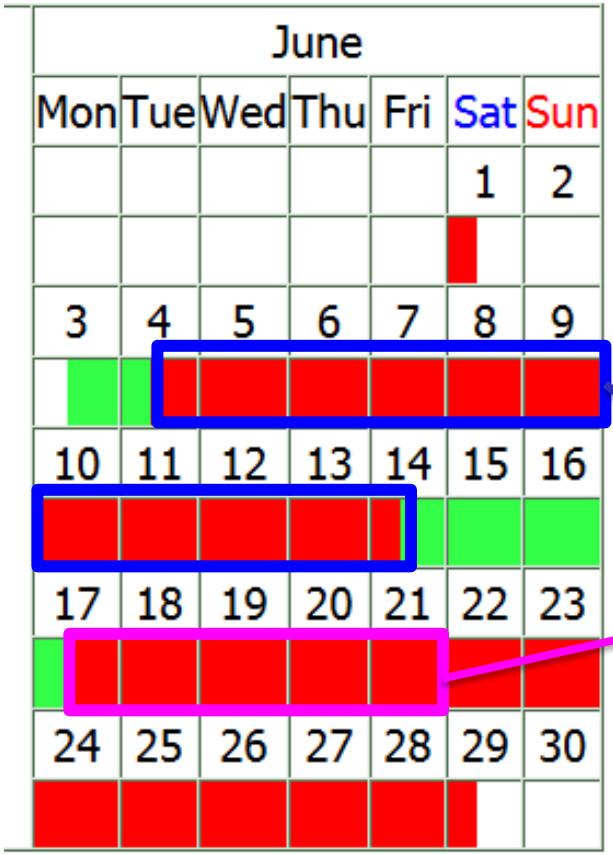
Peak Q.E. ~28% (24% min)

3) Integrated Readout Electronics

- Operate within Belle-II Trigger/DAQ environment
- >= 30kHz L1 trig
- Gbps fiber Tx/Rx
- COPPER backend
- Timing trigger
- iTOP: 8k channels
- 16 iTOP modules
- 4x 128-channel SRM/iTOP module (64x total)



SPring-8 2013 Run Schedule

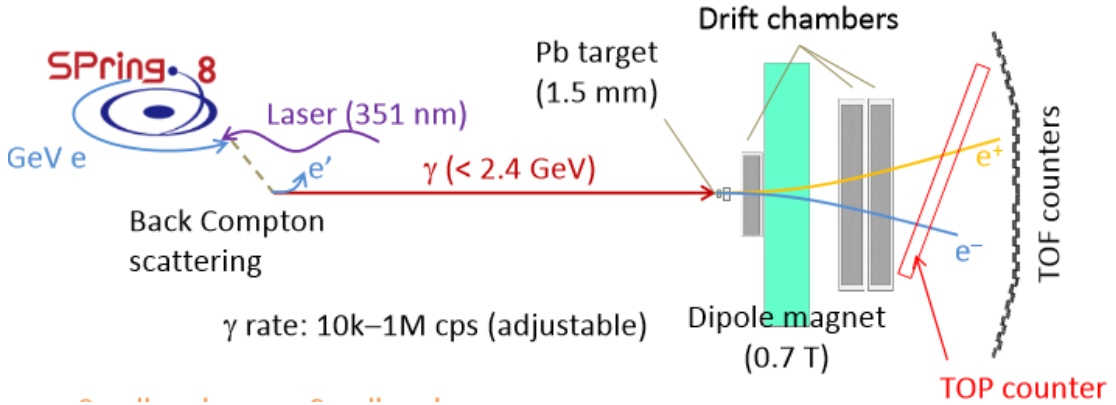


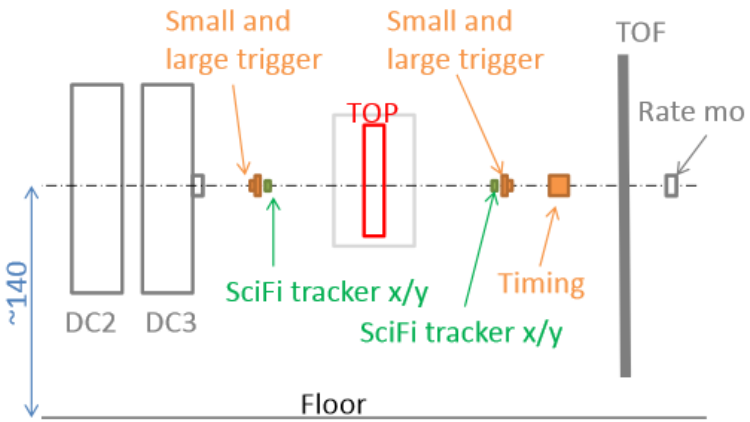
Beam test w/ LEPS detector:

Full detector (final optics)

IRS3B Readout
"Vertical slice" DAQ
(FTSW+FINESSE/COPPER)

1x4 CFD Readout VME-based Caen TDCs

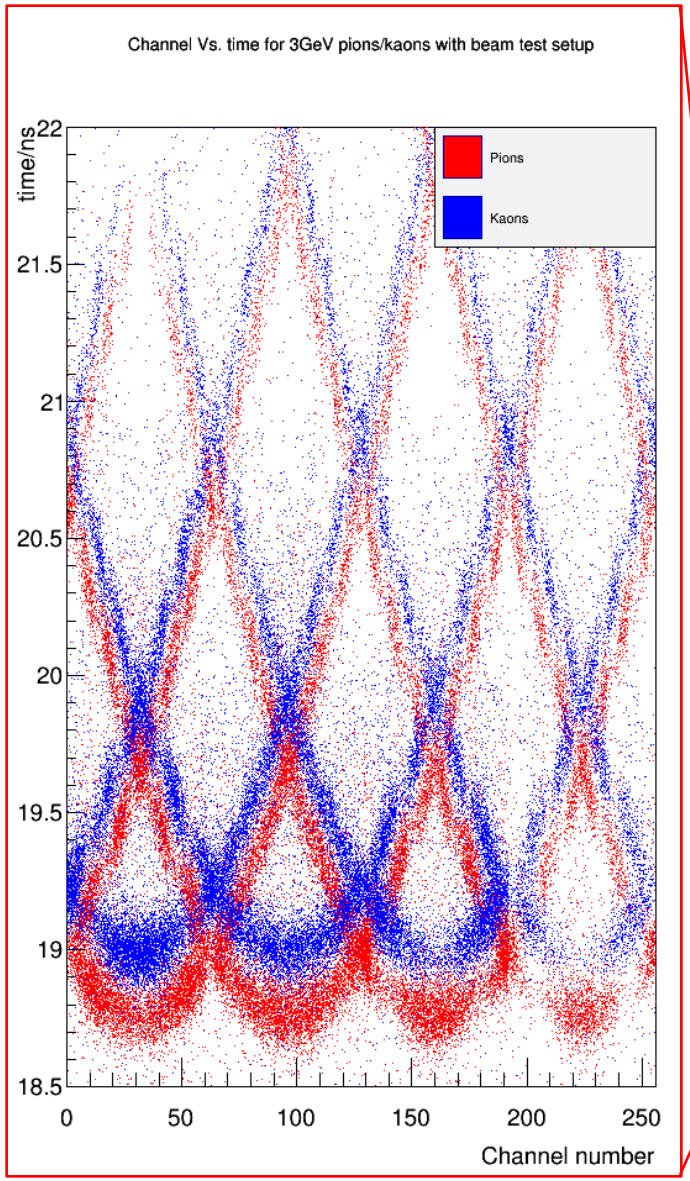


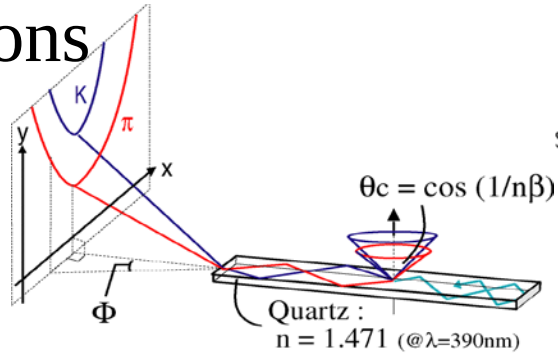


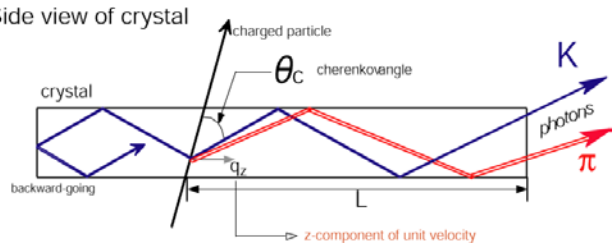
Event rate ~ 5-10Hz
2x polar angles;
1x off centerline (x=20)

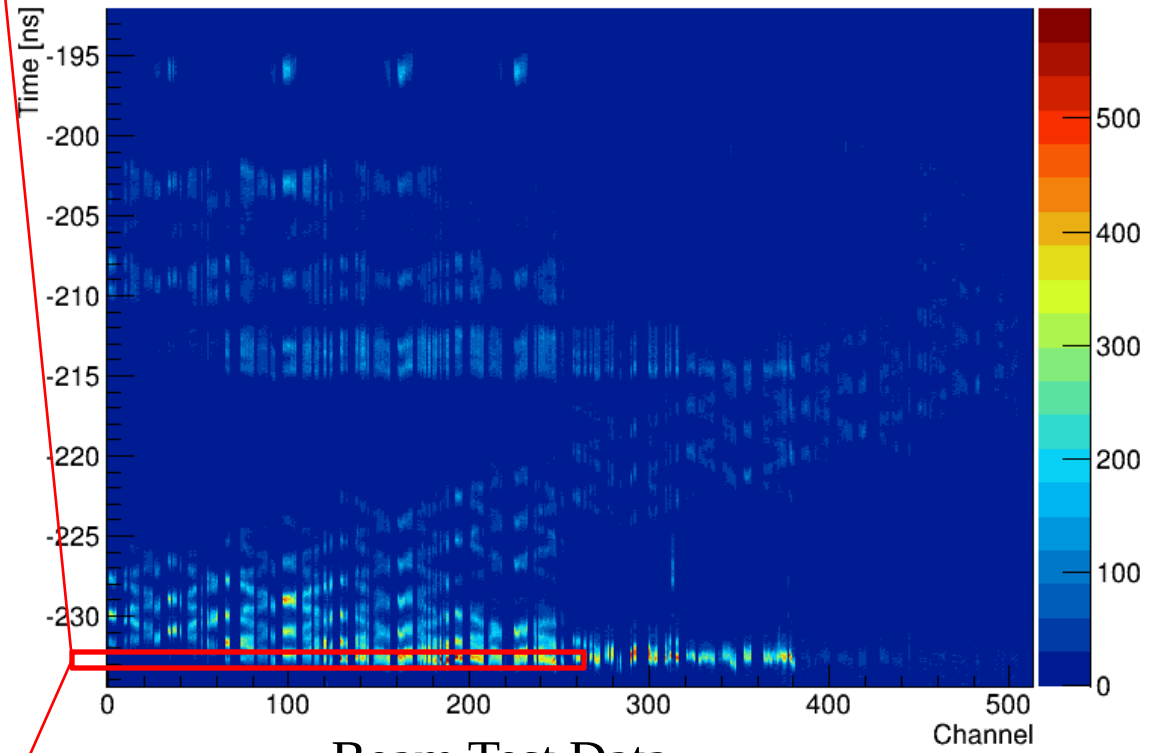
iTOP relativistic velocity separation

- Space-time correlations





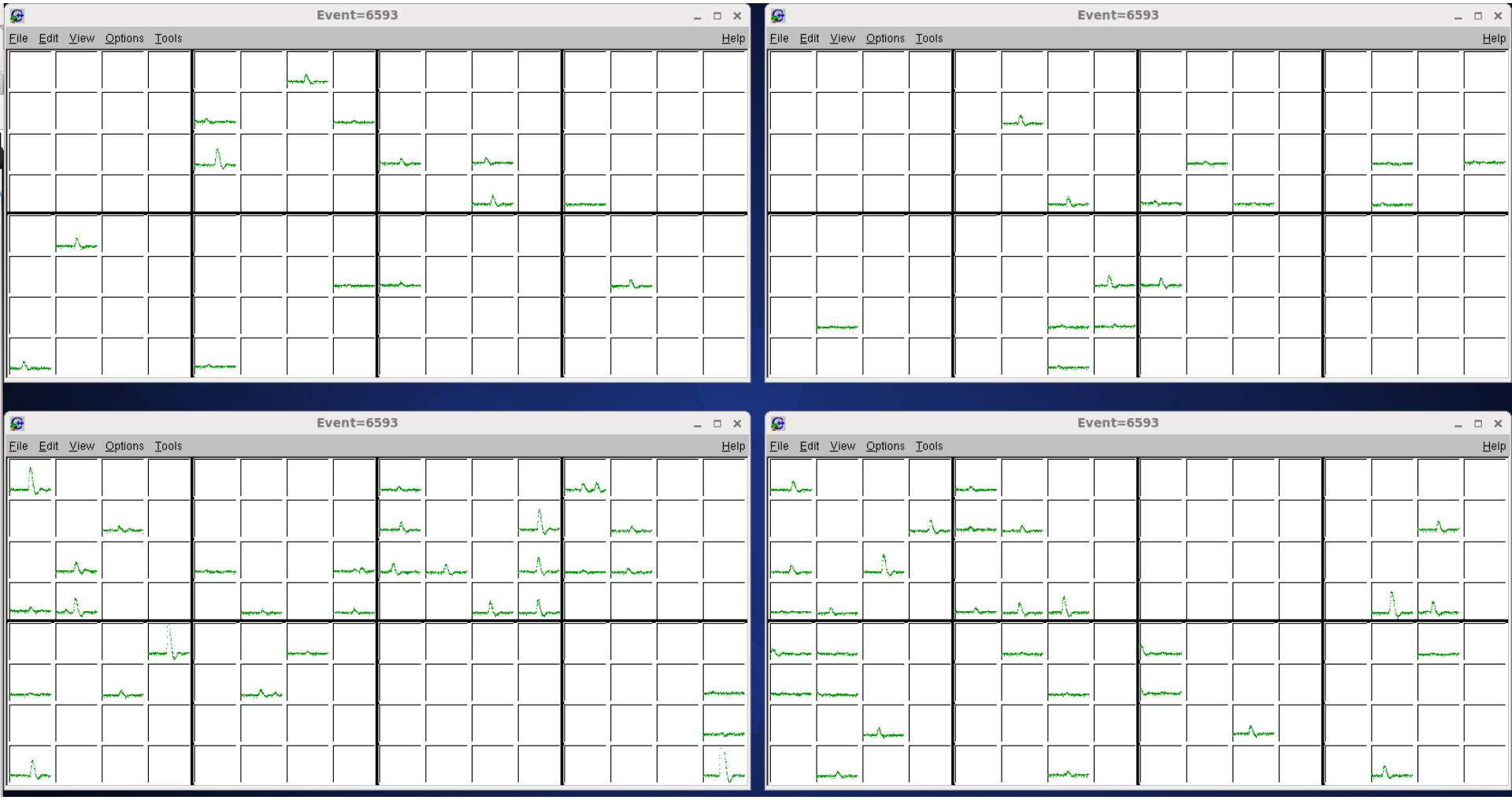




Beam Test Data

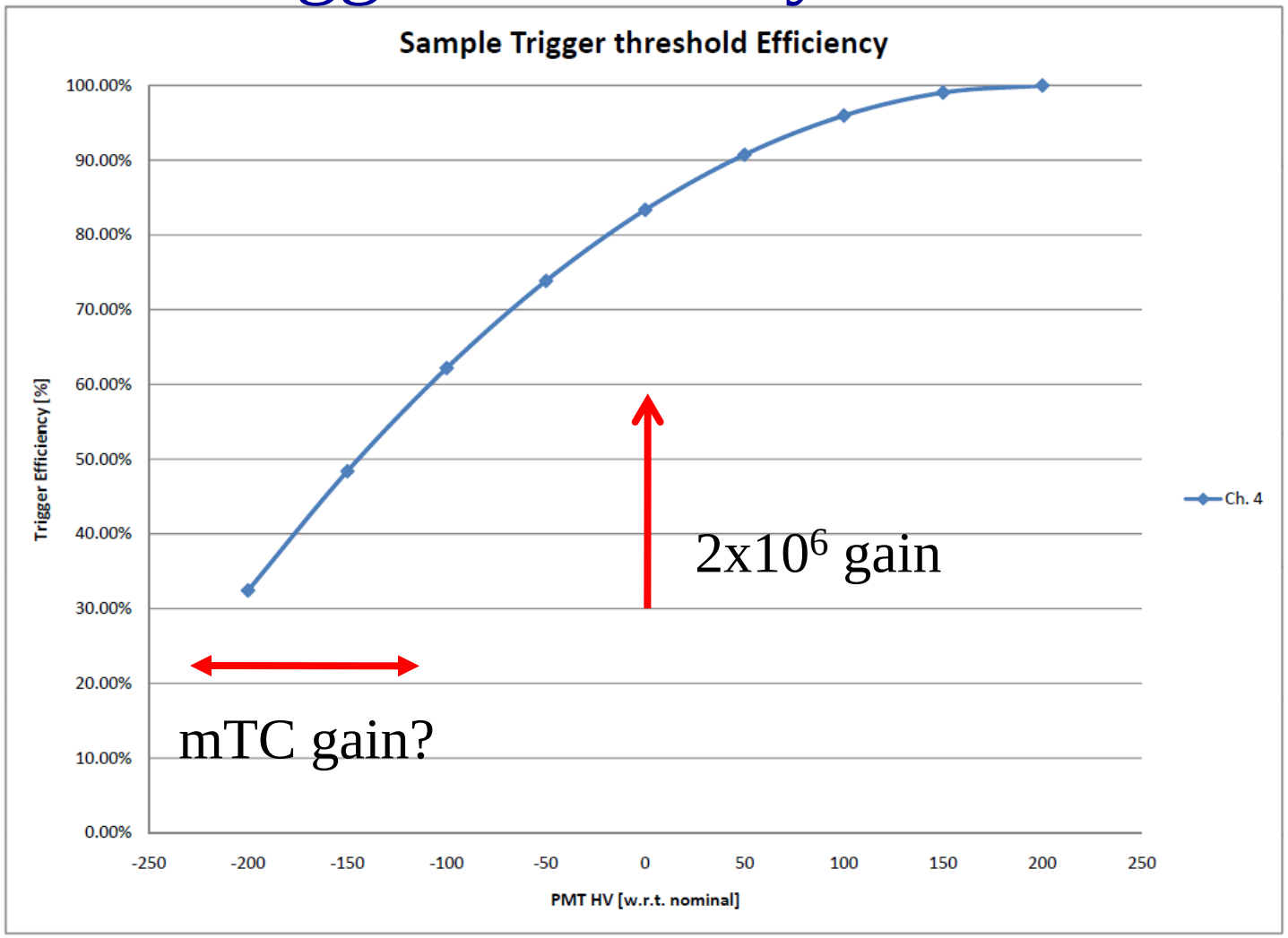
These are cumulative distributions

Typical LEPS Event



About 80% efficient, but running at very high gain!

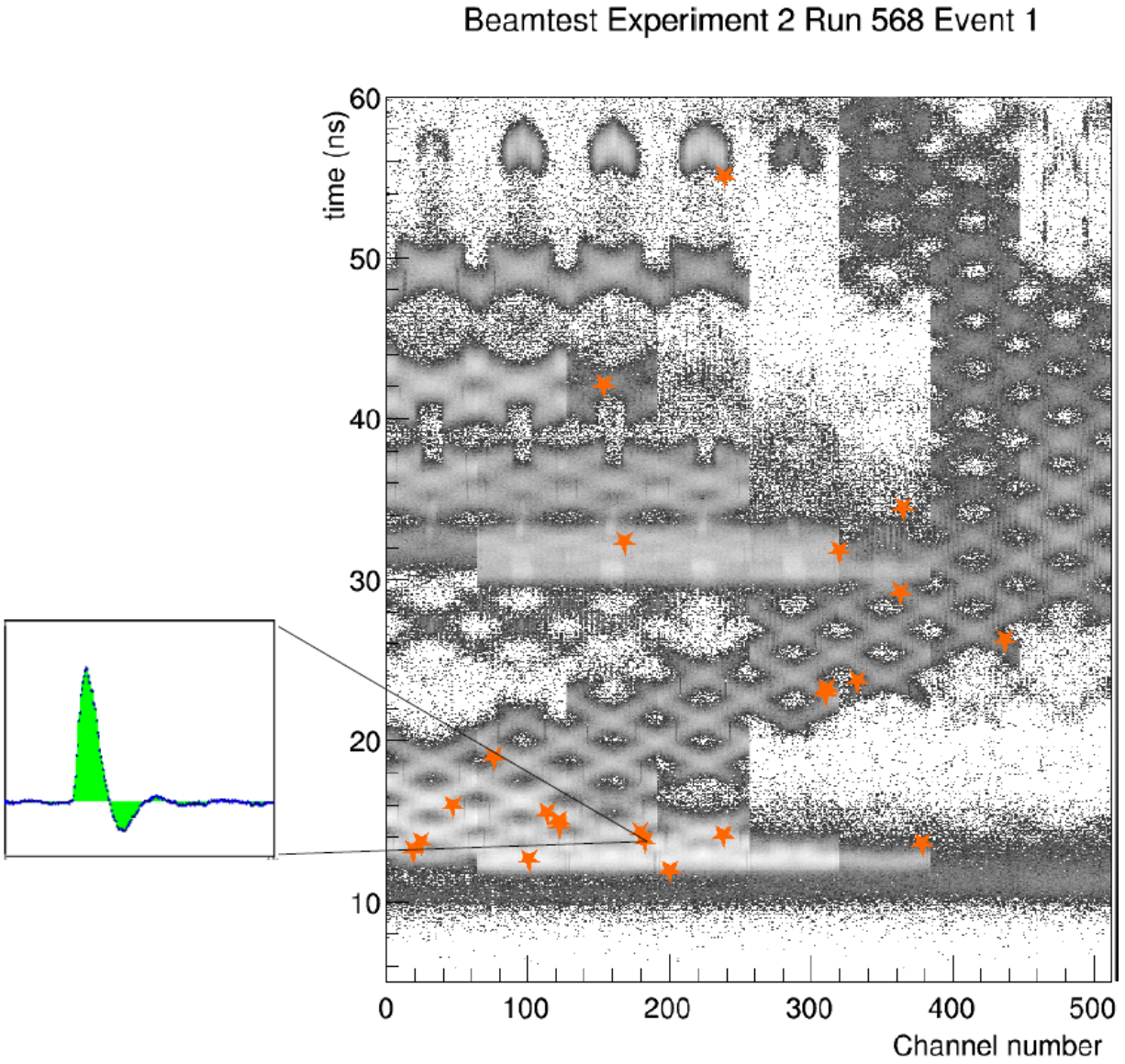
Trigger Efficiency estimate



This is why I am very concerned – same electronics

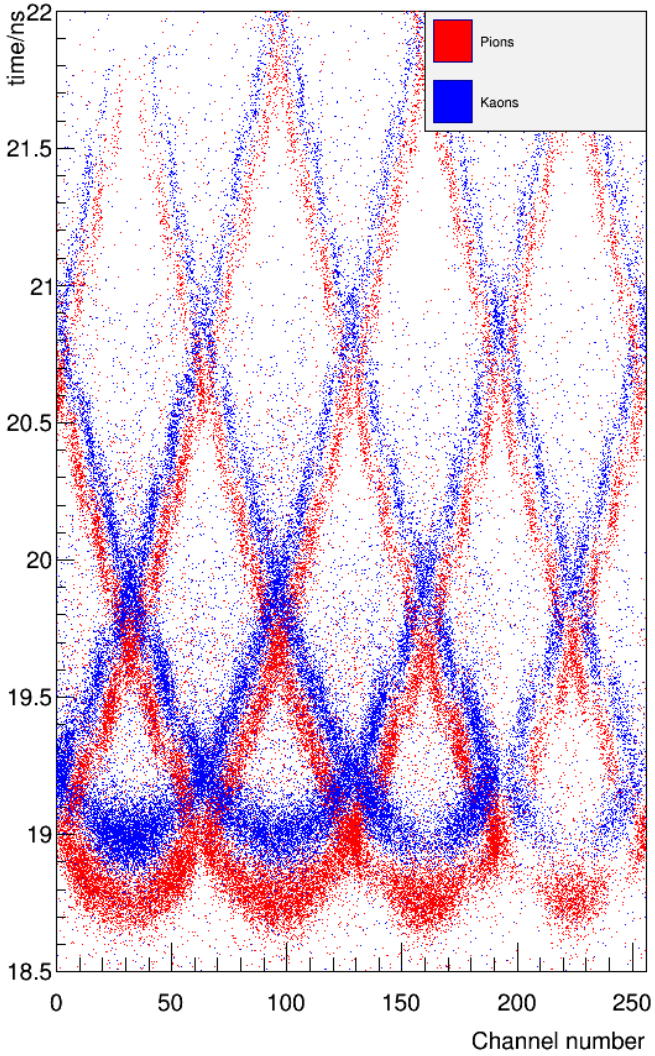
For each event

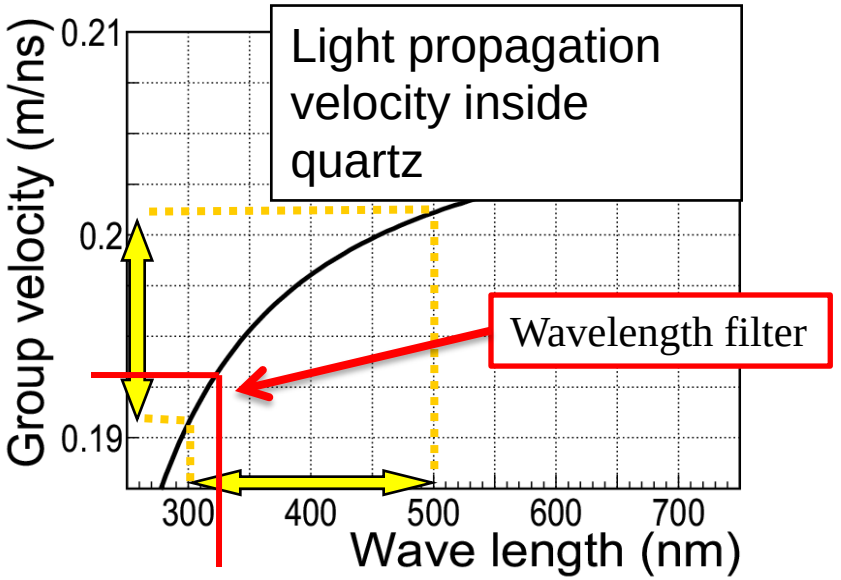
- Test most probable distribution



Temporal broadening

- Limited gain from improved time resolution
- Coarser spatial resolution integrates more of partial ring





- Due to wavelength spread of detected photons

→ propagation time dispersion

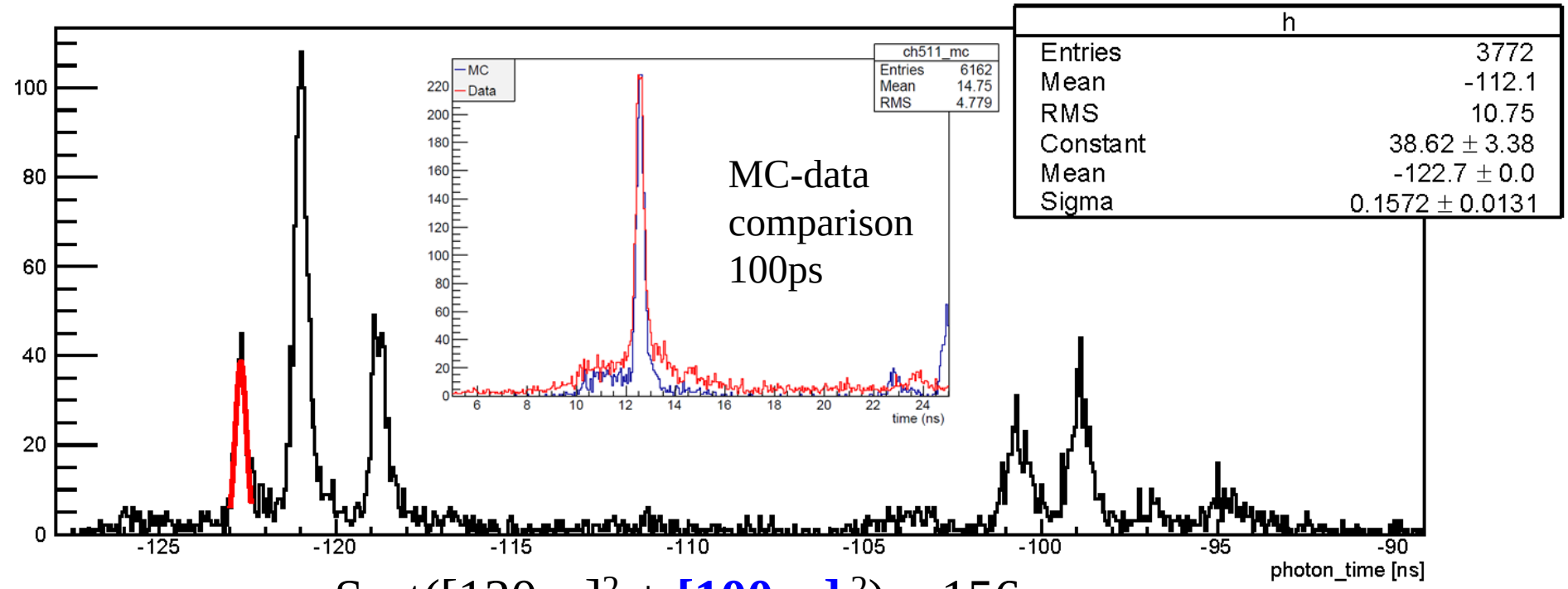
- Longer propagation length

→ Improves projected ring image difference

But broadens time distribution

Measured Narrower Peaks Consistent with MC resolution + 100ps smearing

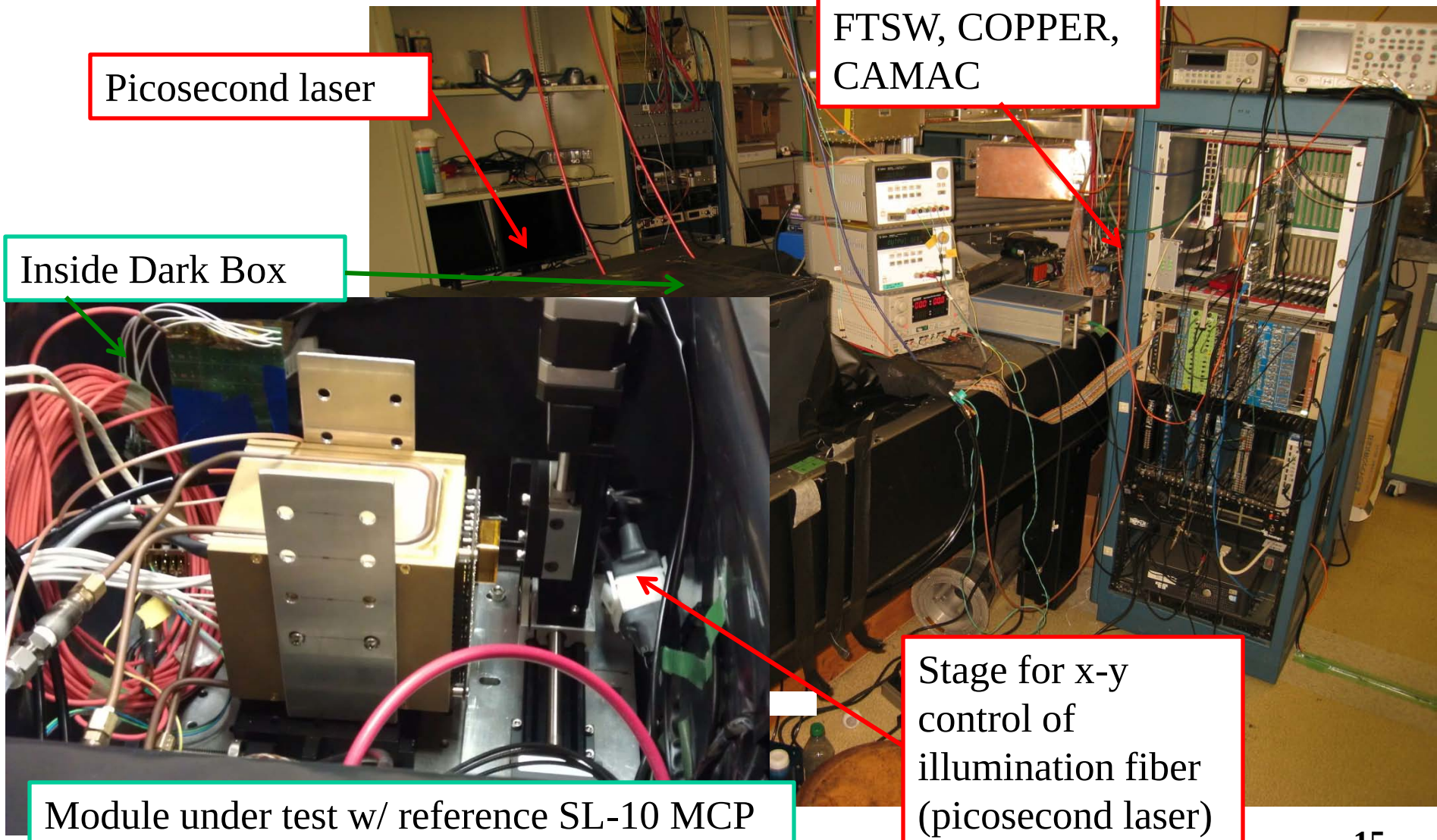
- For ADC>100 and using the “120ps” width determined from GEANT4



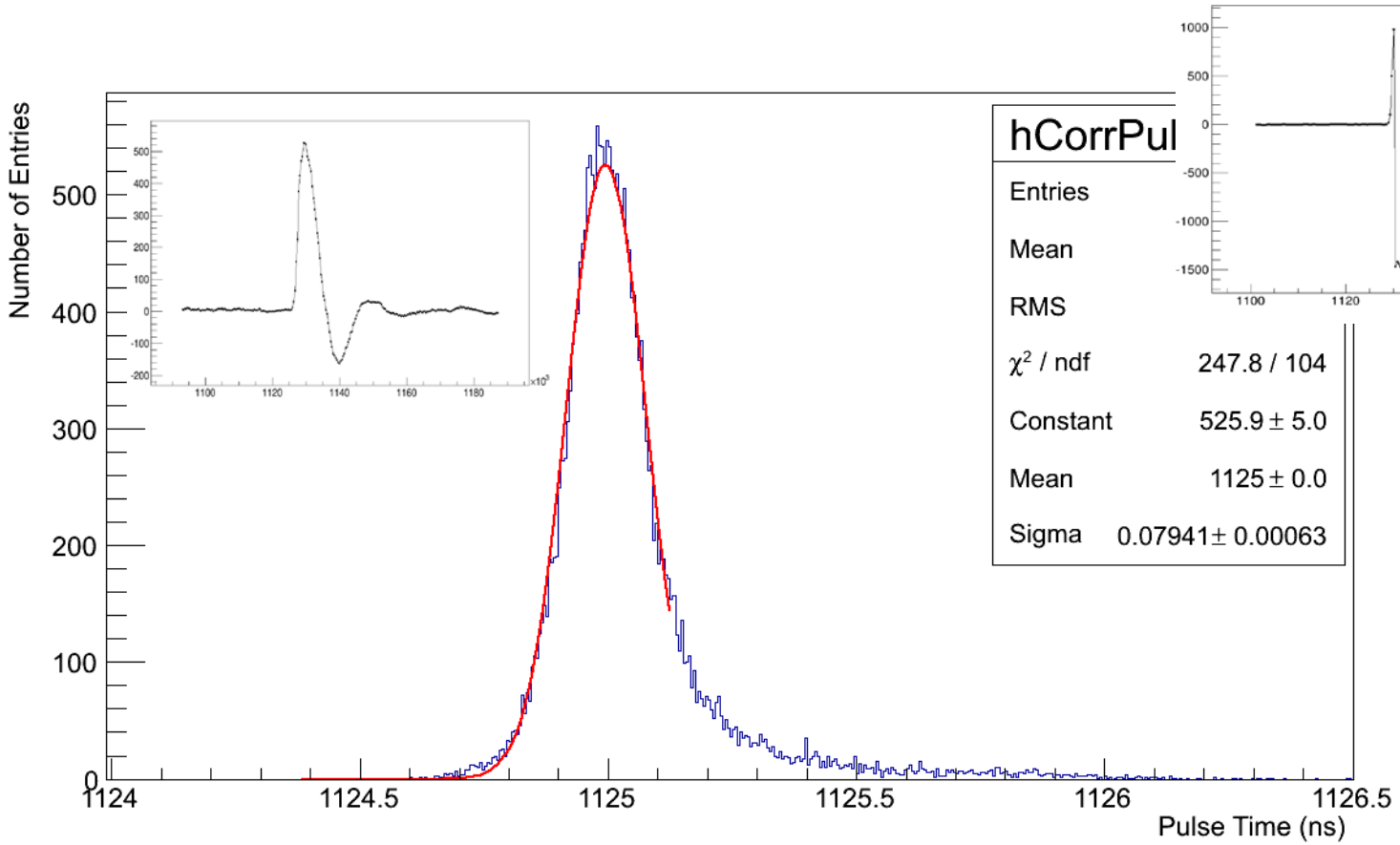
Sqrt([120ps]^2 + **[100ps]** ^{2}) ~ 156 ps

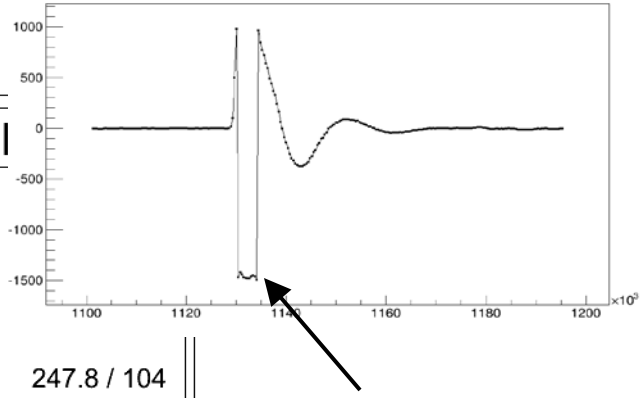
Measurement contribution

Insufficient time/laser scanning resources before LEPS beamtest – subsequent testing in Hawaii



Example single photon* timing, no ADC cuts, no modifications from LEPS configuration



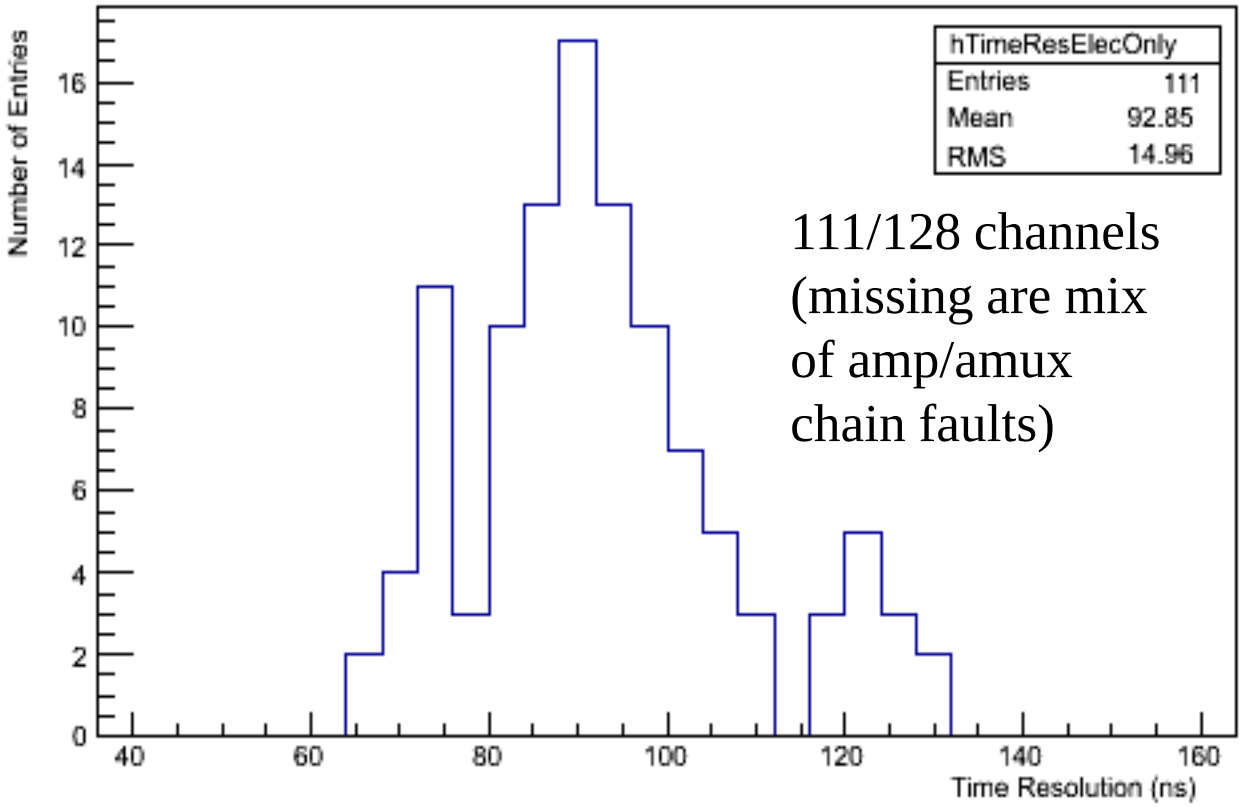


Developed "Time over Threshold" technique to treat these – actually give better timing due to good leading edge

~97% analysis efficiency (3% window "wrap around" cut [recoverable] – FTSW artifact)

* <= 5% occupancy

Board Stack #37 single photon* timing, no ADC cuts, no mods from LEPS configuration**



111/128 channels (missing are mix of amp/amux chain faults)

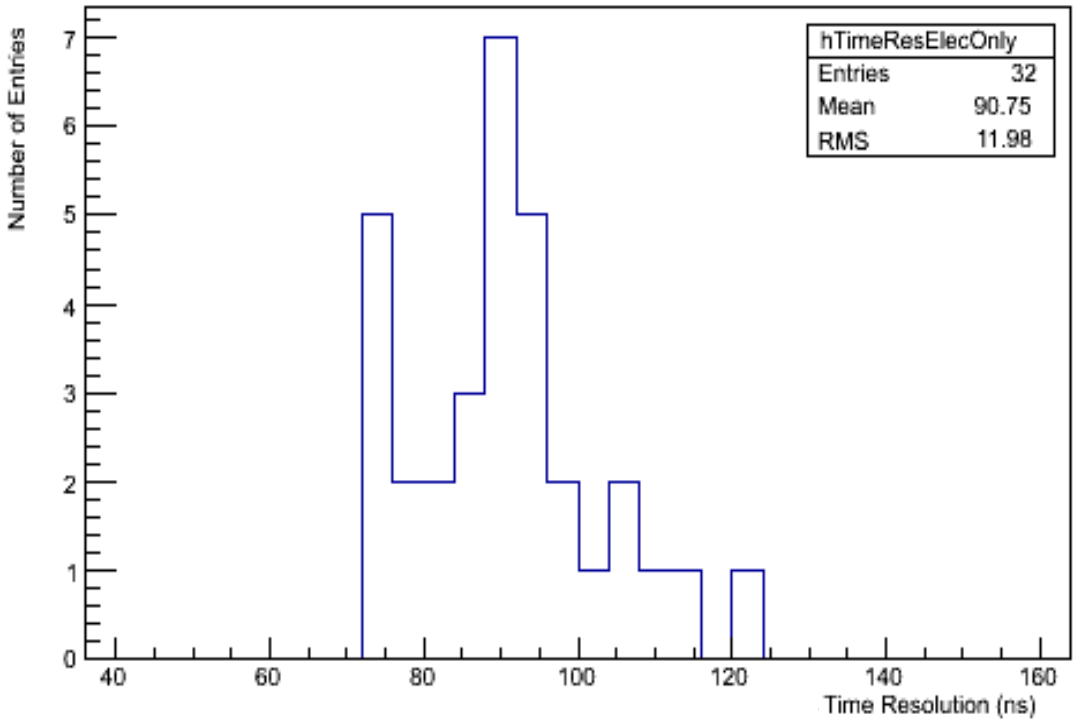
~25ps CAMAC contribution removed (in quadrature, not relevant for Belle II)

93 +/- 16 ps [a couple bad ASICs dominate high-end outliers]

* <= 5% occupancy

** most channels reworkable, didn't have time

Test system @ LEPS had 4 modules

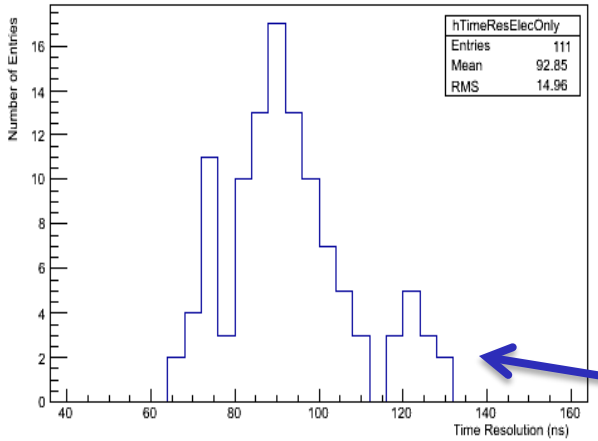


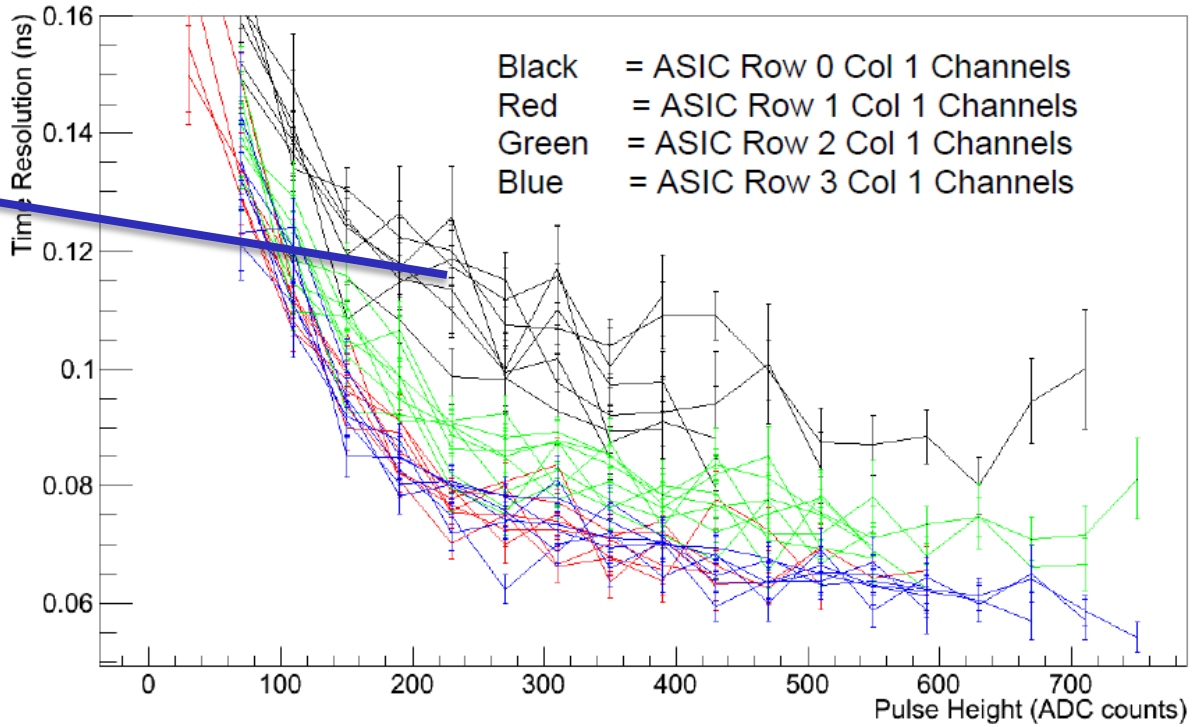
In progress, reporting 32/64 ASICs (2 of 4 modules)

Same conditions, 1x channel (Ch. 6) per ASIC

91 +/- 12 ps [bad ASICs only get to vote once, Ch. 6 not worst]

What limits resolution? Why large scatter?





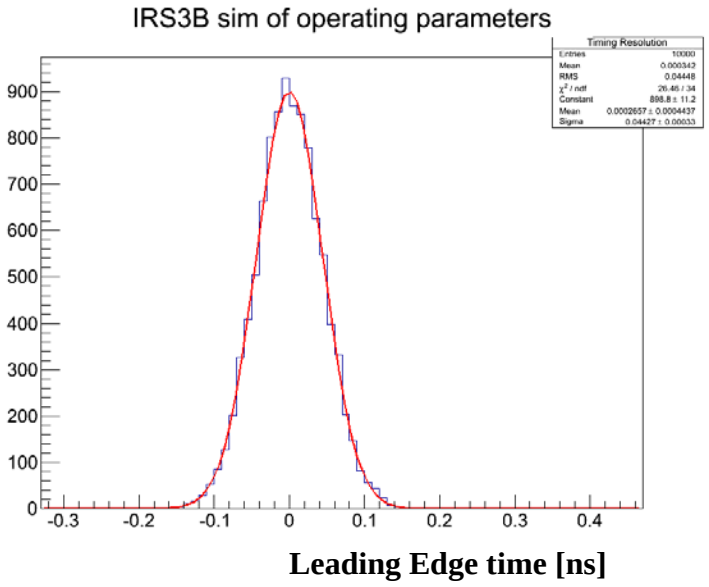
- **Amplitude dependence similar**
- **Channels on same ASIC have similar limiting resolution**

Understanding Expectations: IRS3B "toy" Monte Carlo

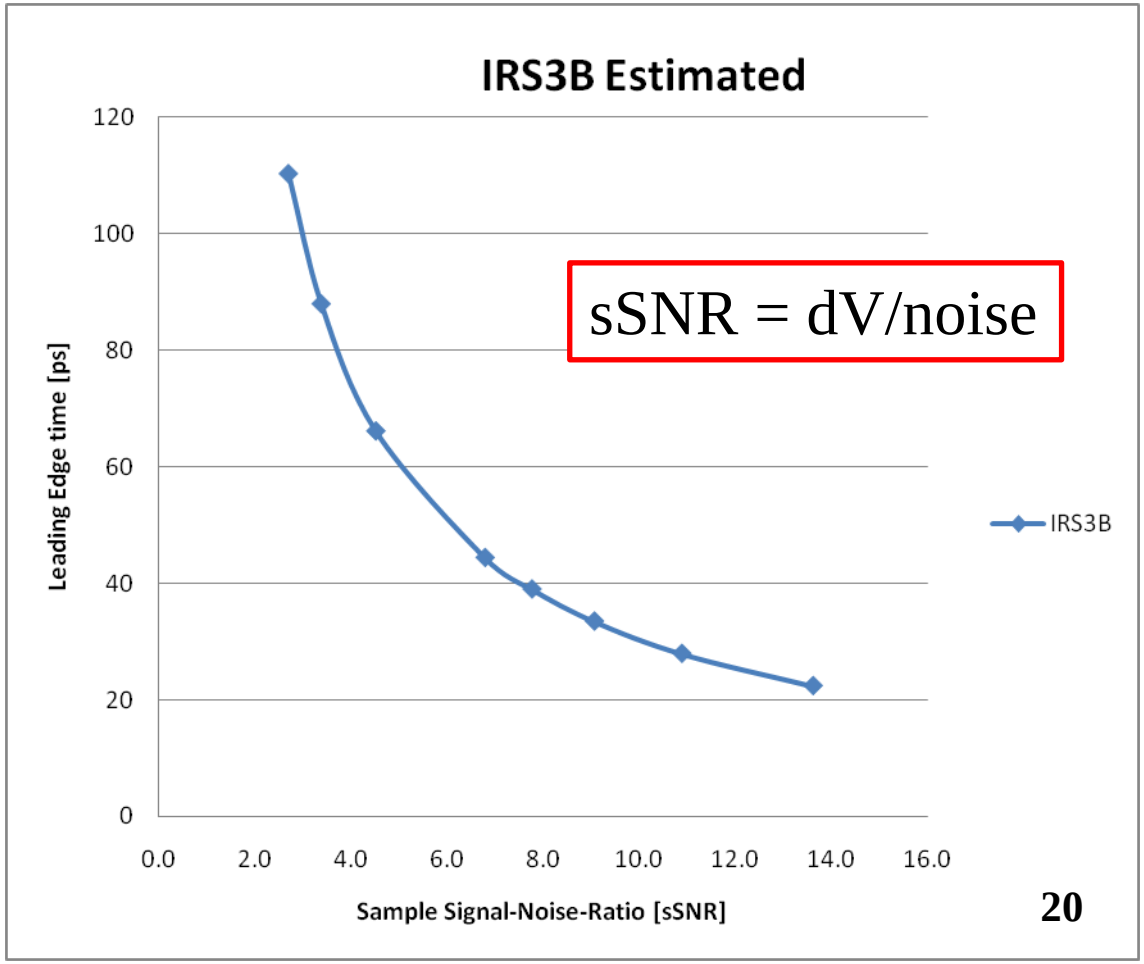
Vpeak	**100 ADC**
Risetime	**2.7 ns**
Sampling rate	**2.72 Gsa/s**
nom dT	**0.368 ns**
nom dV	**13.617 ADC/sample**

40% CFD ratio:

Applied between 2 points on leading edge that bracket this transition



~44ps for 100mV peak, 2mV noise



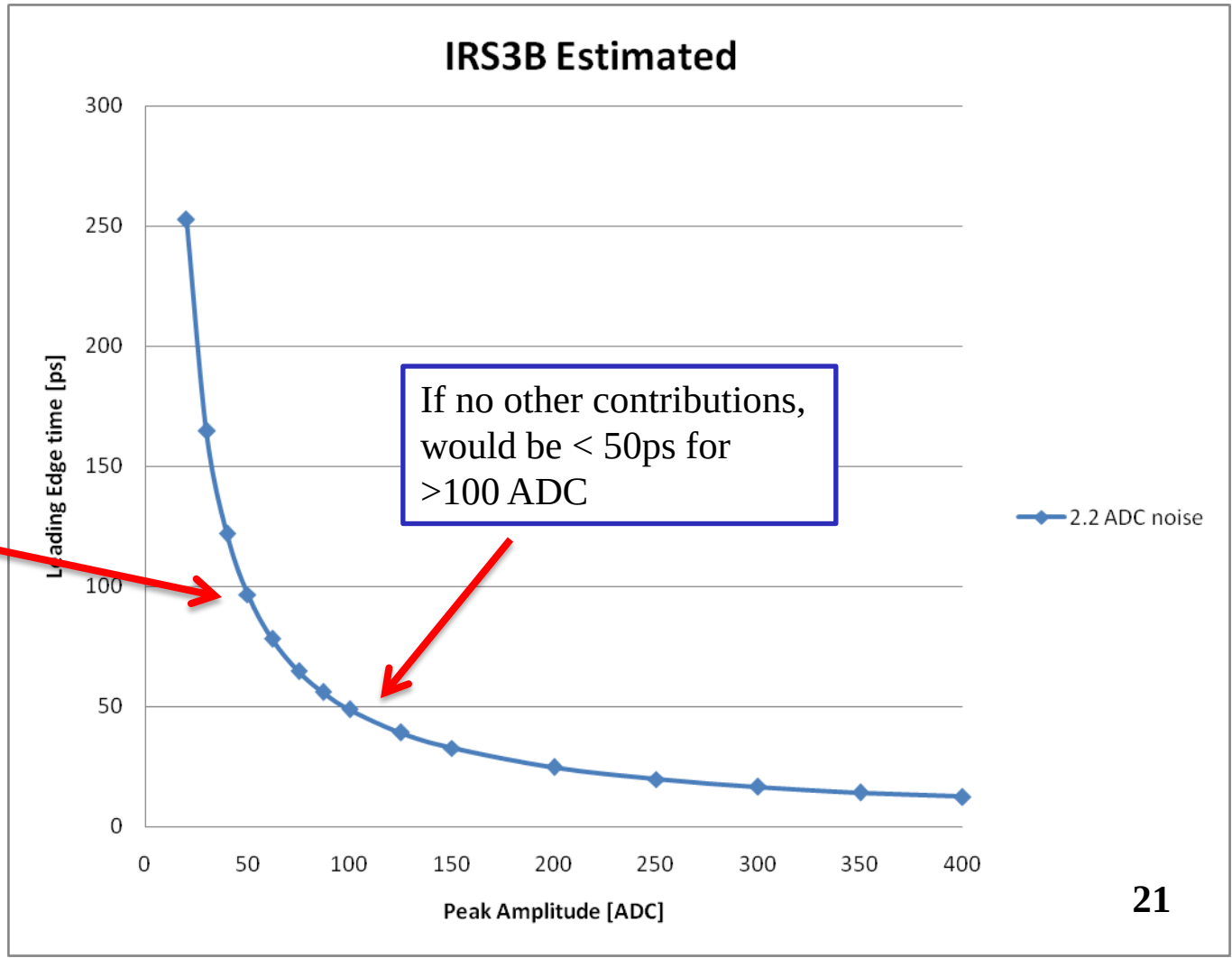
In general, noise is constant: SNR ~ S*C

Noise	2.2 ADC
Risetime	2.7 ns
Sampling rate	2.72 Gsa/s
nom dT	0.368 ns

40% CFD ratio

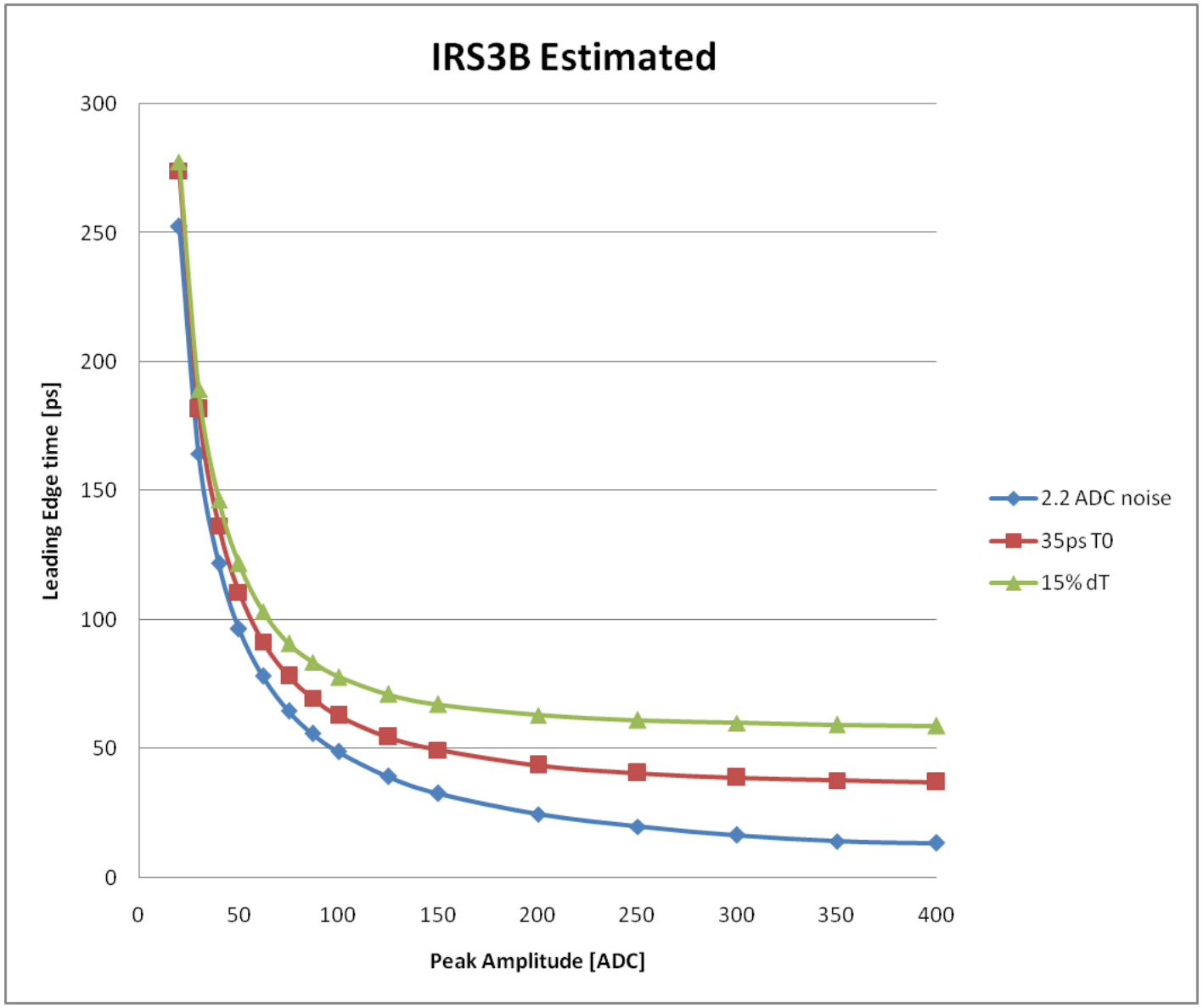
Even in ideal case, for only using 2 points on leading edge, need Vpeak >= 50 ADC to get below 100ps timing

(gain issue)



Adding in realistic degradations

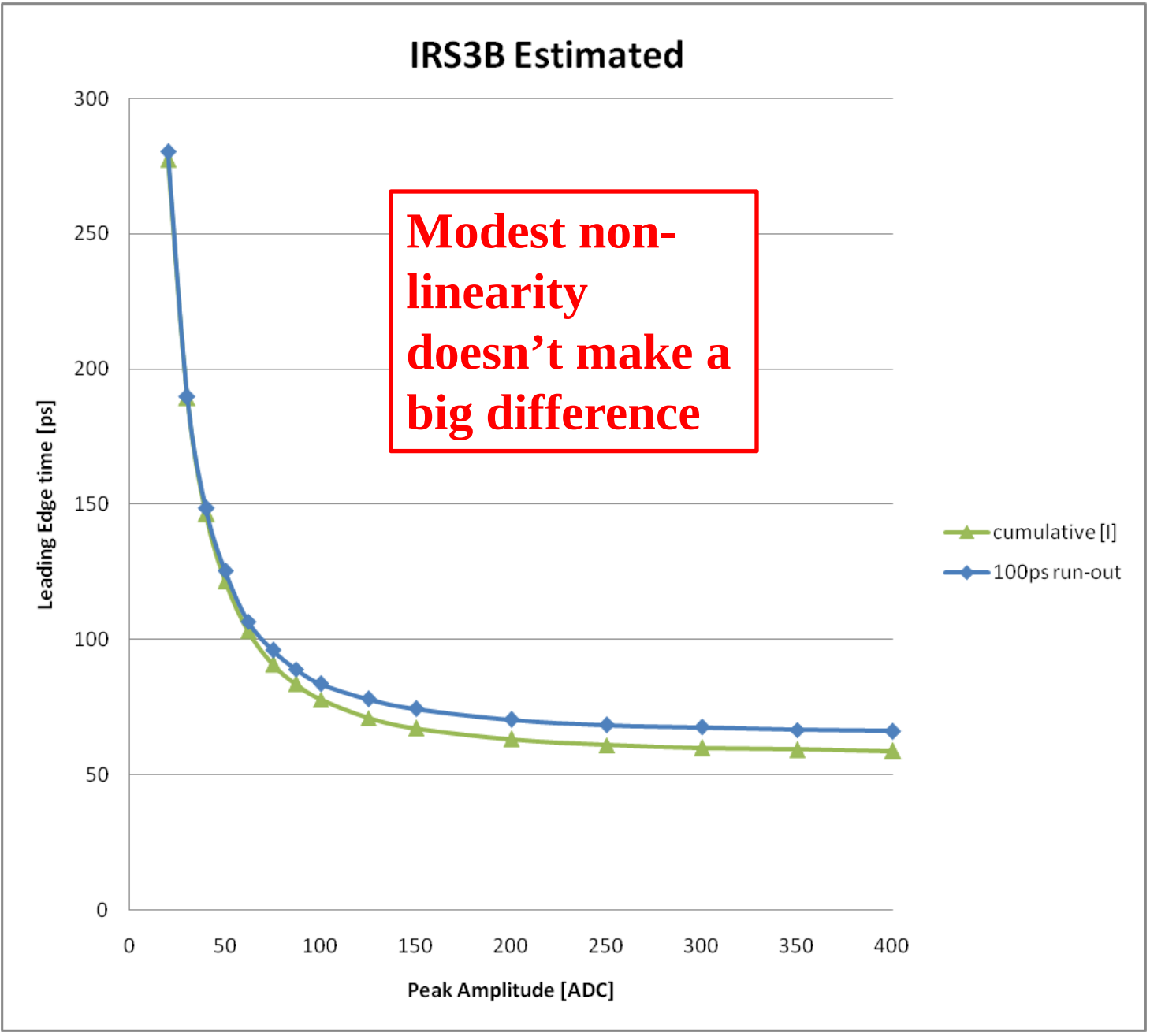
40% CFD ratio



What effects still missing?

- Residual Timebase jitter ?
- Non-linearity on leading edge?
- Something else ?

Adding in realistic degradations (II)

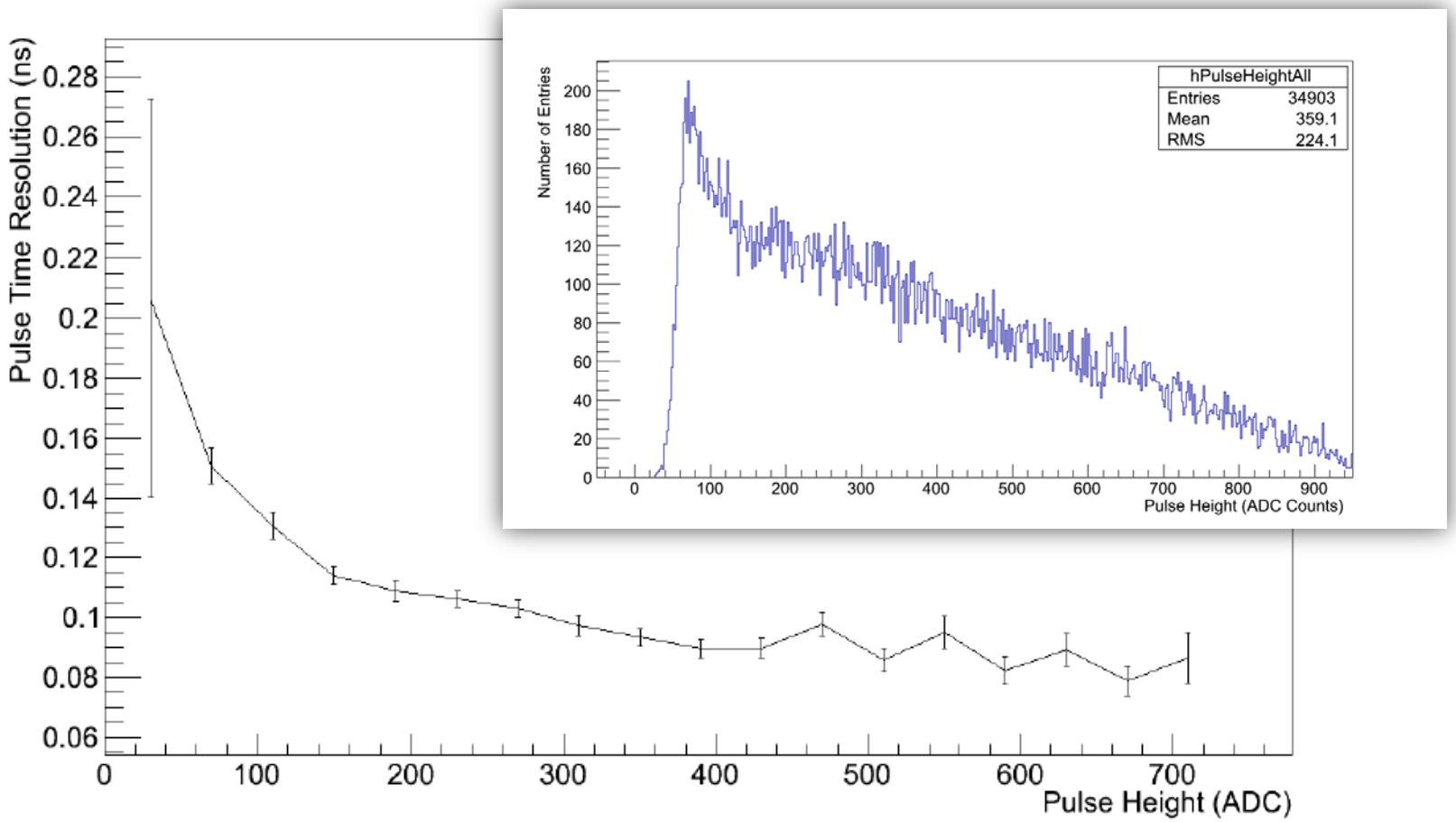


What effects still missing?

Amplifier noise? (doesn't impact pulser or sine data)

What remains to get to <= 50ps ?

1. Increased Amplification



Want >100 ADC counts (>~ 60mV) for smallest pulses

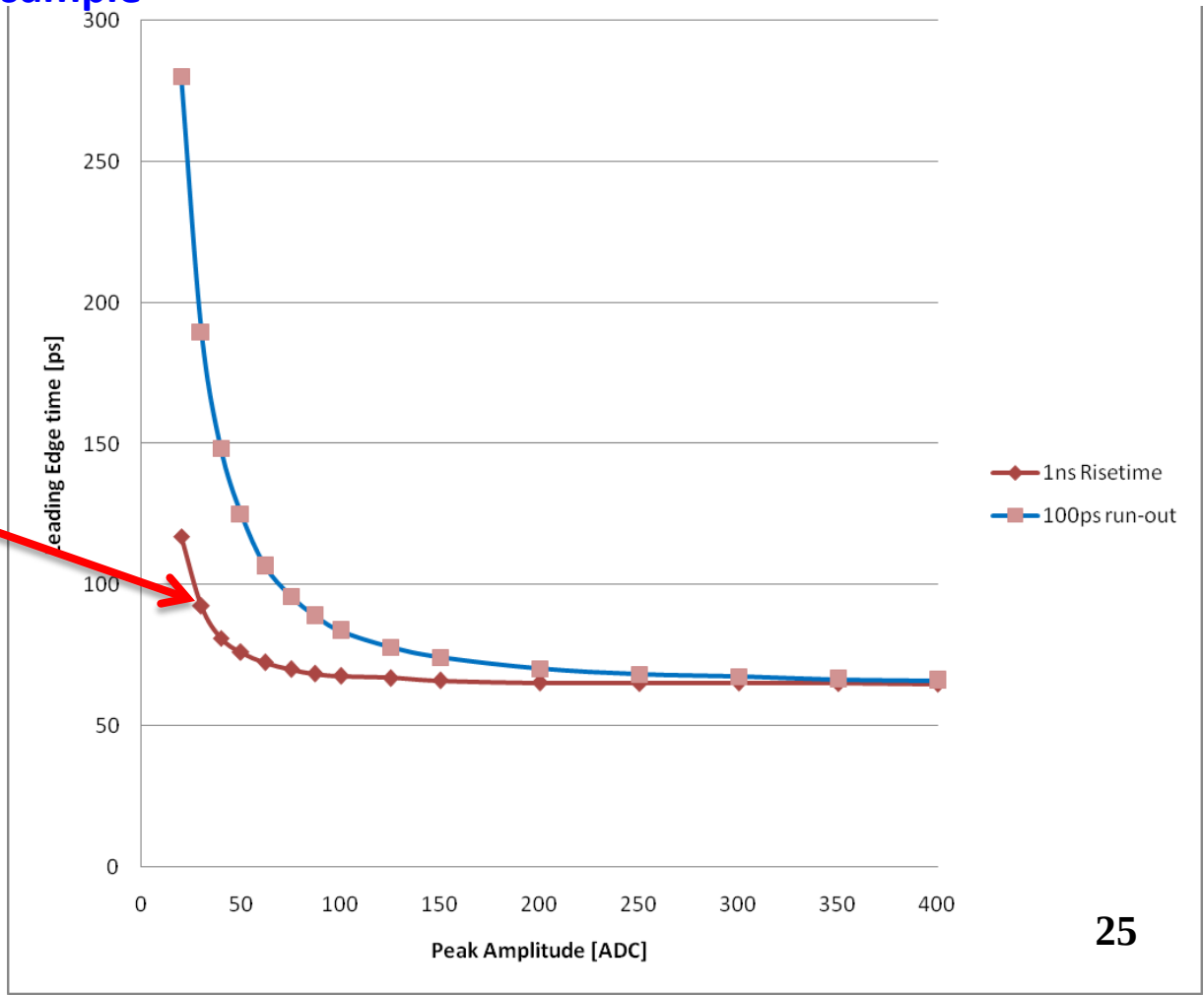
2. Improved Risetime

Vpeak	**100 ADC**
Risetime	**1.0 ns**
Sampling rate	**2.72 Gsa/s**
nom dT	**0.368 ns**
nom dV	**13.617 ADC/sample**

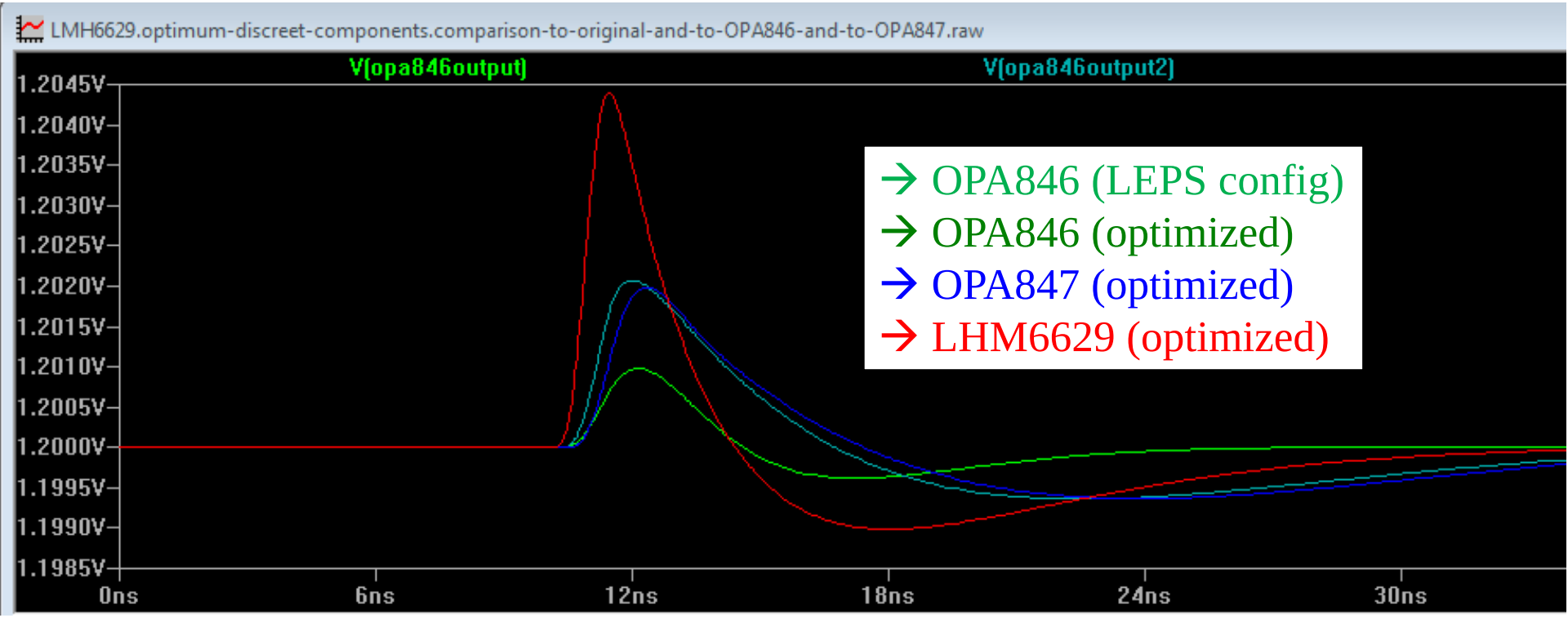
40% CFD ratio

Now < 100ps for ADC>30 (with no other changes)

Increasing amplitude and risetime has similar effect – will do both



Improved Amplifier Choice

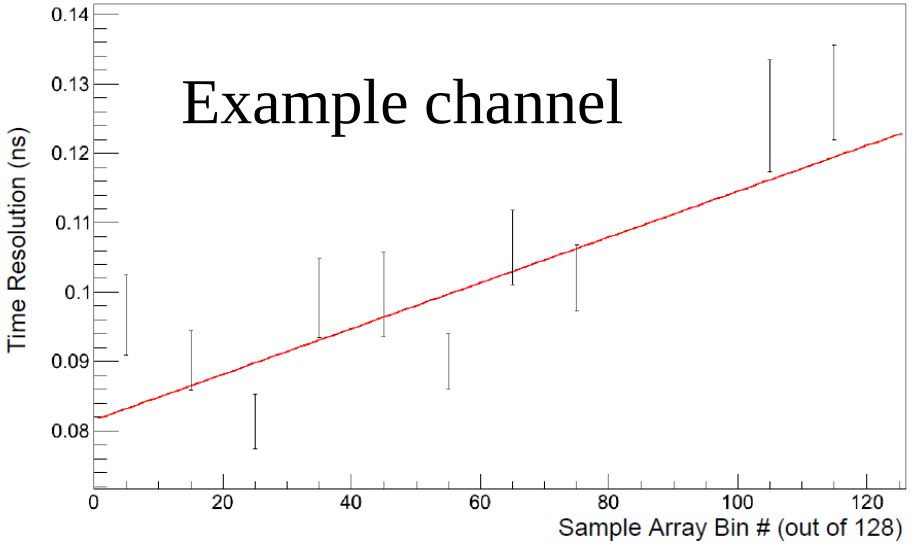


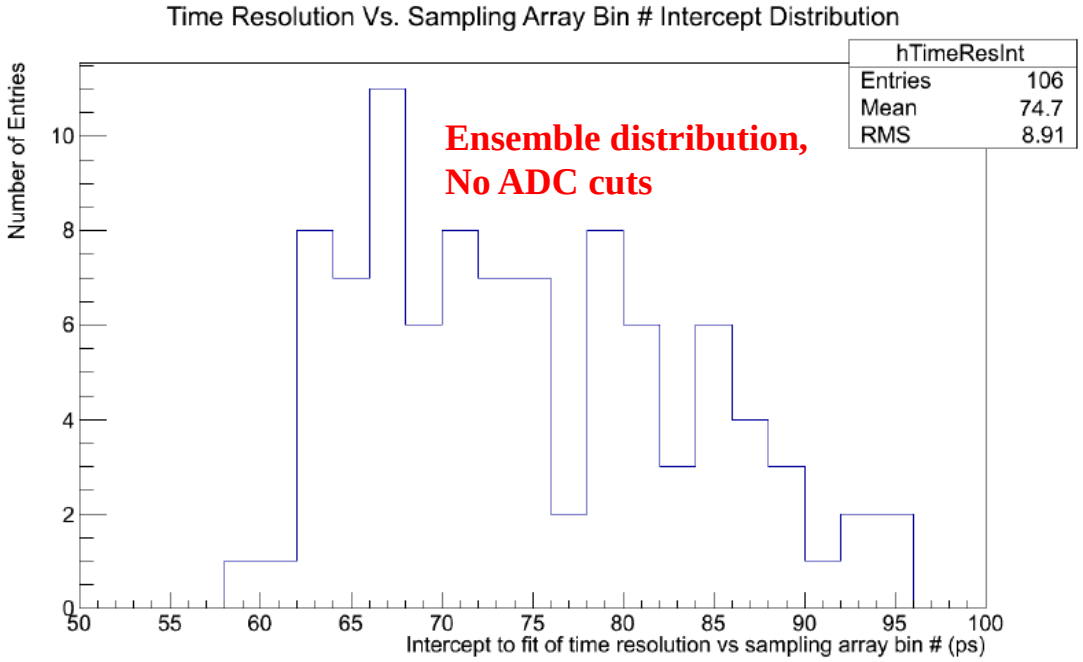
Simulation indicates -- prior to changing layout radically (2x stage design), can already improve amplitude/risetime by switching to LHM6629 (single stage)

4x gain, >2 faster risetime

3. Improve Timebase Stability

A combination of jitter (noise on VadjN) and coarseness of DAC are the primary contributors



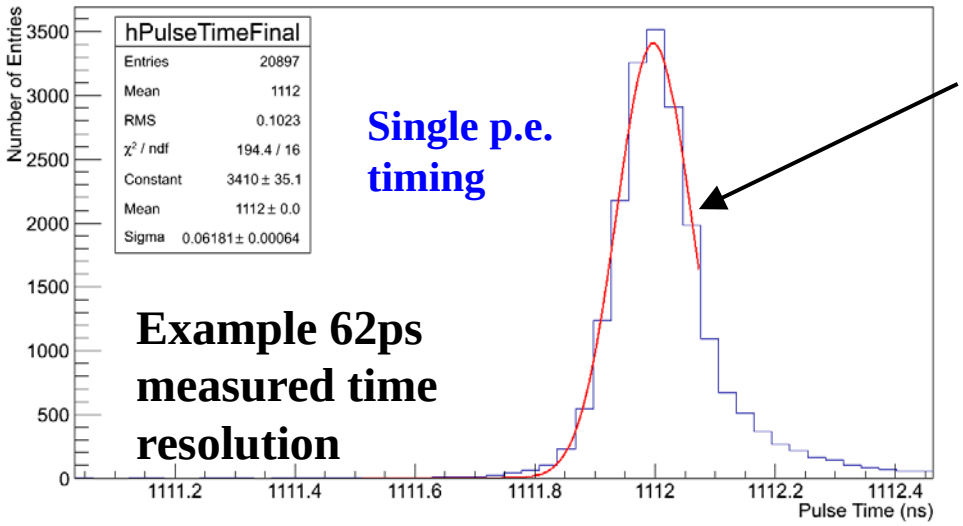


100ps Average

75ps Average

- Plot distribution of intercepts from linear fit to time resolution vs. sampling array bin # plot
- Represents time resolution if there was no degradation along sampling array

Improved amp, calibration

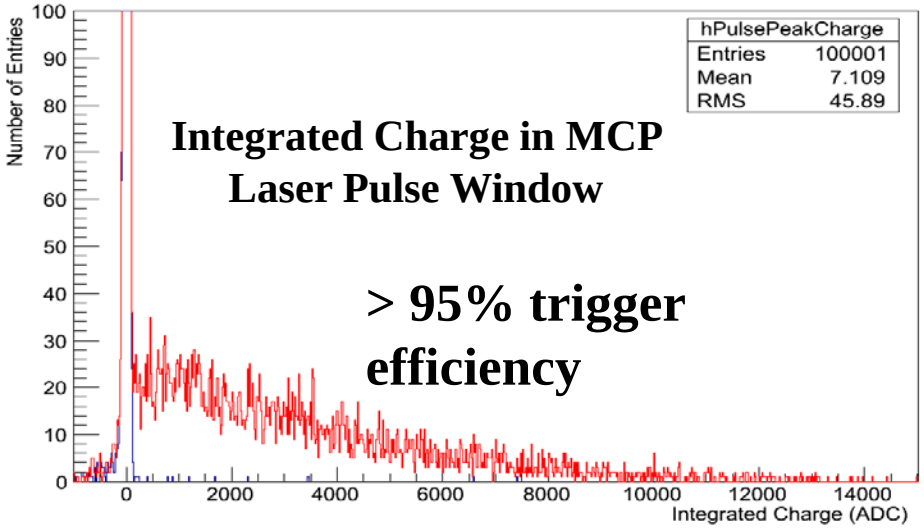


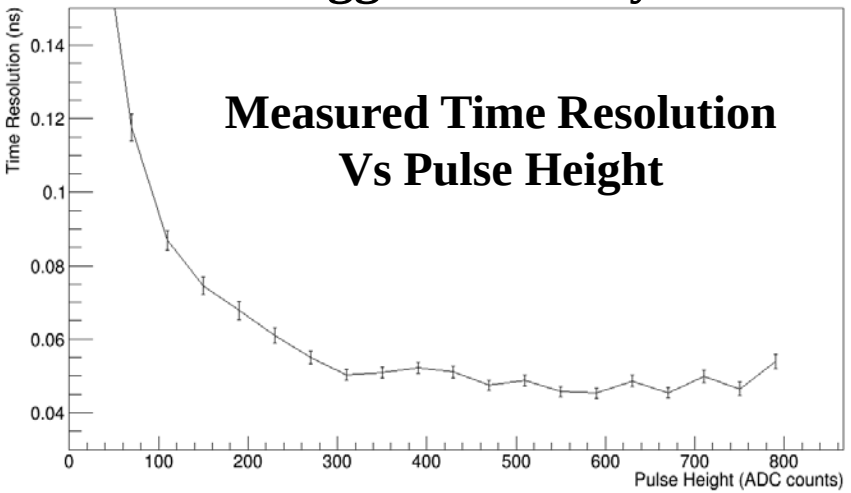
Measure time resolution in core distribution

- Trailing tail expected from photoelectron backscatter within PMT
- Also leading non-Gaussian tail due to small pulses

Requirement: <100ps
Goal: 50ps with higher gain

LEPS beam test: ~100ps timing, 77-86% trigger efficiency





- **Brian will talk about calibration specifics tomorrow**

Summary – Day 5

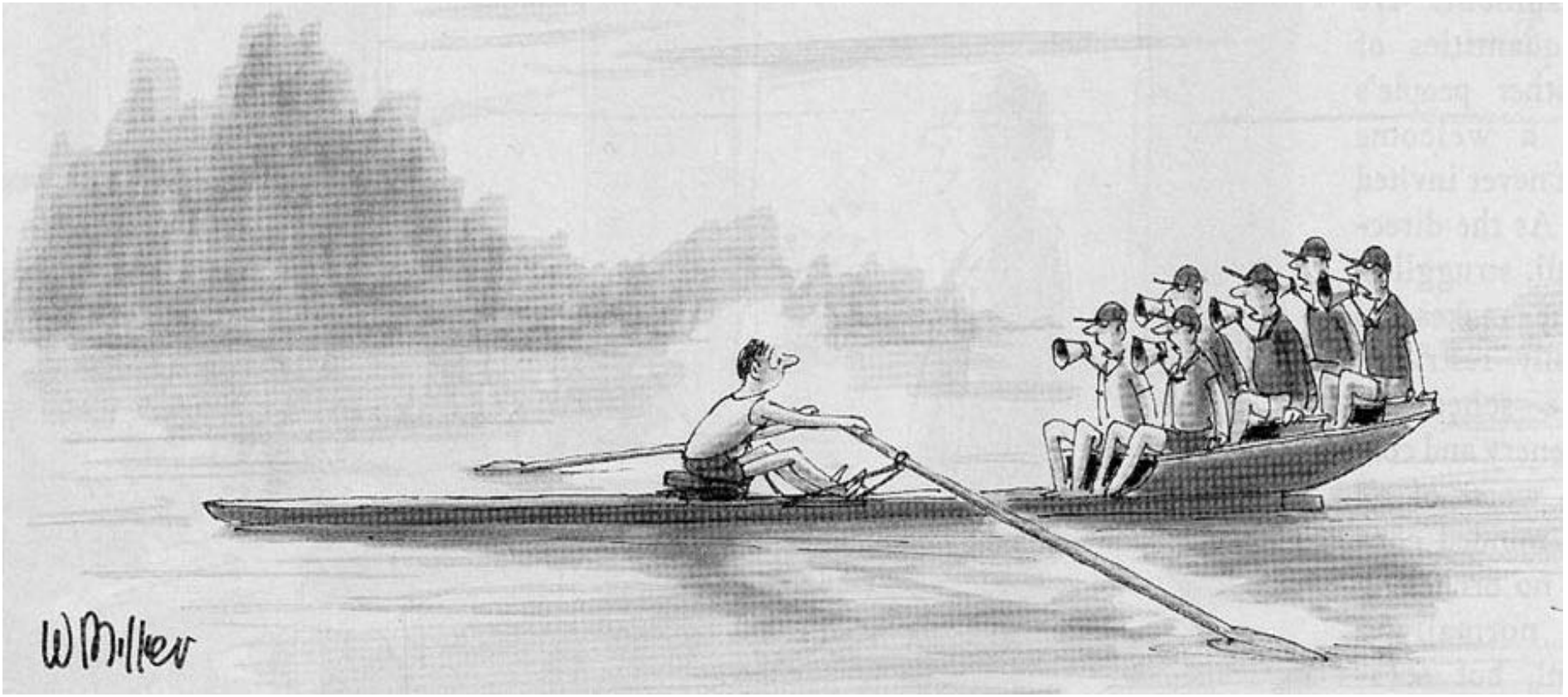
Some additional information provided

- **Go through list of items from last time (next slide)**
- **All of these concepts are straightforward, though much, much, much to be assimilated all at once**
- **Brian Kirby will take you through calibration process tomorrow**
- **Essential issues to be addressed for quality mTC data-taking:**
  - **Are register configurations/feedbacks being set properly ?**
  - **Can we tell ? (meaningful DQM tools ?)**
  - **Understanding what is being done ?**
  - **<u>Calibration!</u> (and diagnostics)**

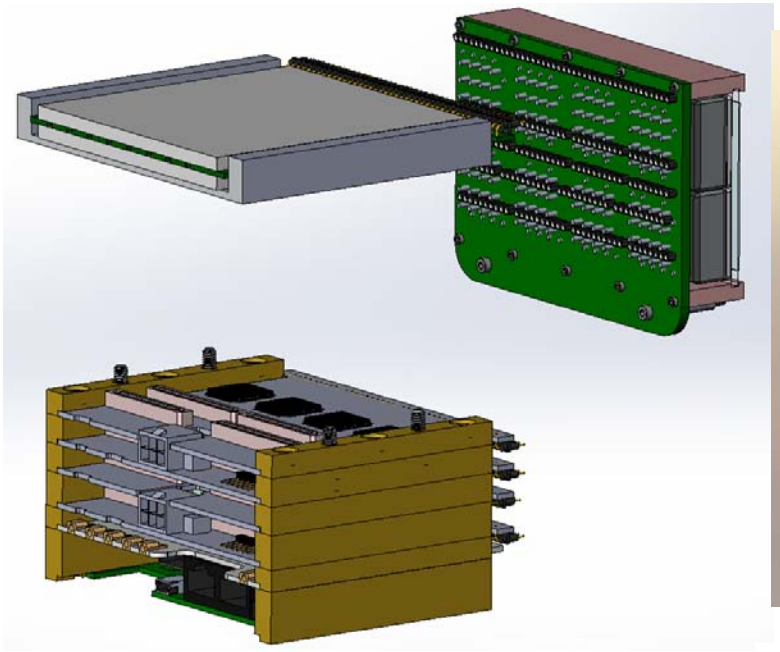
Specific DQM Needs

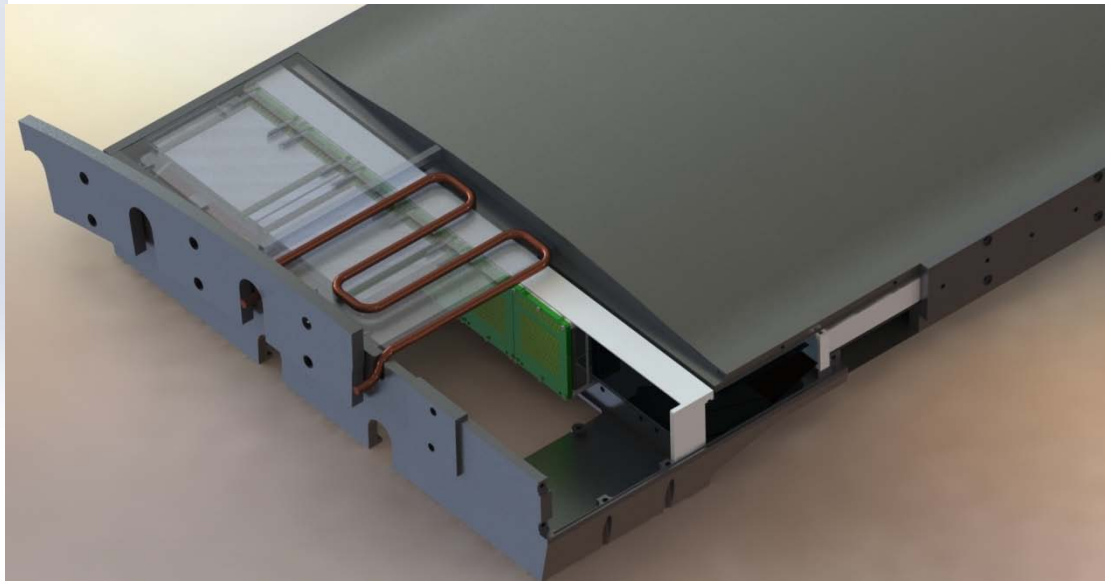
- **As data being accumulated:**
  - **What are best estimates of:**
    - ✓ **Pedestal residual (flag bad windows)**
    - ✓ **Sampling rate**
    - ✓ **Average (normalized) pulse width versus sample number [and across window seam]**
    - ✓ **Window dT**
    - ✓ **Channel hit occupancy**
    - ✓ **Pulse height spectra by channel, by PMT and by event**
    - ✓ **Event “time zero” mean and moment**
    - ✓ **Time offsets between modules and between clock fanout branches**

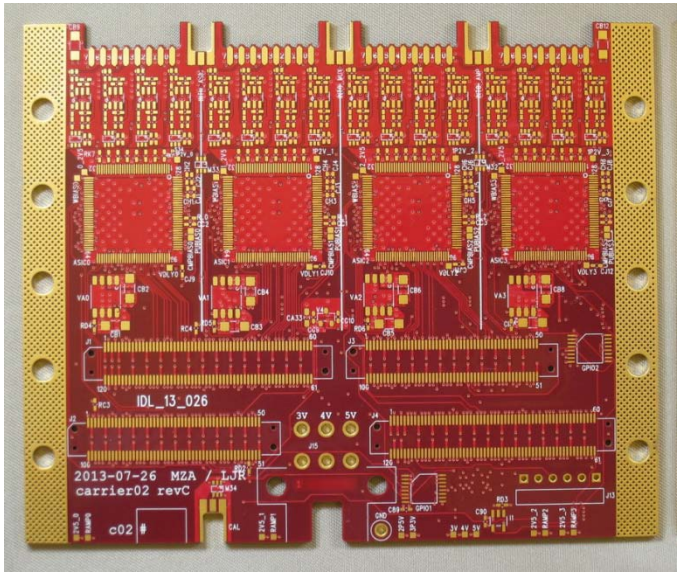
Back-up slides

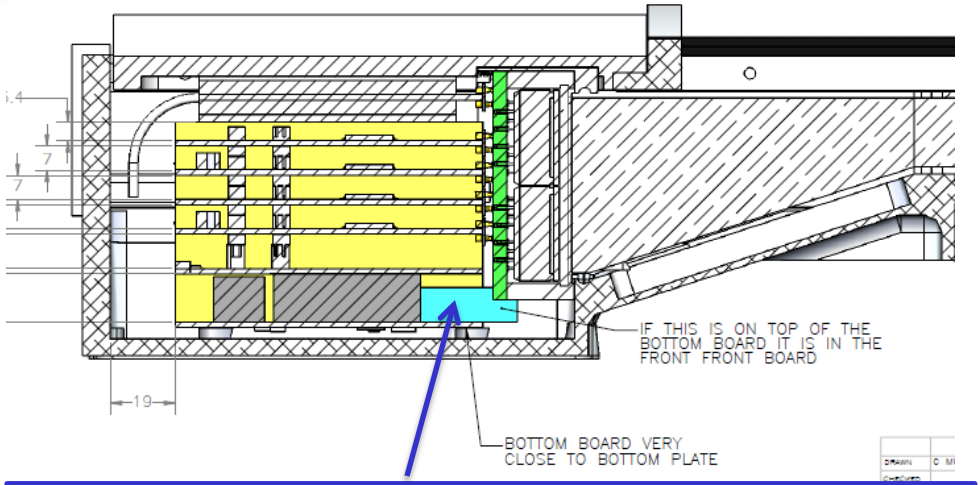


Final Board Stack Mechanics





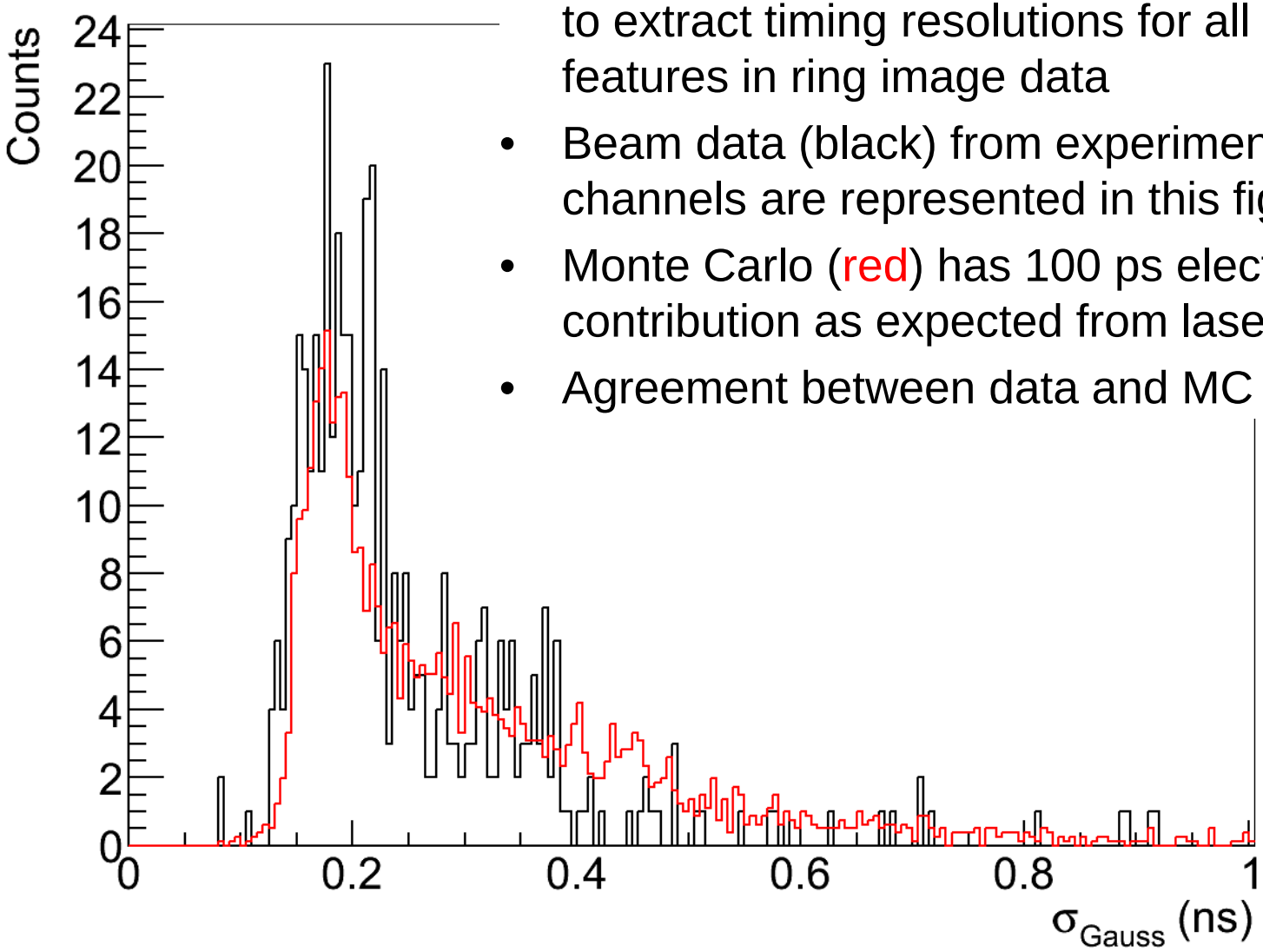




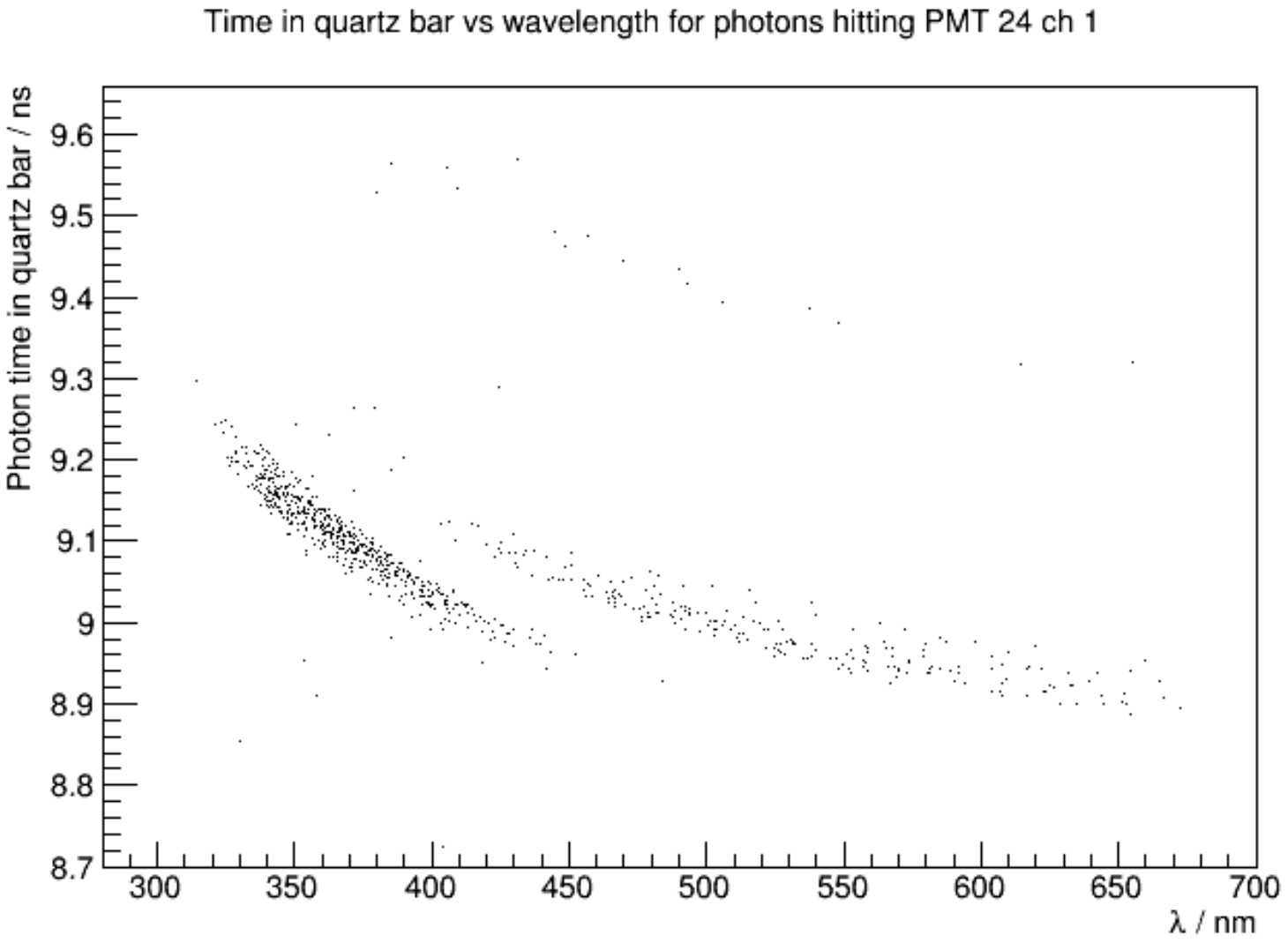
1 last mechanical conflict: fiber transceiver

Timing Widths – All Peaks in Ring Images

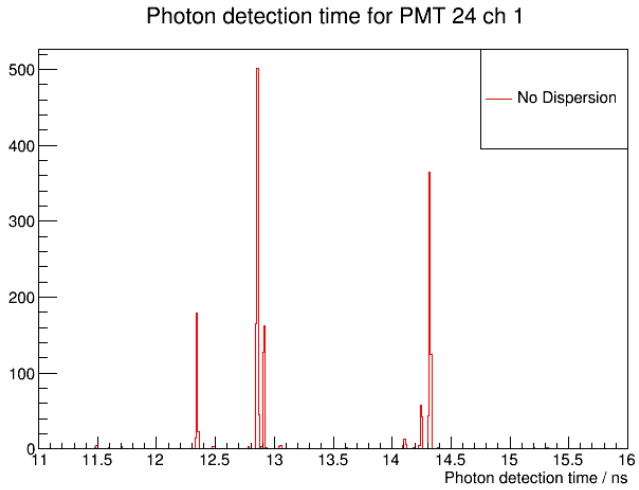
- All channels were analyzed by peak finding/fitting to extract timing resolutions for all narrow (<1 ns) features in ring image data
- Beam data (black) from experiment 2 (373/512 channels are represented in this figure)
- Monte Carlo (red) has 100 ps electronics contribution as expected from laser results
- Agreement between data and MC is excellent

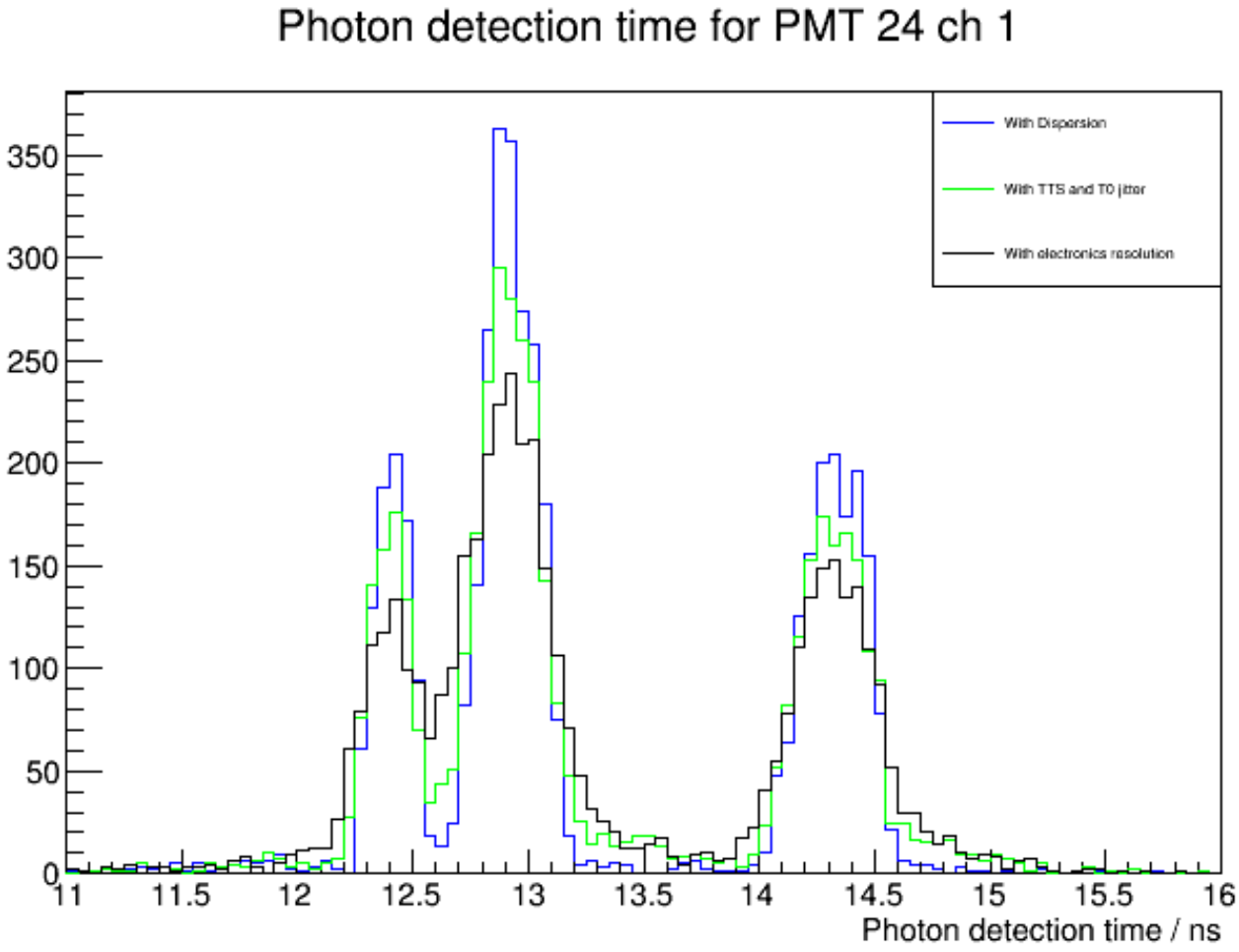


Impact of Propagation



Narrowest leading edge peaks in MC of beamtest data (~120ps)



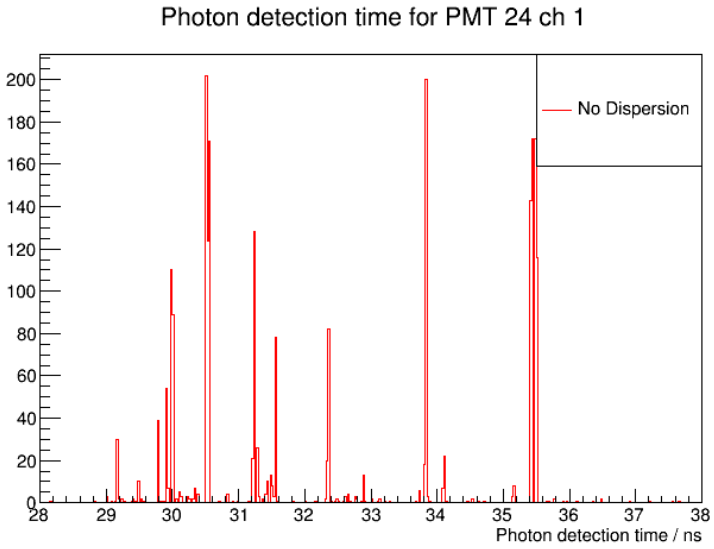


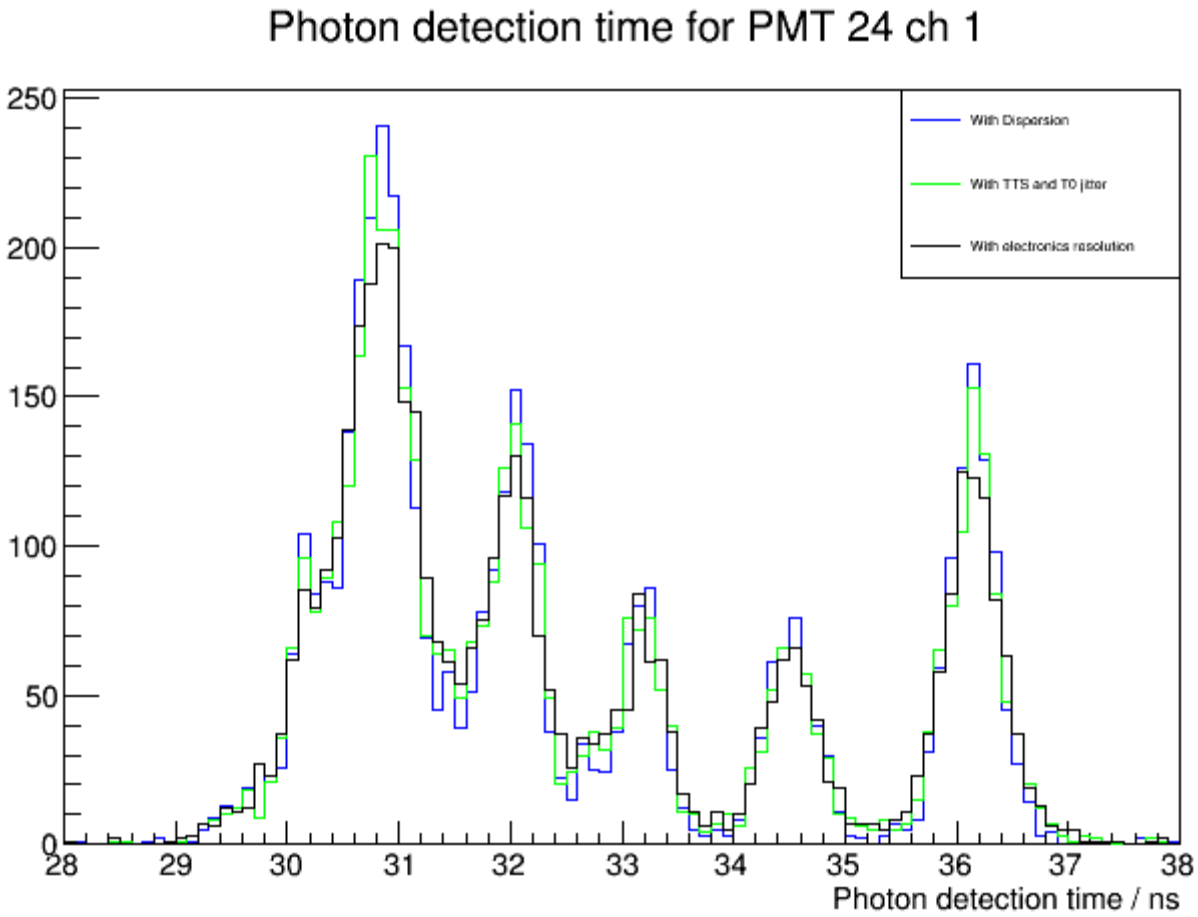
Normal Incidence
1st peak width:

No dispersion: 6-8ps
With dispersion: 90-100ps
+TTS/T0 jitter: 110-120ps
+ electronics: 150-160ps

[M. Barrett]

Timing for Mirror Reflected Peaks

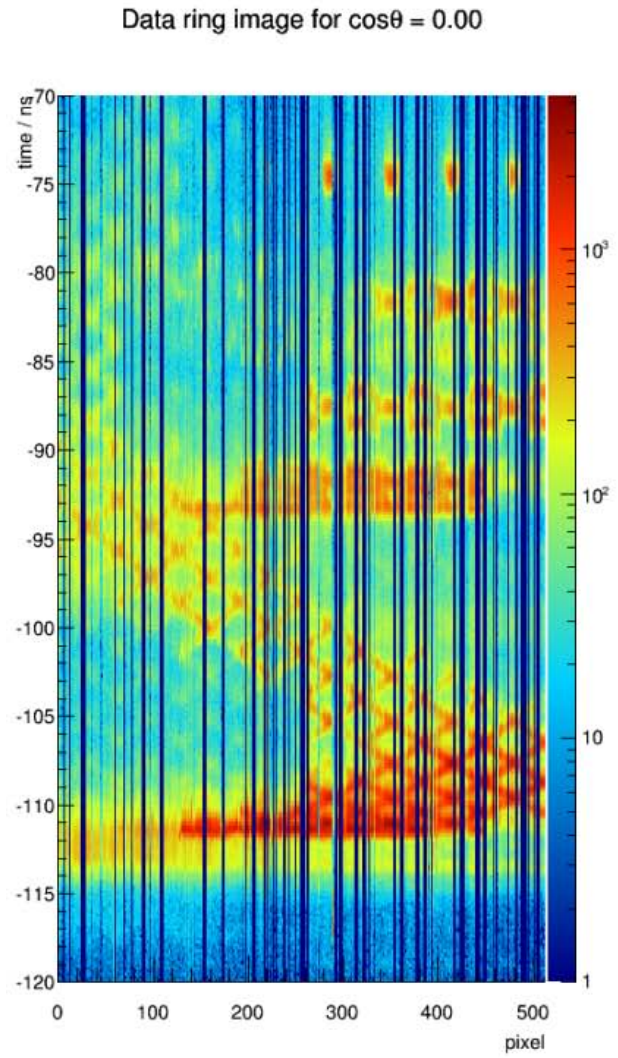


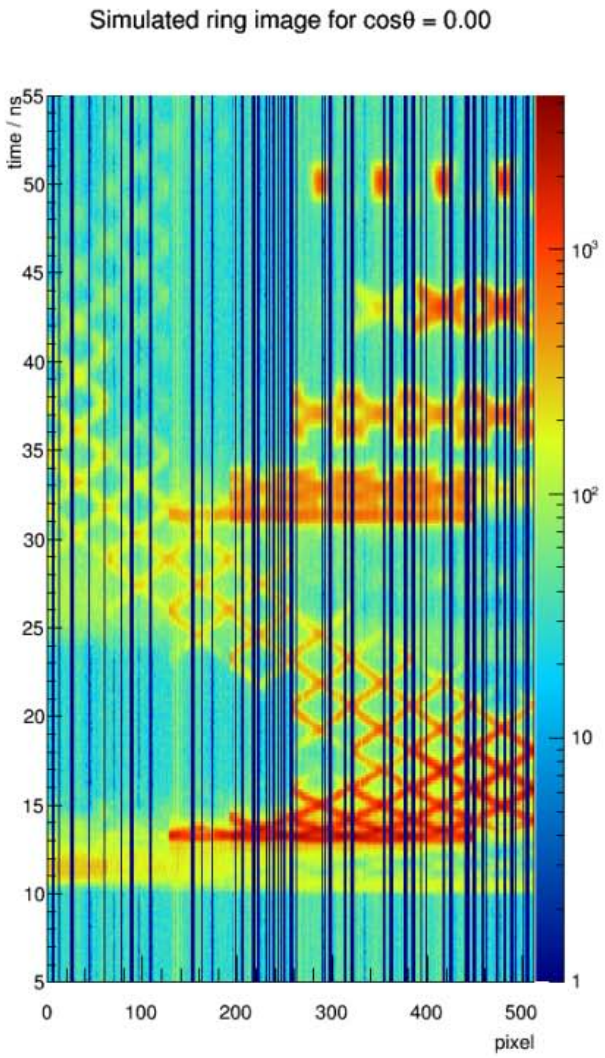


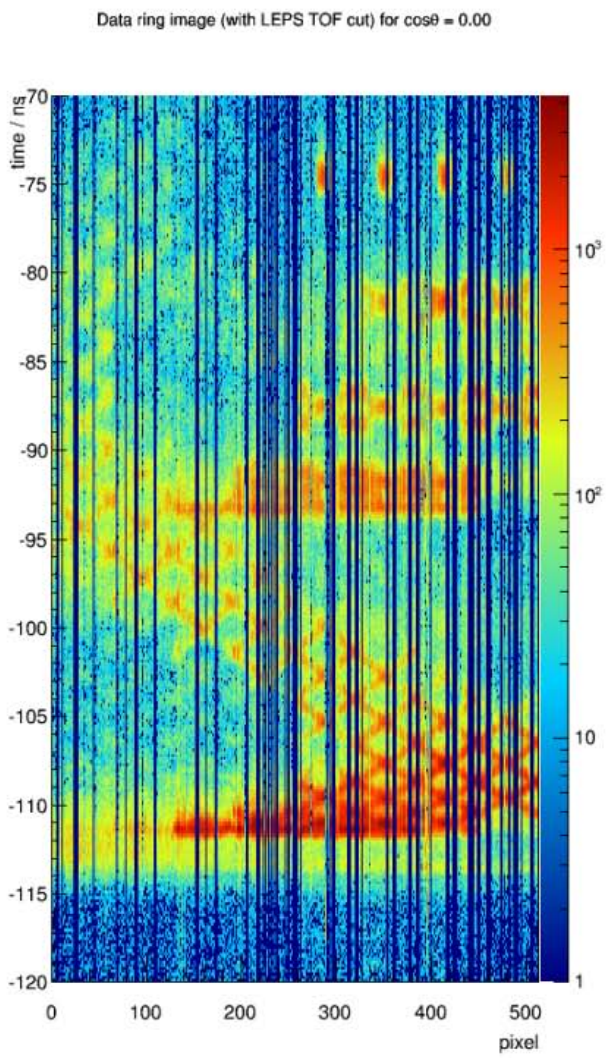
Mirror peaks:

No dispersion: 6-8ps
With dispersion: 300-350ps
+TTS/T0 jitter: 300-350ps as above plus 0-10ps
+ electronics: 300-350ps as above plus 10-20ps

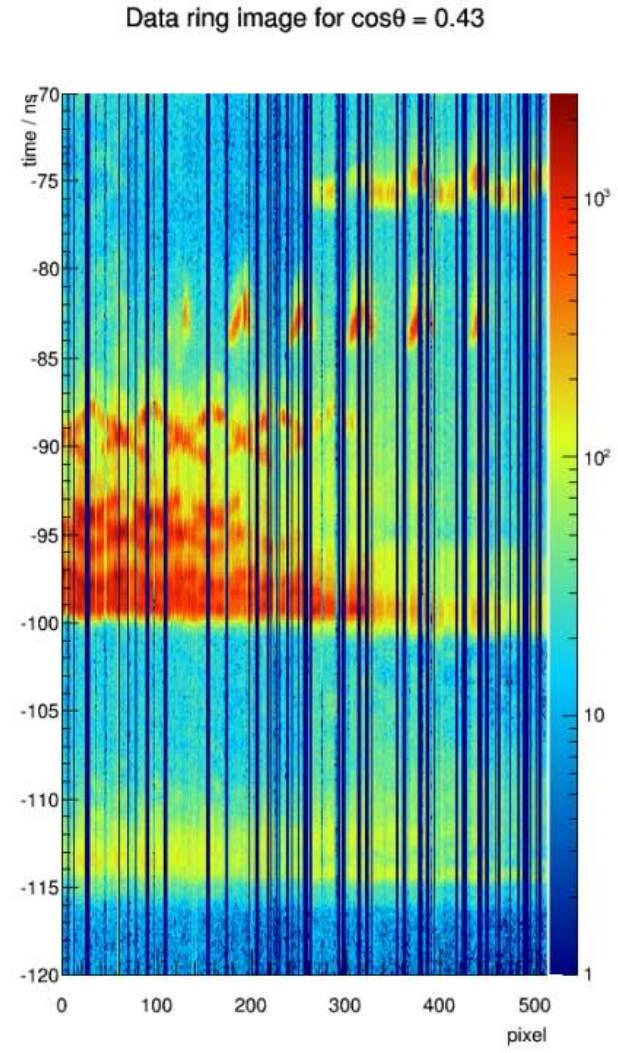
Data/MC Ring Images
Normal Incidence

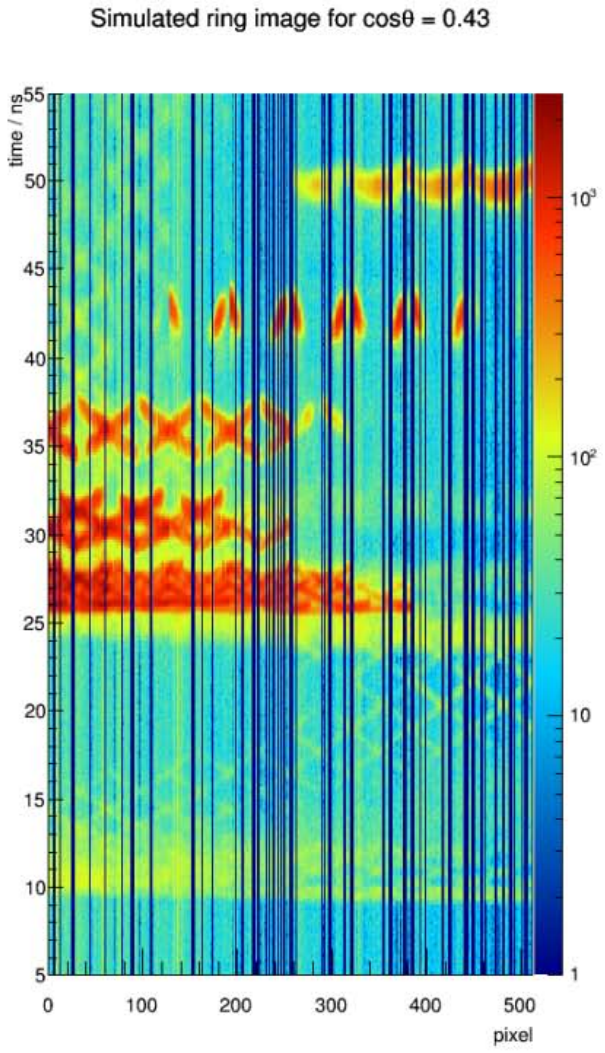


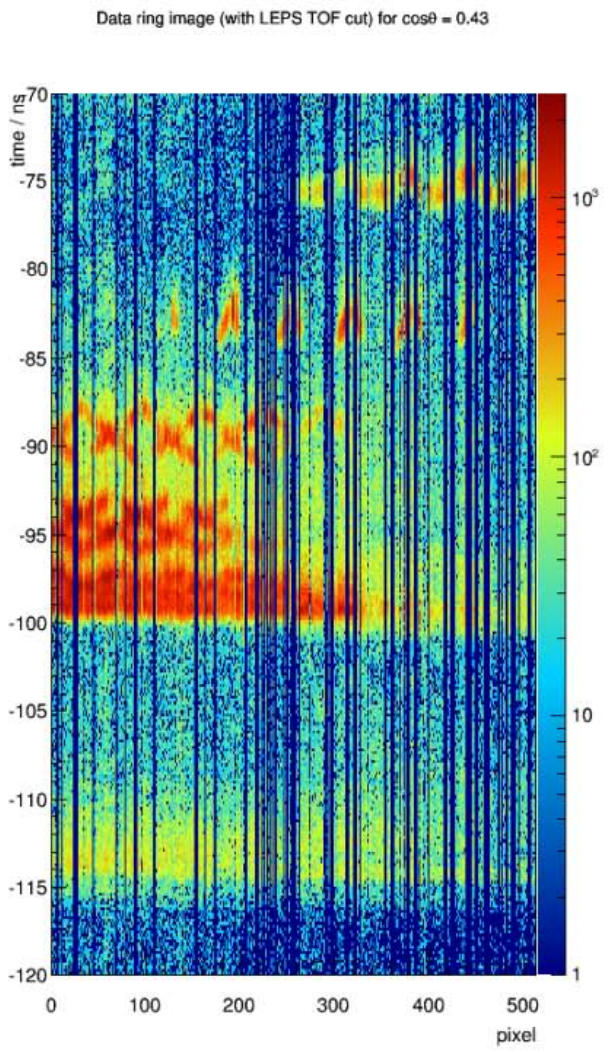




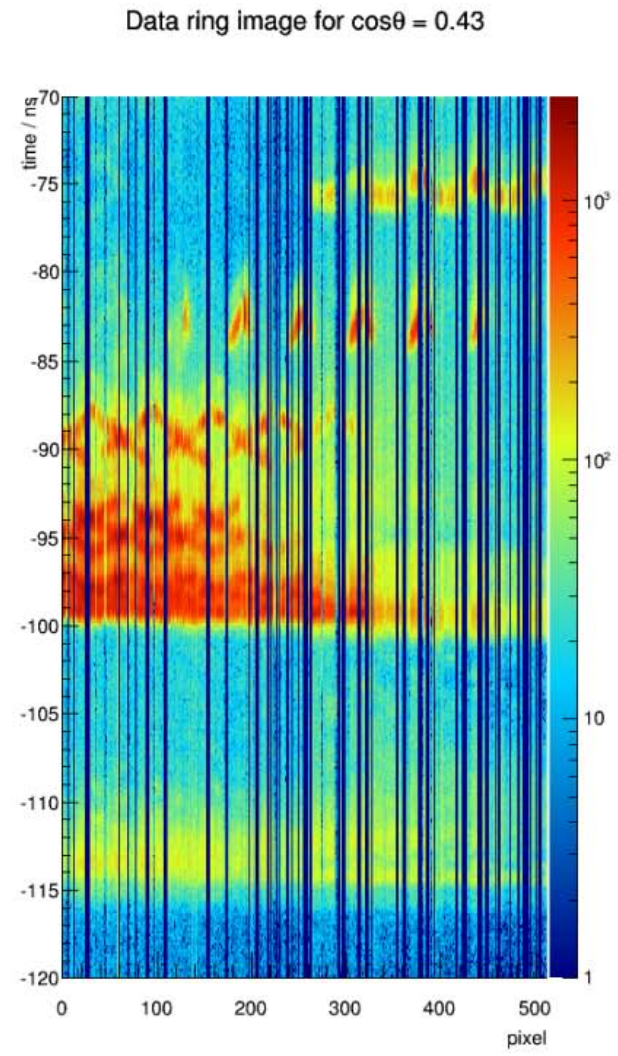
Data/MC Ring Images
Inclined Angle

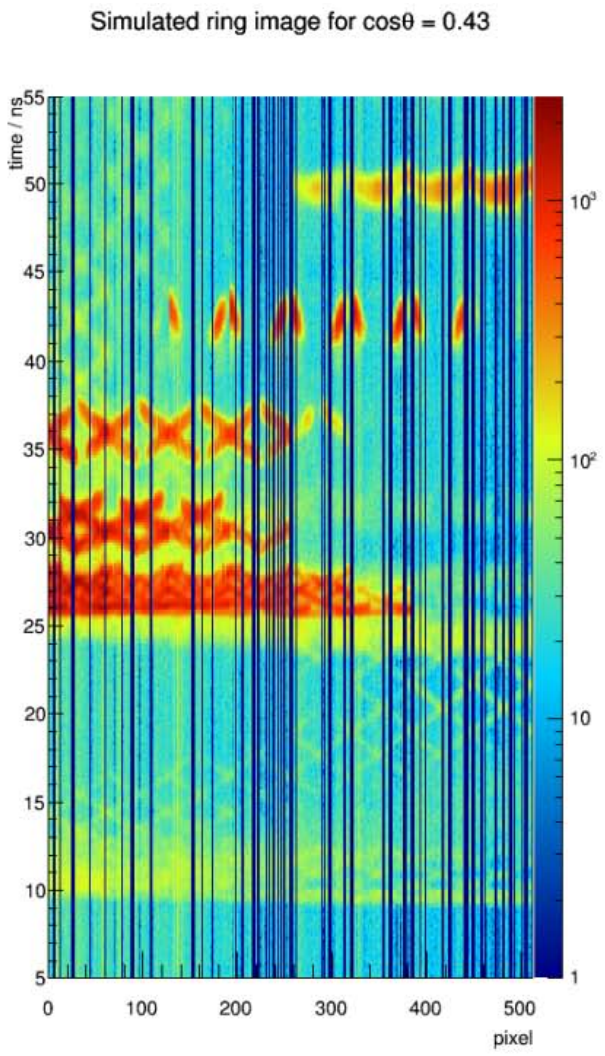


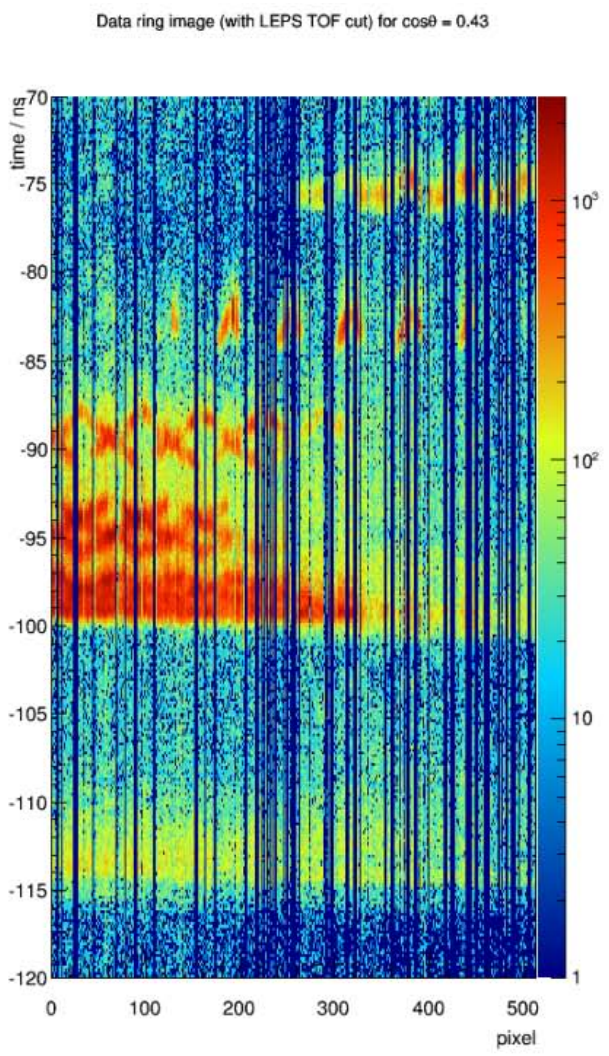




Data/MC Ring Images Near Detector Edge





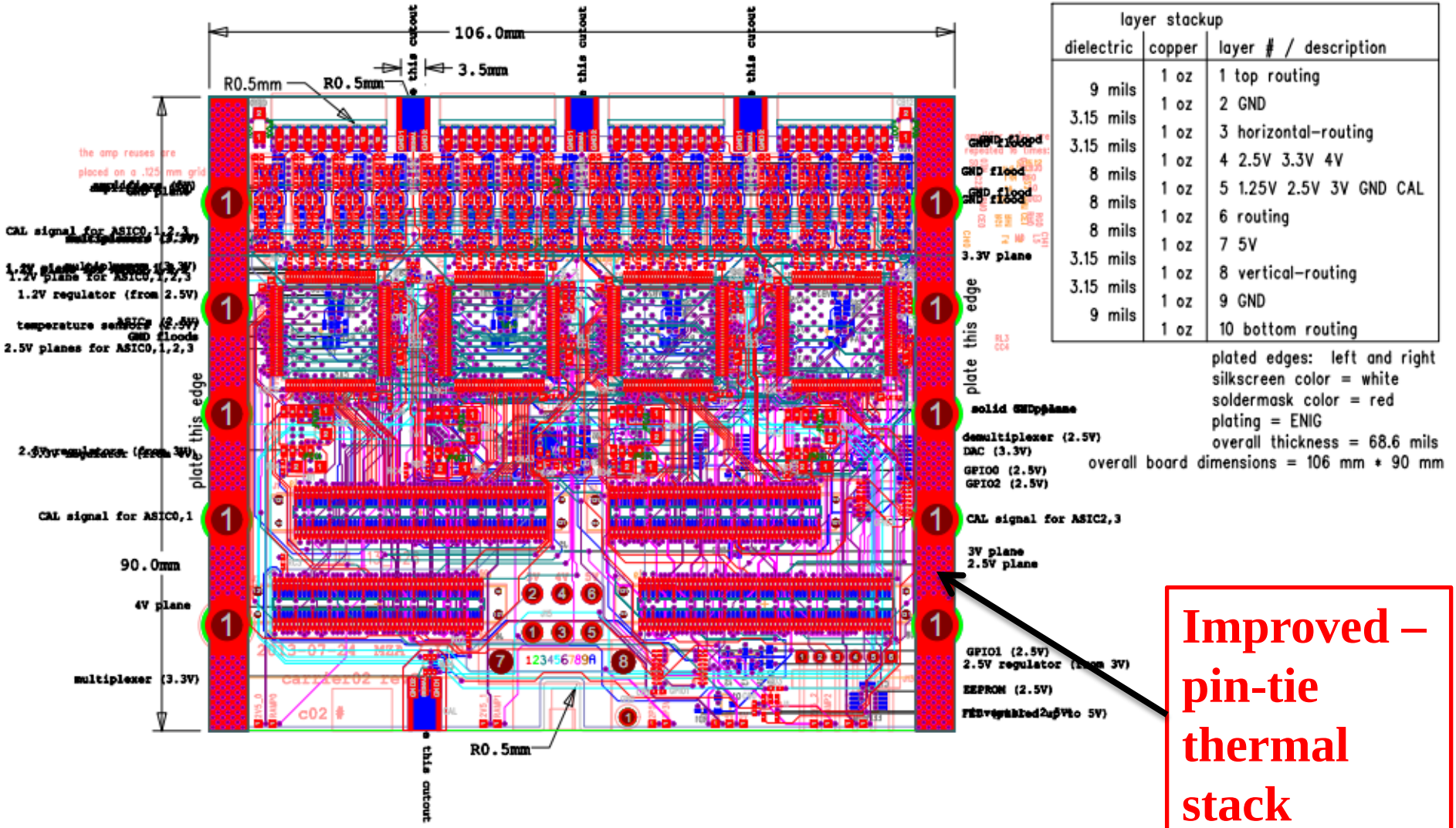


Improvements to carrier02

- √ Will populate with improved amplifiers
- √ add series resistor and capacitors to VadjN/VadjP (10 Ohm+200pF+47nF+2uF)
- √ exchange SMA connectors for MMCX
- √ exchange 12 bit external DAC for 16 bit one in same series
- √ re-visit c02 wiring to allow powering entire boardstack with just one cable
- √ extend width of boards and add holes for new thermal wall structure concept
- √ swap ASIC regulator for one with a shutdown feature

full list at http://www.phys.hawaii.edu/~mza/PCB/iTOP/boardstack-v3.html

Layout of carrier02 revC



layer stackup		
dielectric	copper	layer # / description
	1 oz	1 top routing
9 mils	1 oz	2 GND
3.15 mils	1 oz	3 horizontal-routing
3.15 mils	1 oz	4 2.5V 3.3V 4V
8 mils	1 oz	5 1.25V 2.5V 3V GND CAL
8 mils	1 oz	6 routing
8 mils	1 oz	7 5V
3.15 mils	1 oz	8 vertical-routing
3.15 mils	1 oz	9 GND
9 mils	1 oz	10 bottom routing

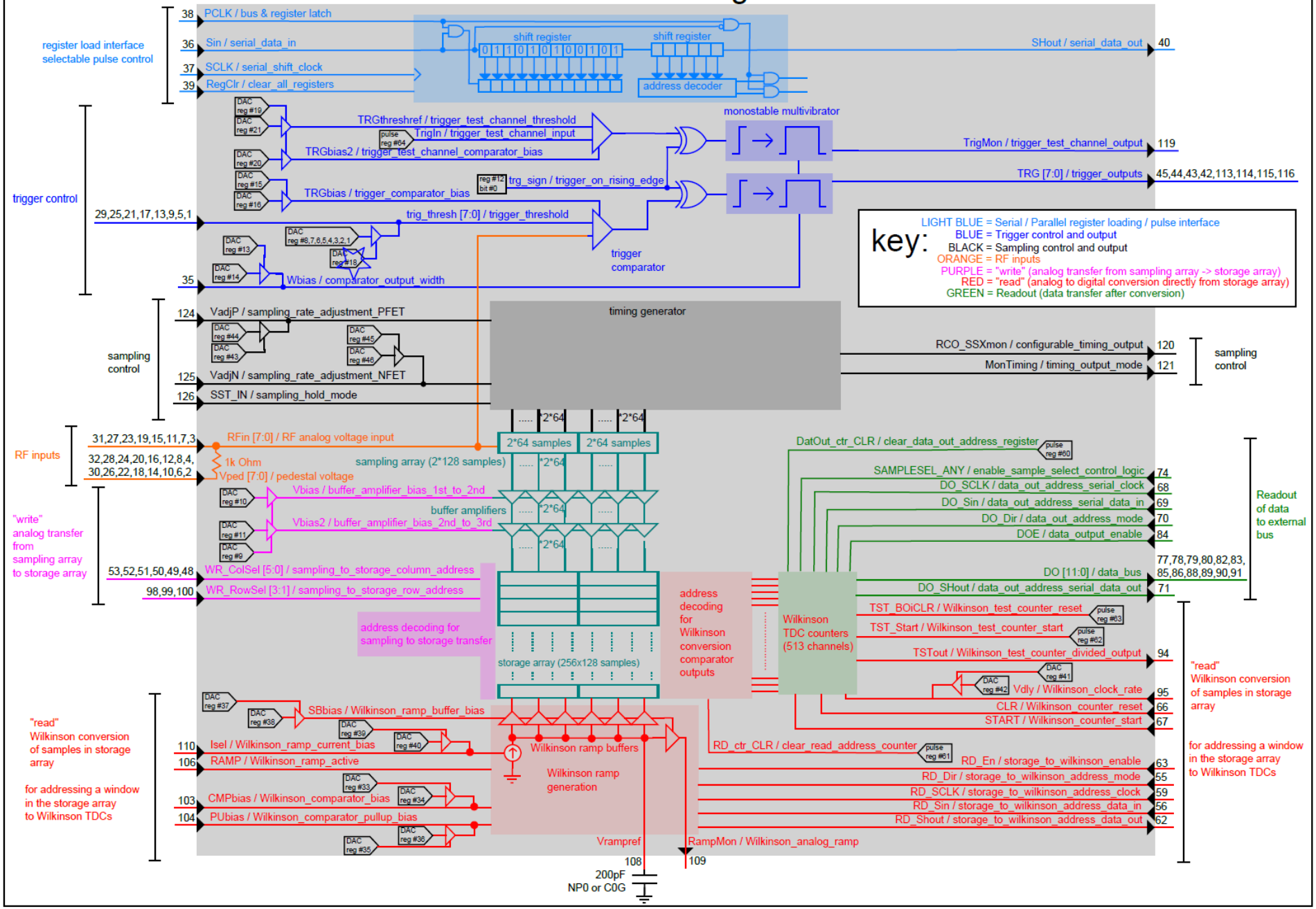
plated edges: left and right
silkscreen color = white
soldermask color = red
plating = ENIG
overall thickness = 68.6 mils
overall board dimensions = 106 mm * 90 mm

Improved – pin-tie thermal stack

design posted at:
http://www.phys.hawaii.edu/~mza/PCB/iTOP/carriers/index.html

IRS3B block diagram

2012-10-23

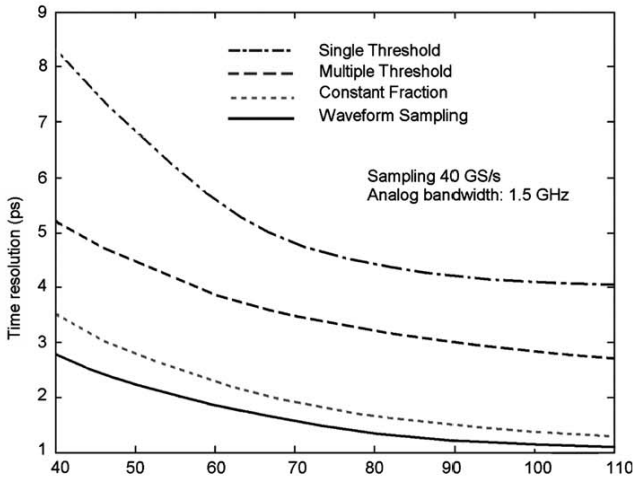


http://www.phys.hawaii.edu/~mza/ASIC/IRS2-BLAB3A/index.html

Expectations – matched to measurements

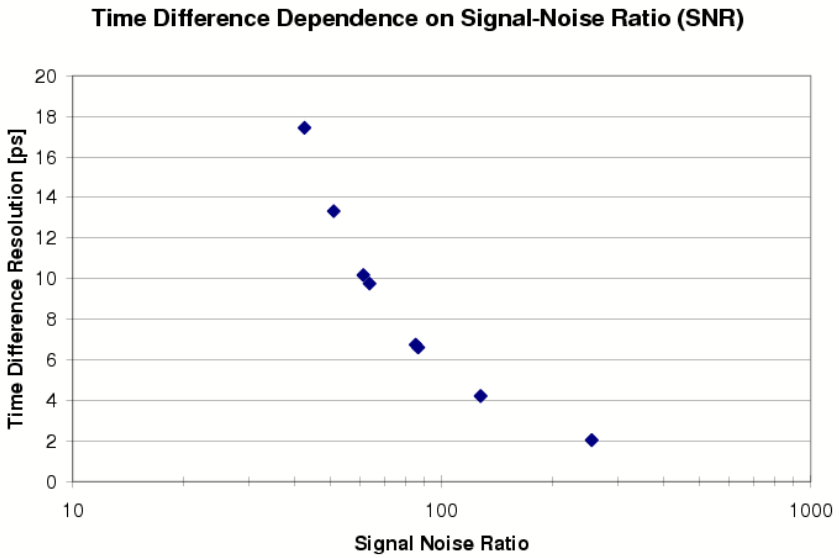
- Noise/amplitude
- Non-linearity
- Timebase non-uniformity

Simulation includes MCP response



J-F Genat, G. Varner, F. Tang, H. Frisch
NIM A**607 (2009) 387-393**.

1GHz analog bandwidth, 5GSa/s



G. Varner and L. Ruckman
NIM A**602 (2009) 438-445**.