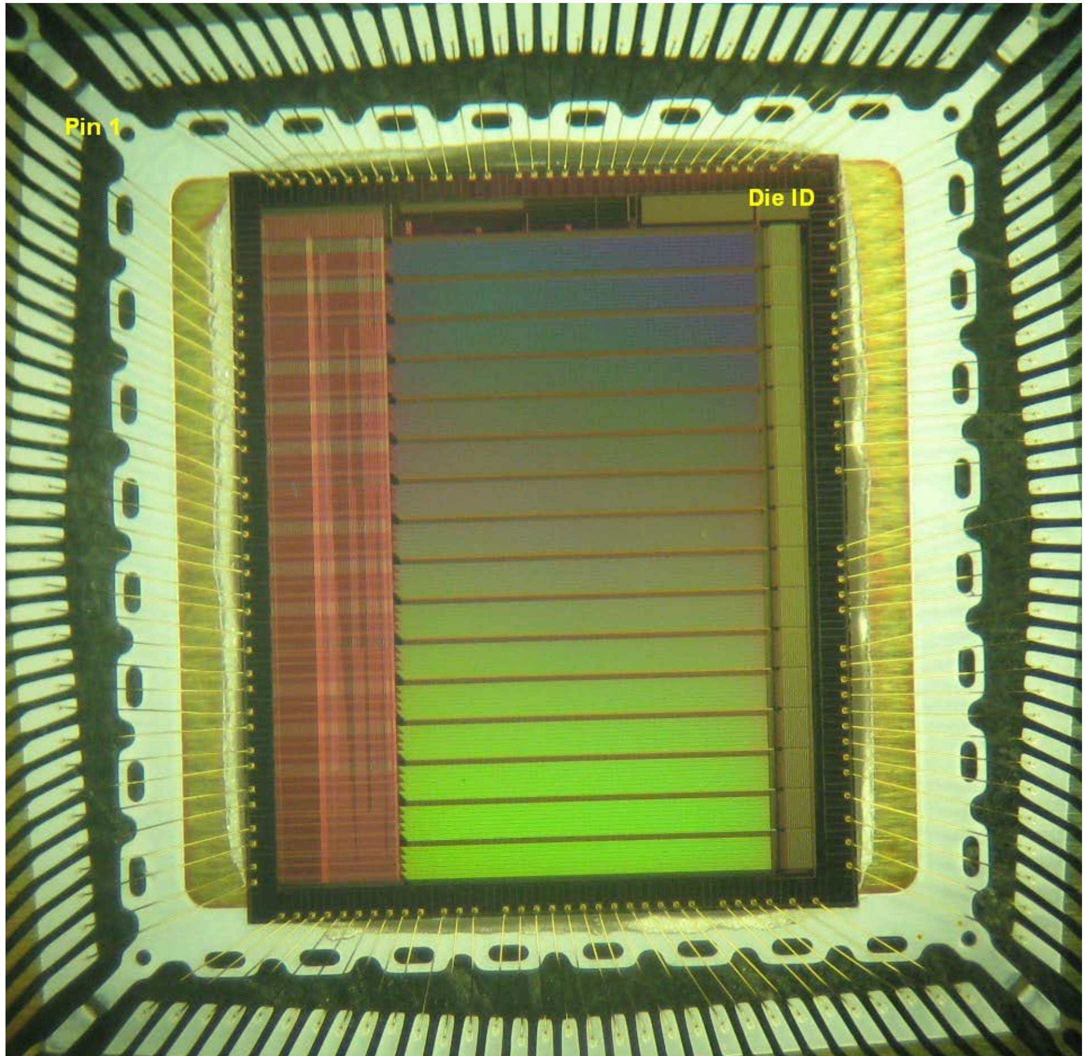
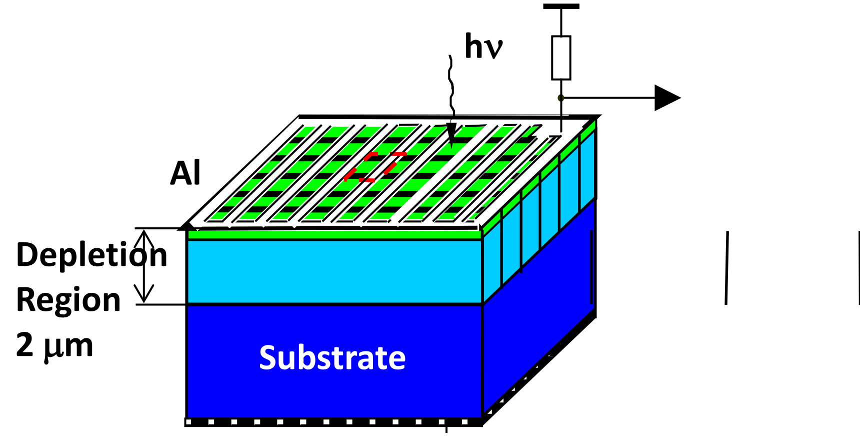
# Reminder of some practical aspects of the TARGETX ASIC

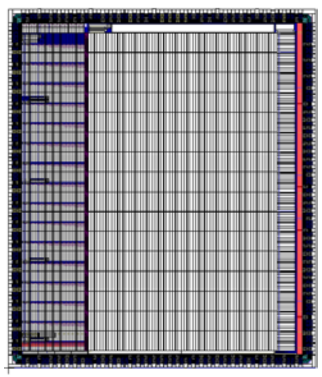


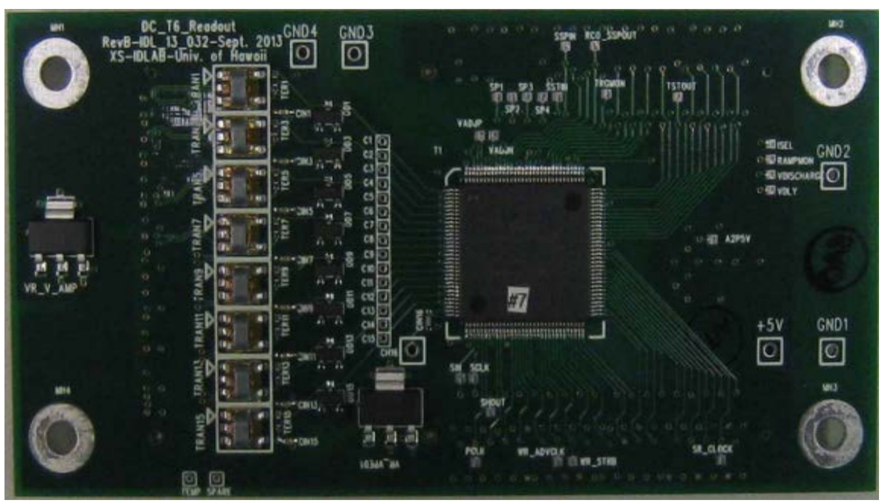


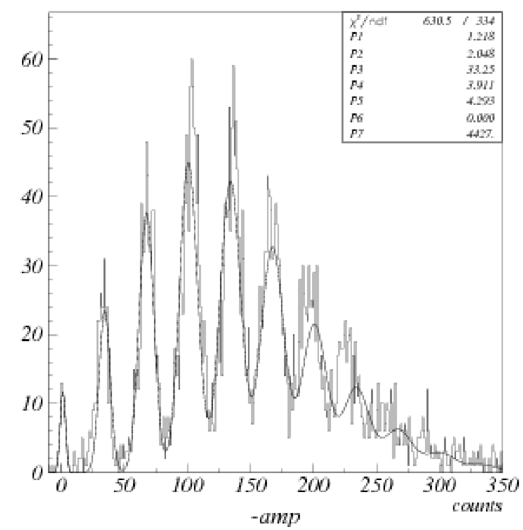
Gary S. Varner -- 7 MAR 2016

# TARGET Application



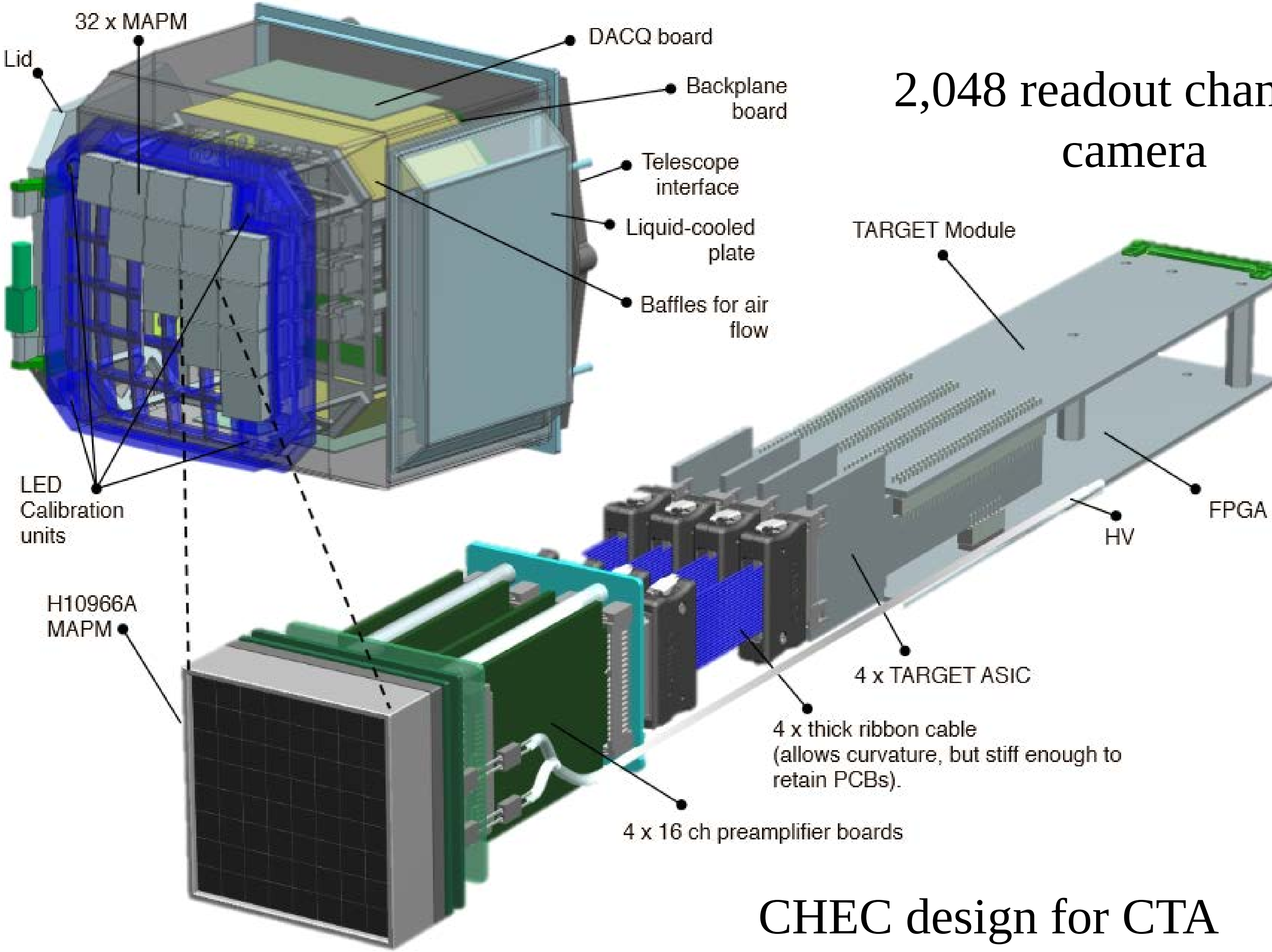



- **16 channels**
- **0.5-1.2 GSa/s**
- **10-12-bit digitization**
- **Samples stored, digitized in groups of 32**
- **16k samples per channel (16us at 1GSa/s)**
- **Integrated triggering capability**

500kHz – 2MHz dark rate not a problem:
5 p.e. threshold reduces rate to < 1kHz
while maintaining > 99% MIP efficiency

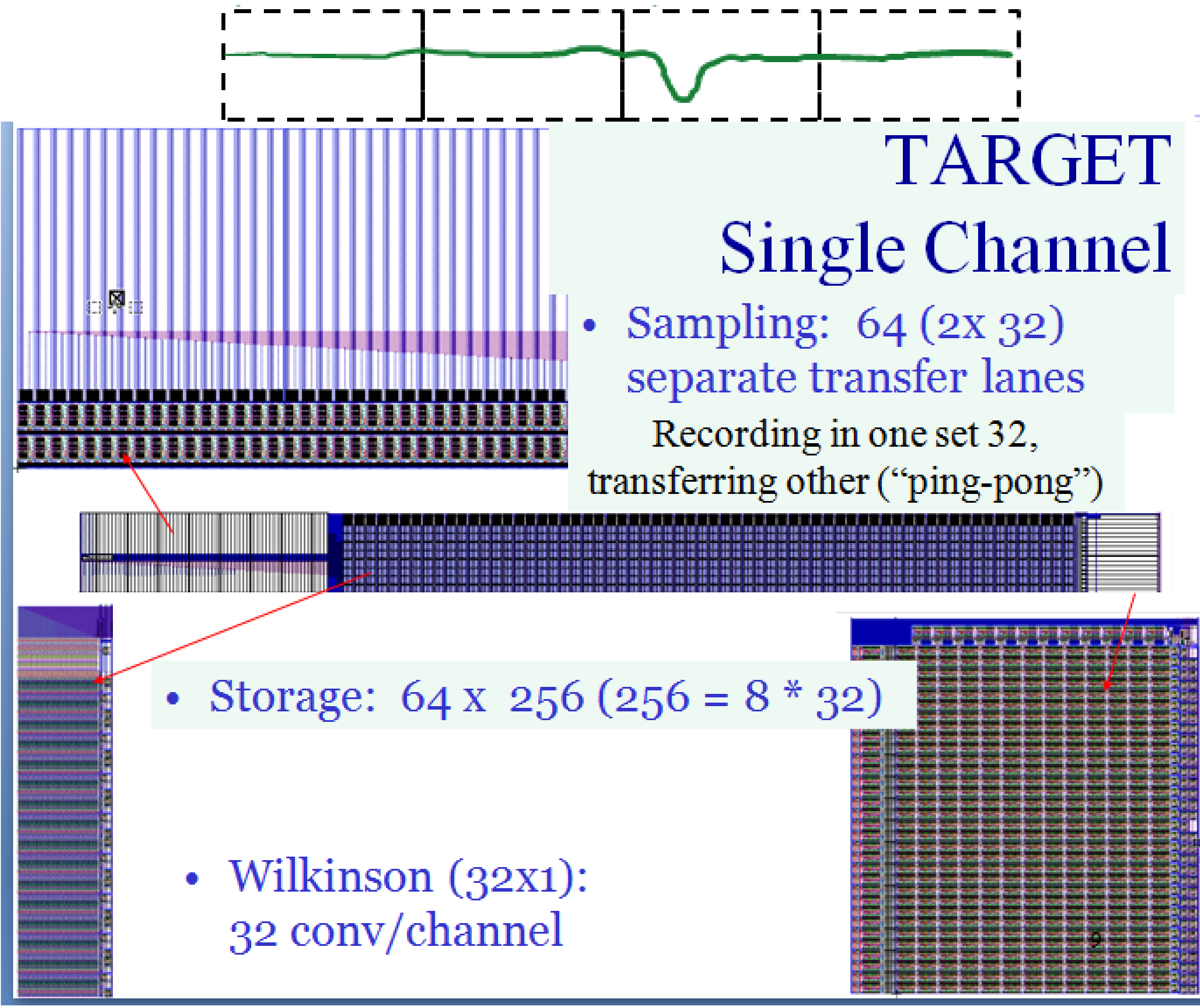
# The original application

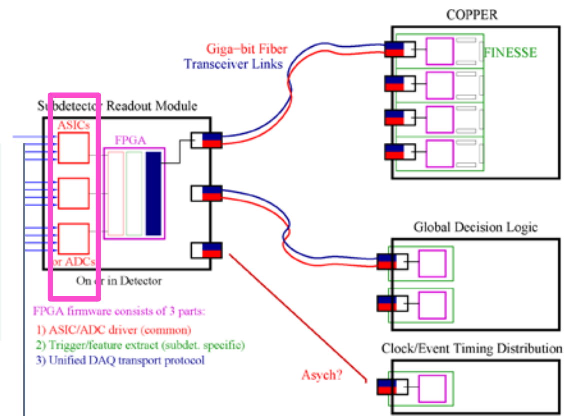



2,048 readout channels/ camera

CHEC design for CTA

# TARGET ASIC Overview

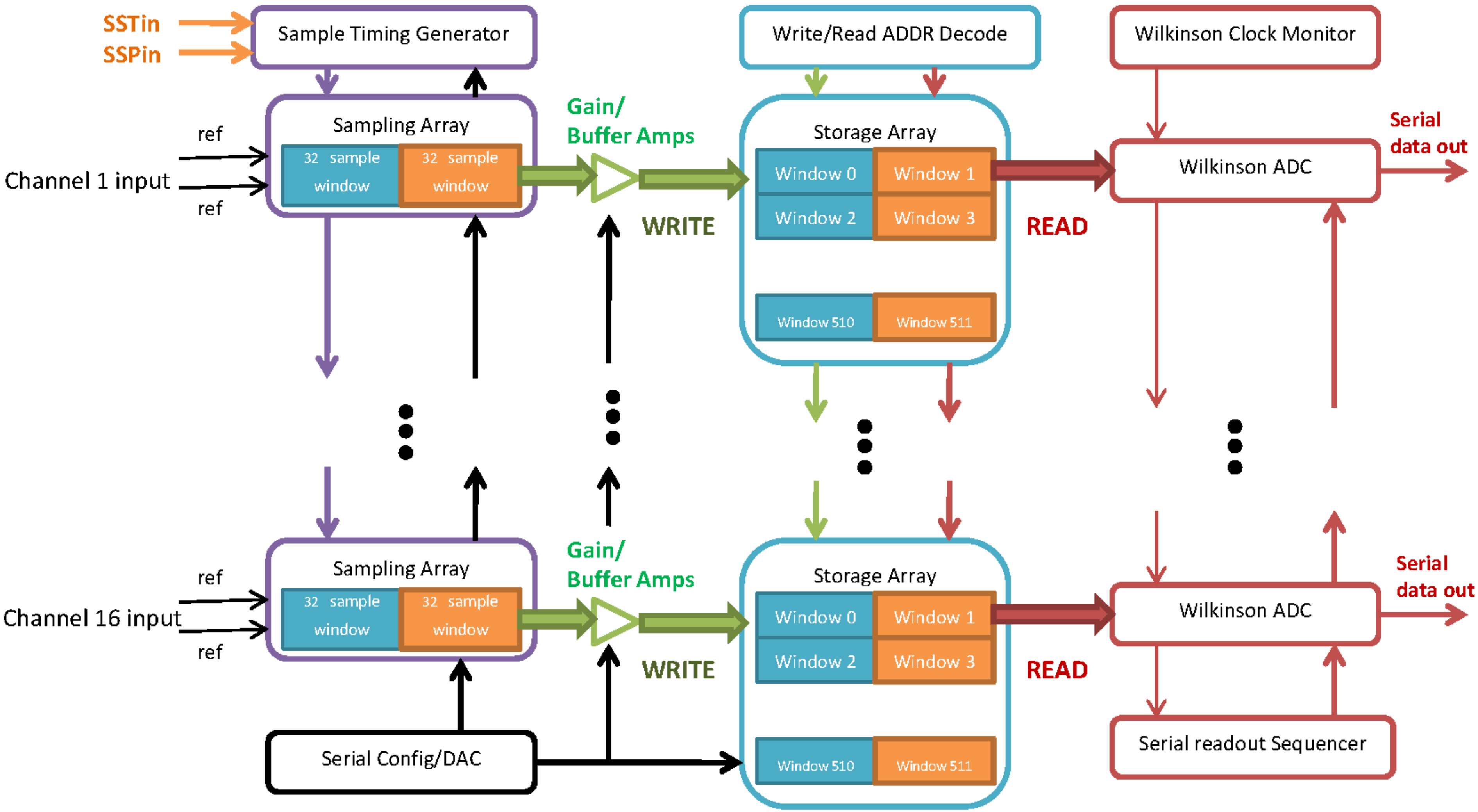



**Very similar to IRSx:**

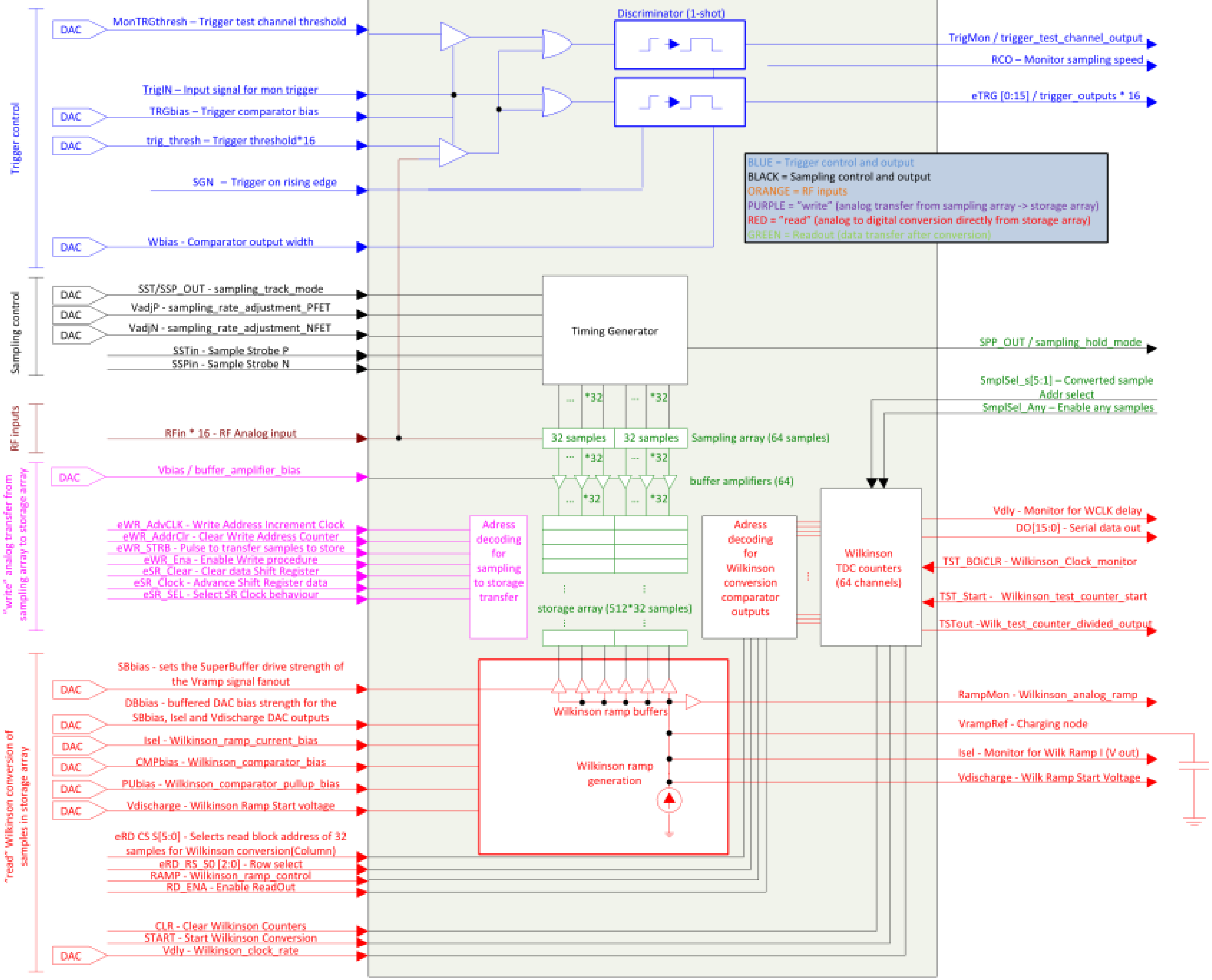
- Sampling aligned to SuperKEKB RF clock
- 2x more channels
- Sampling 3x slower
- No precision timing requirement

# TARGET ASIC



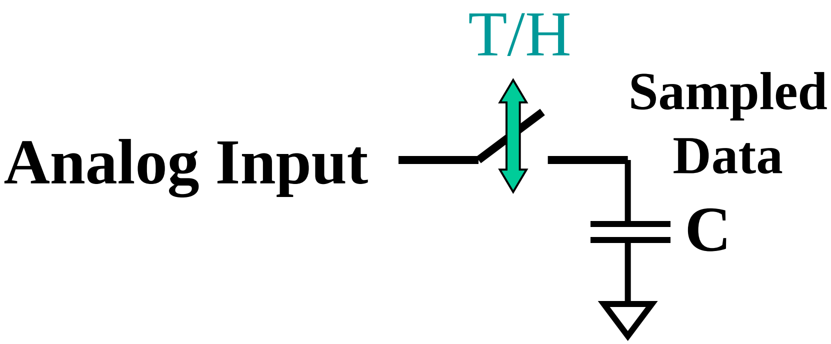
SSTin
SSPin
Sample Timing Generator
Write/Read ADDR Decode
Wilkinson Clock Monitor
Sampling Array
ref
Channel 1 input
ref
32 sample window
32 sample window
Gain/ Buffer Amps
WRITE
Storage Array
Window 0
Window 1
Window 2
Window 3
Window 510
Window 511
READ
Wilkinson ADC
Serial data out
Sampling Array
ref
Channel 16 input
ref
32 sample window
32 sample window
Gain/ Buffer Amps
WRITE
Storage Array
Window 0
Window 1
Window 2
Window 3
Window 510
Window 511
READ
Wilkinson ADC
Serial data out
Serial Config/DAC
Serial readout Sequencer

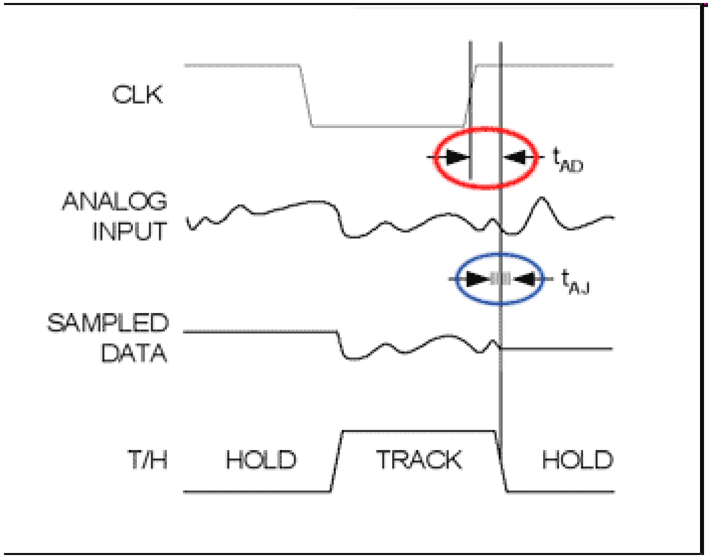
# TARGET Architecture



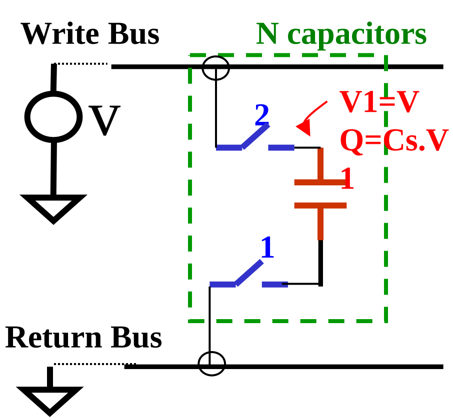
# Underlying Technology

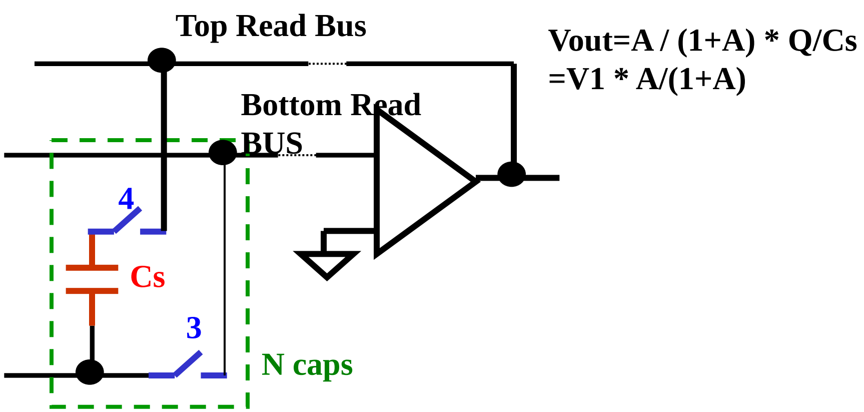
- Track and Hold (T/H)



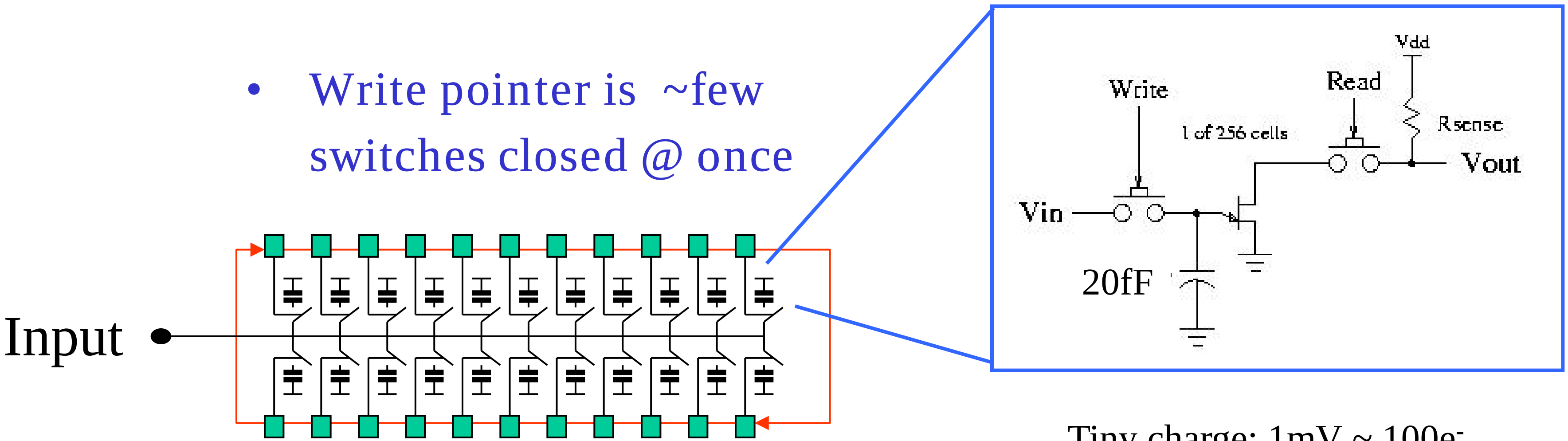

- Pipelined storage = array of T/H elements, with output buffering



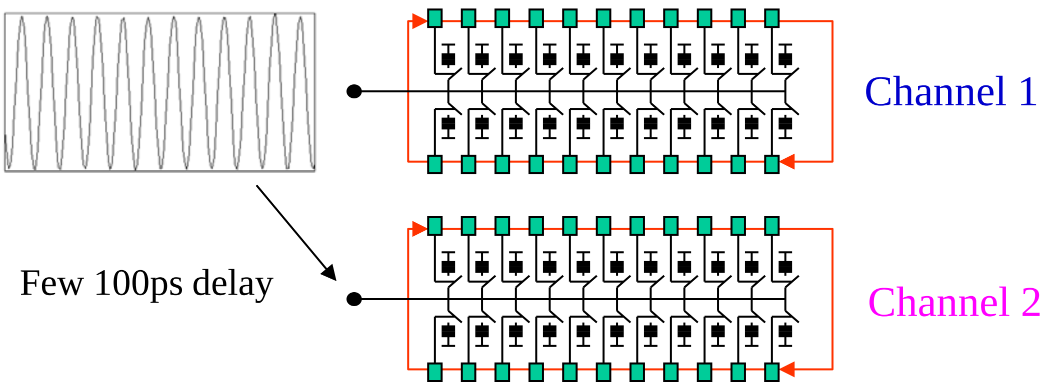



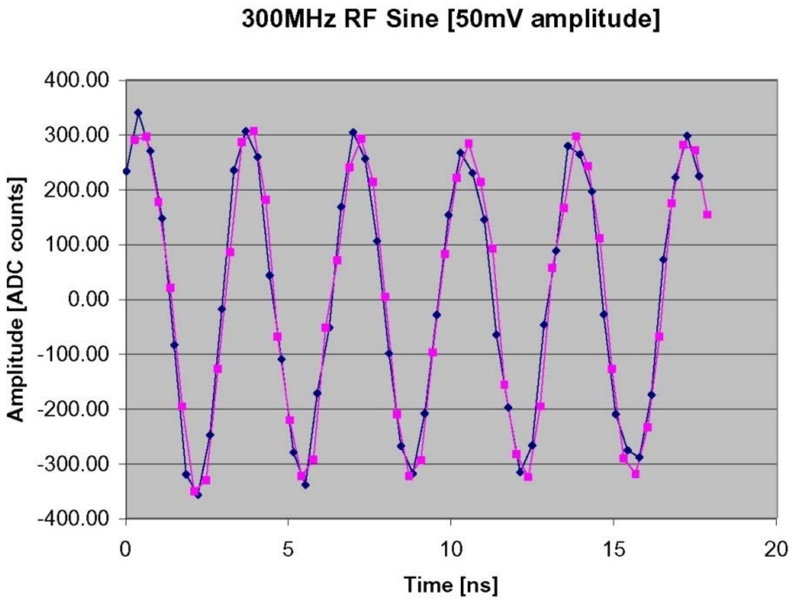
# Switched Capacitor Array Sampling

- Write pointer is ~few switches closed @ once




Tiny charge: 1mV ~ 100e-

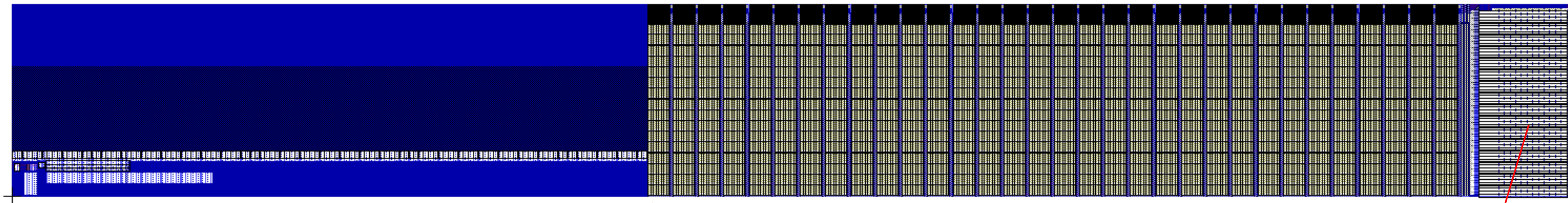


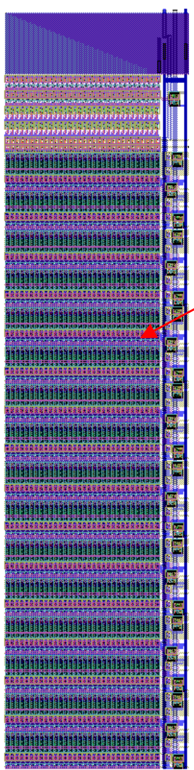



# TX Single Channel

- Sampling: 64 (2x 32) separate transfer lanes

Recording in one set 32, transferring other (“ping-pong”)



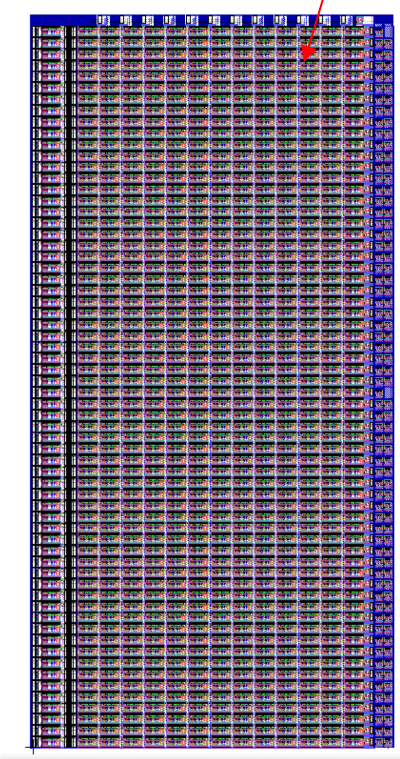


- “2-stage” transfer

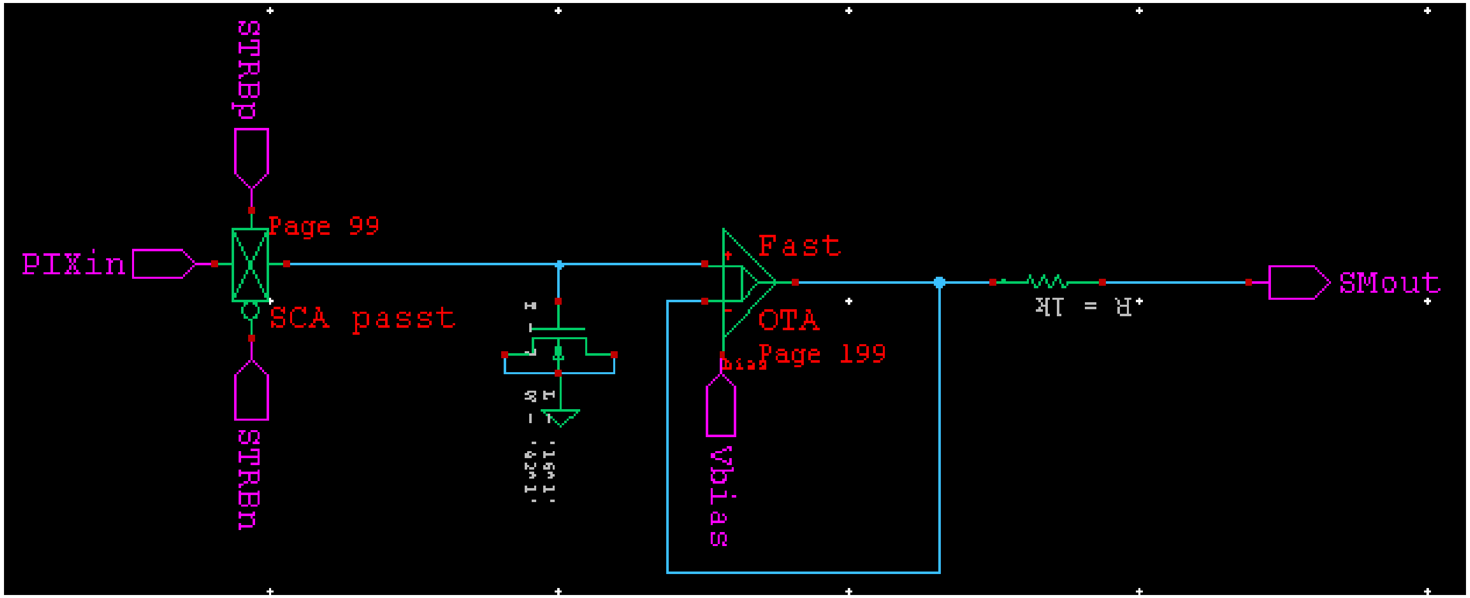
- Storage: 32 x 512 (16k samples)

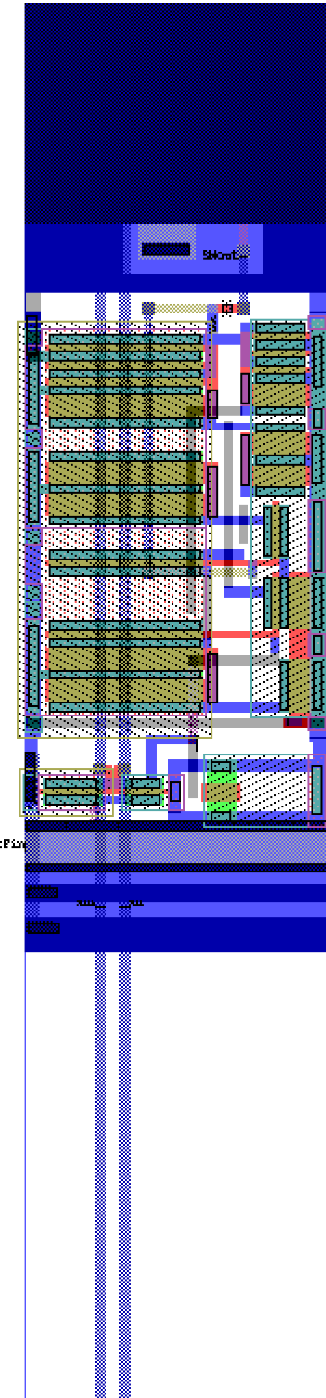
- Wilkinson (16 ch * 32x)

- 512 conv in parallel



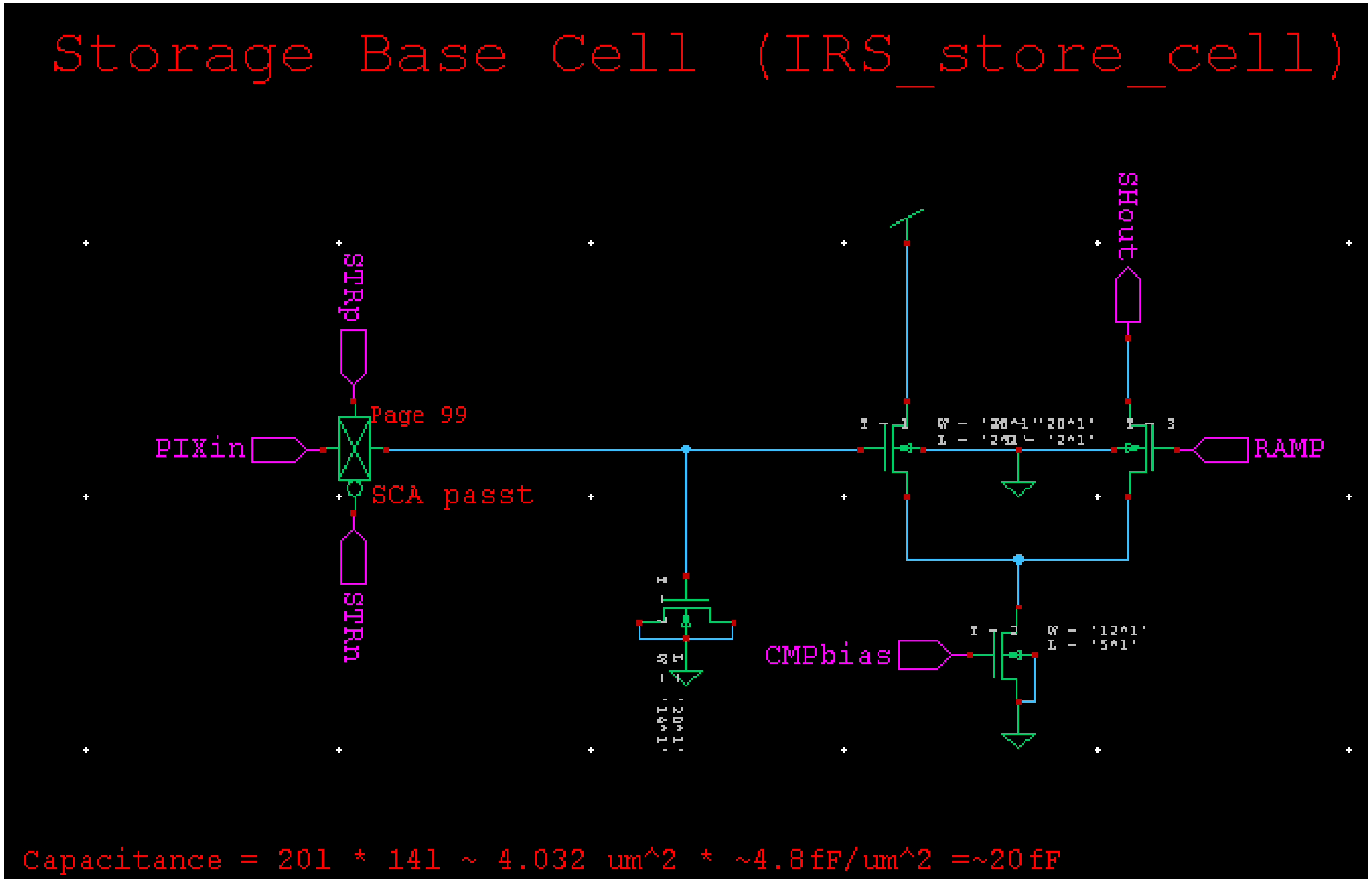
# TX Sample Cell

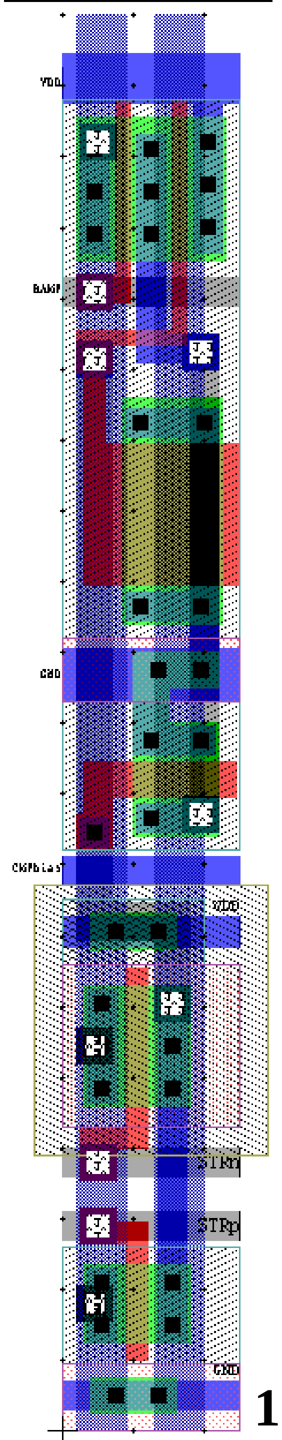


- Main element is buffer amp (OTA)
  - Relatively low current (10's uA) operation possible

# Storage Cell

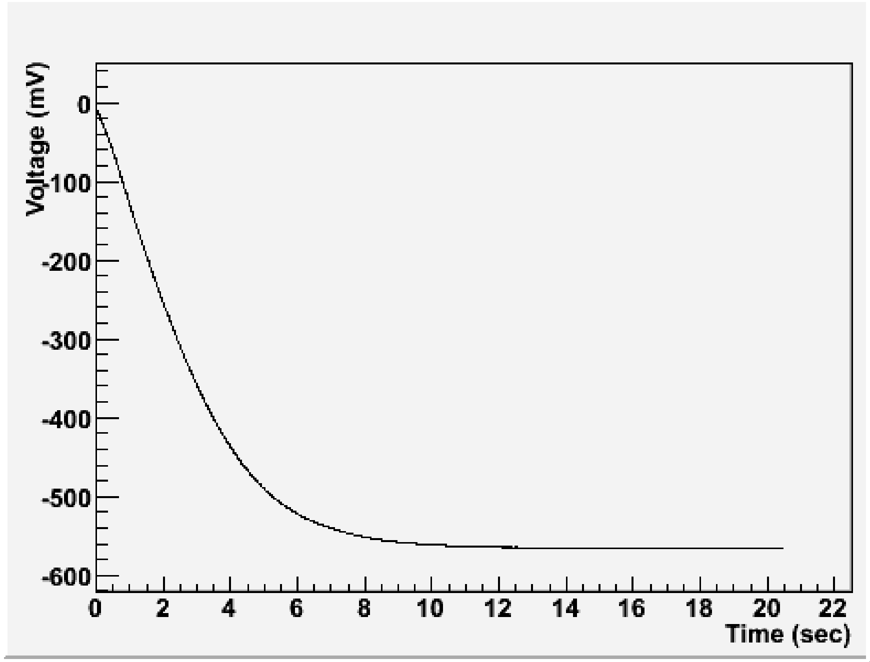


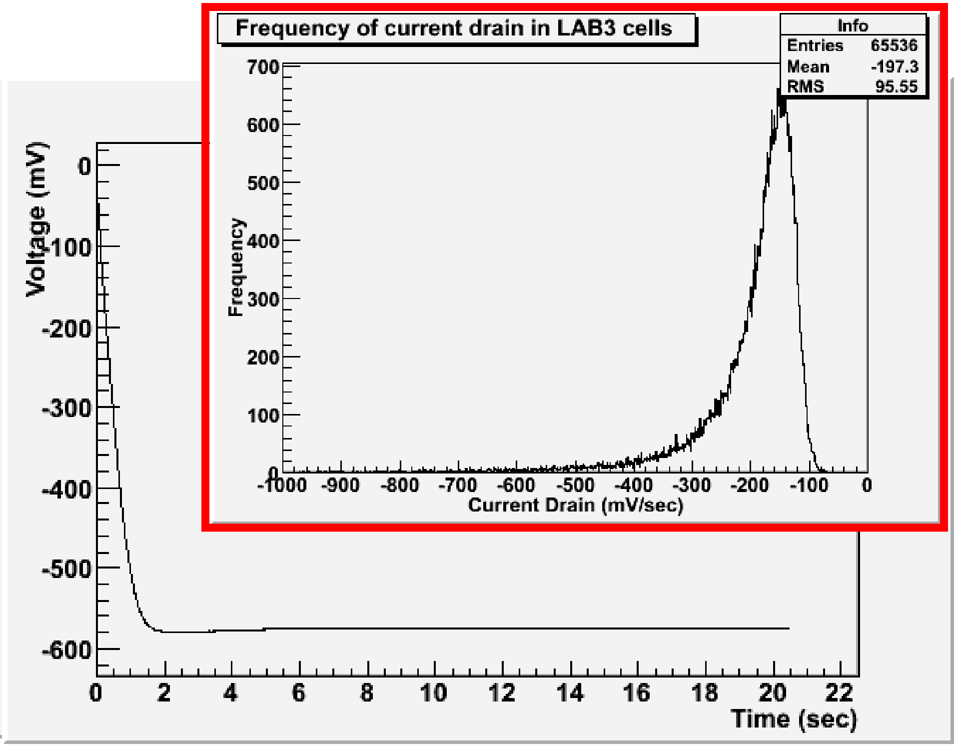




- Diff. Pair as comparator
  - Only power on selected block

# Competing Goals

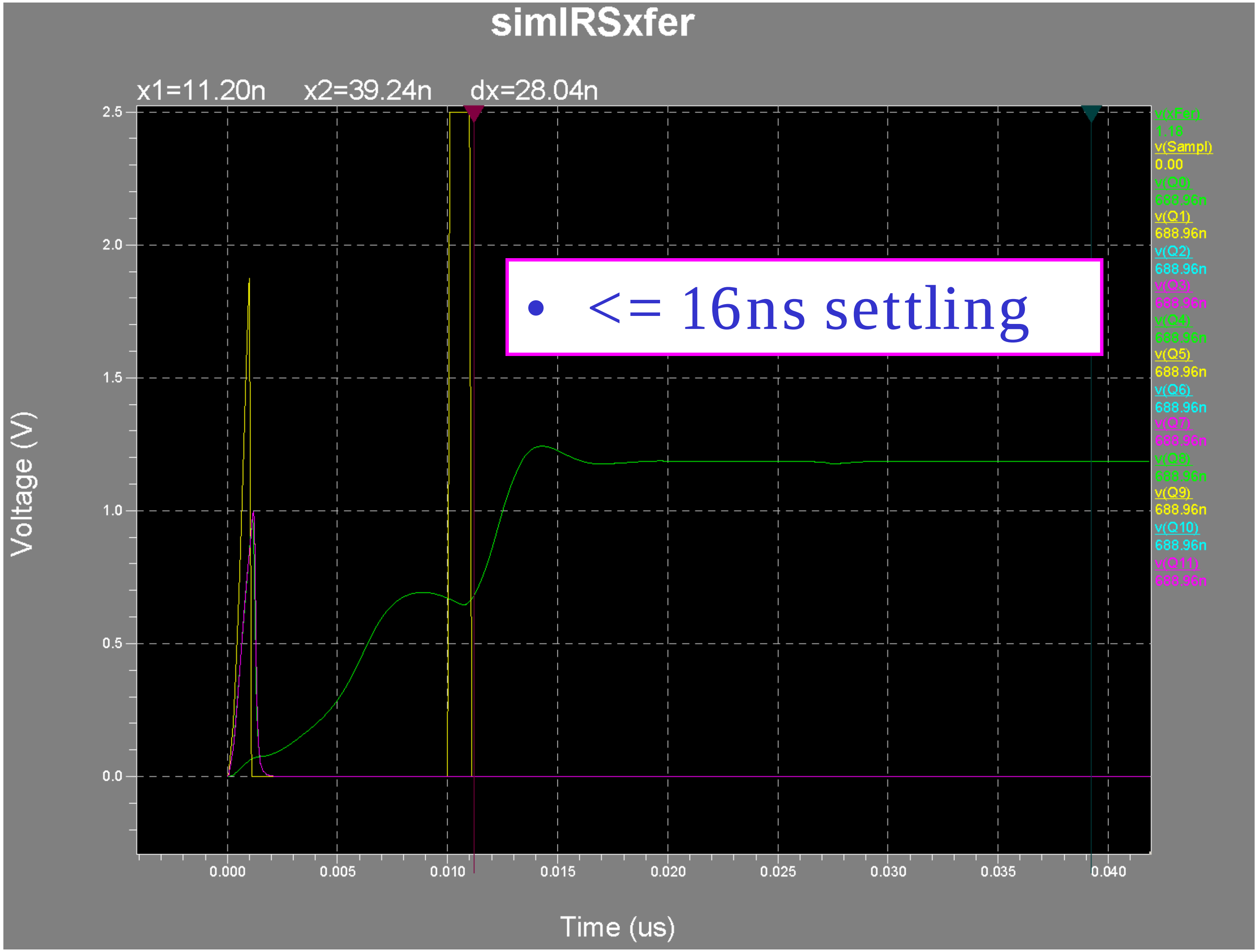
Need small C for
Dense Storage



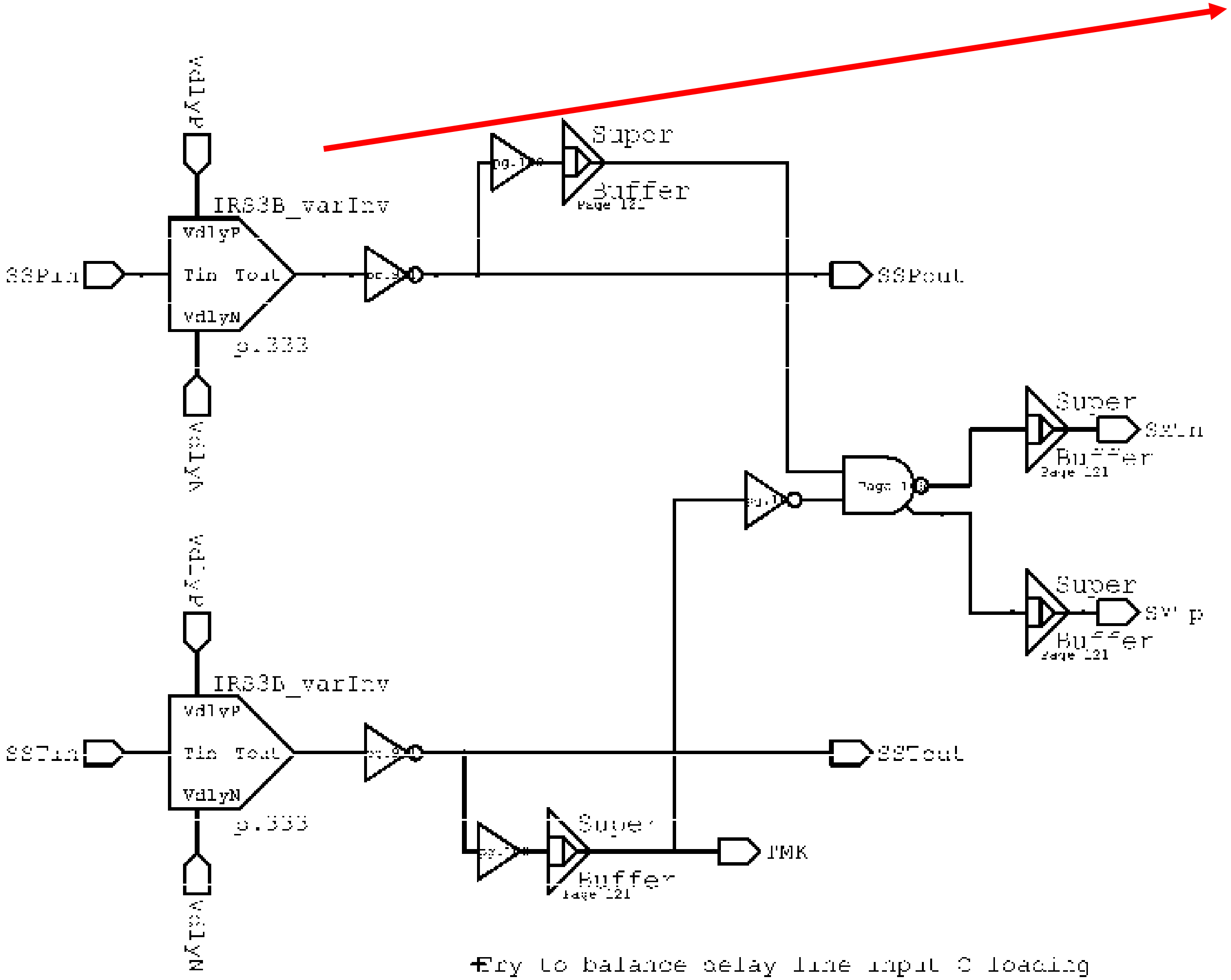

Sample channel-channel variation
~ fA leakage typically

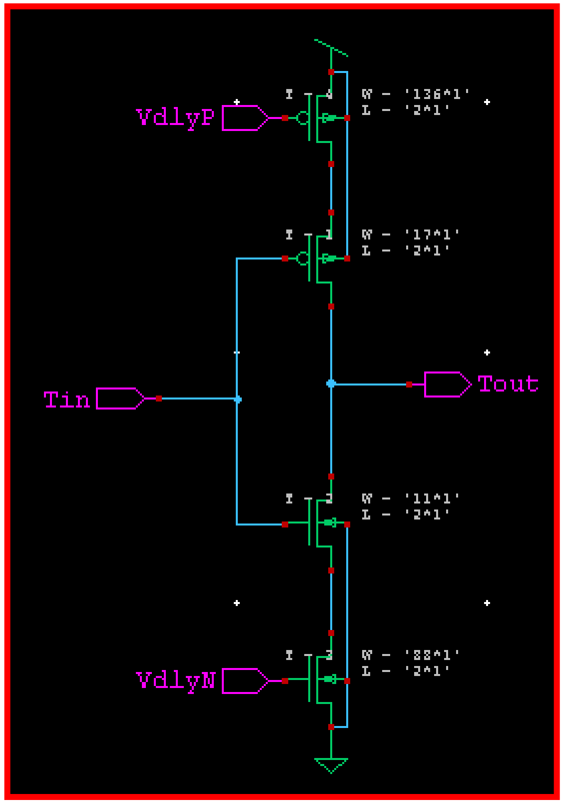
# Sample transfer – realistic capacitance




- 200Ω isolation resistor to reduce ringing

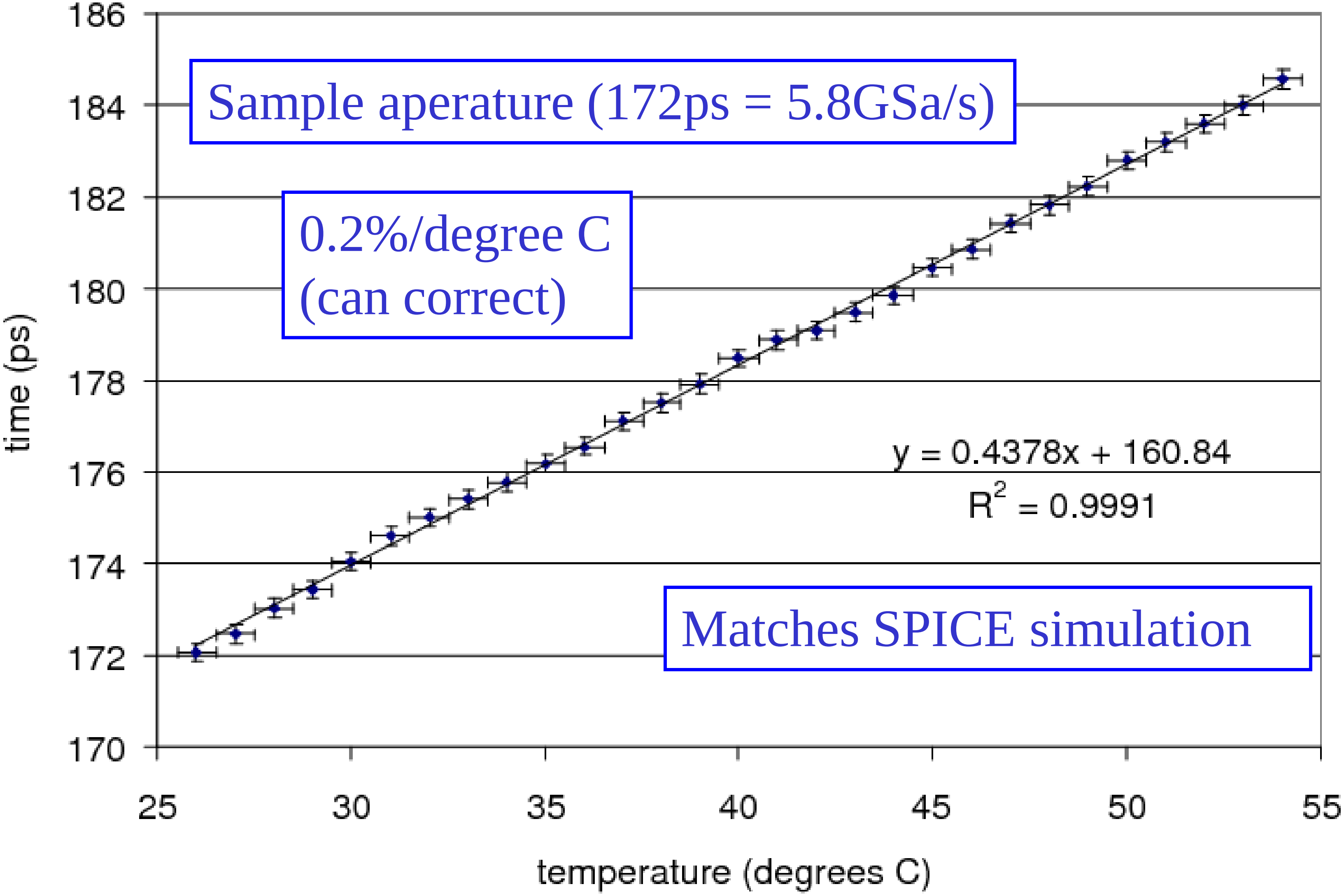
# Timebase Generator



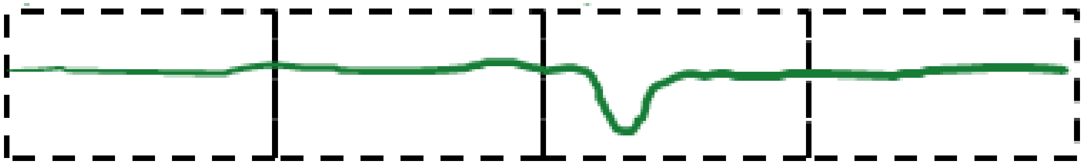



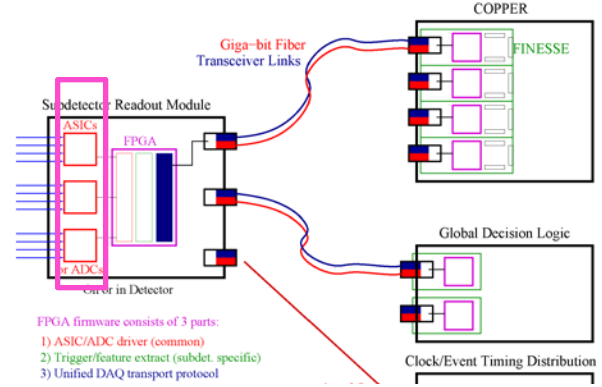

- Base delay

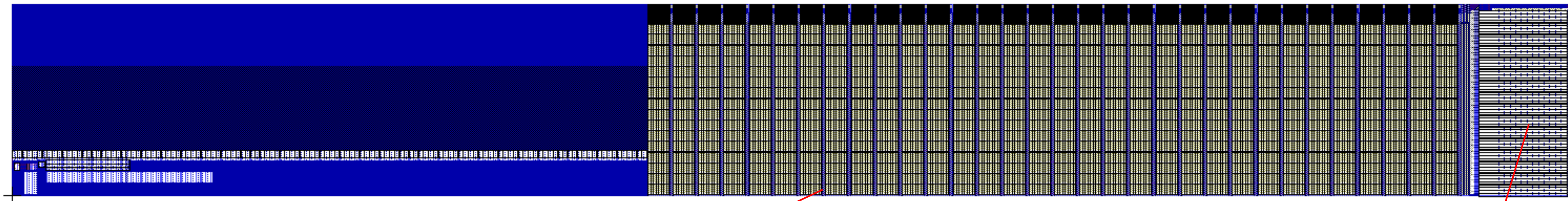
# Temperature Dependence

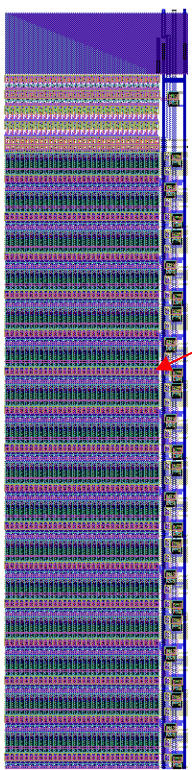


# Window stitching





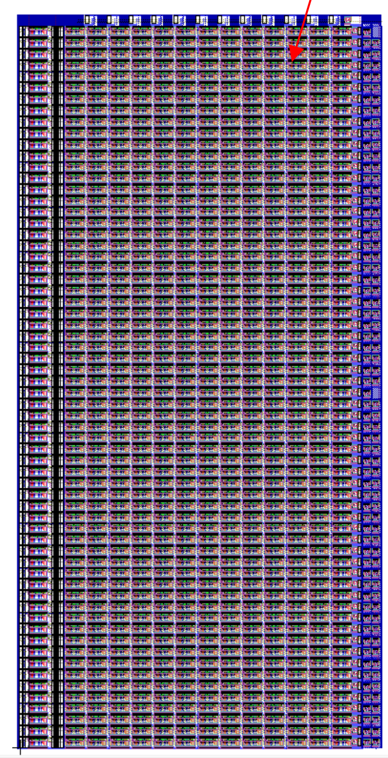





- Sampling: 128 (2x 64) separate transfer lanes

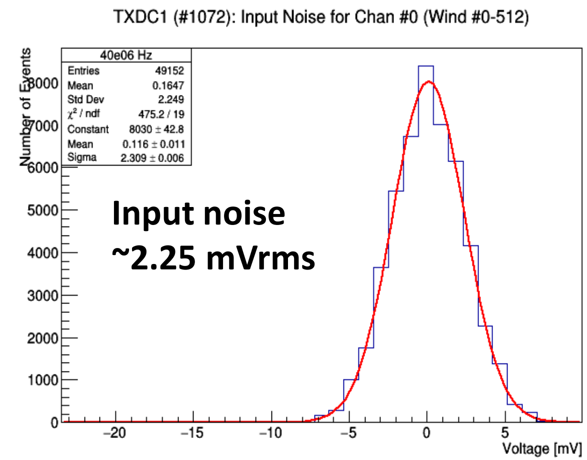
**Recording in one set 64, transferring other ("ping-pong")**

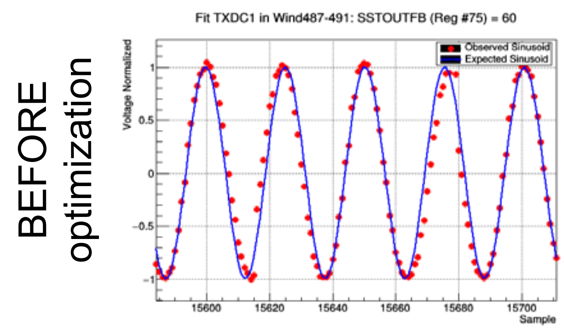
- Storage: 64 x 512 (32k per ch.)
  - Wilkinson ADC (64 at once)
  - 64 conv/channel (512 in parallel)

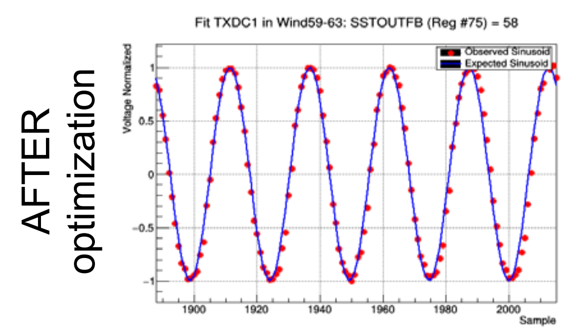


# Test protocols

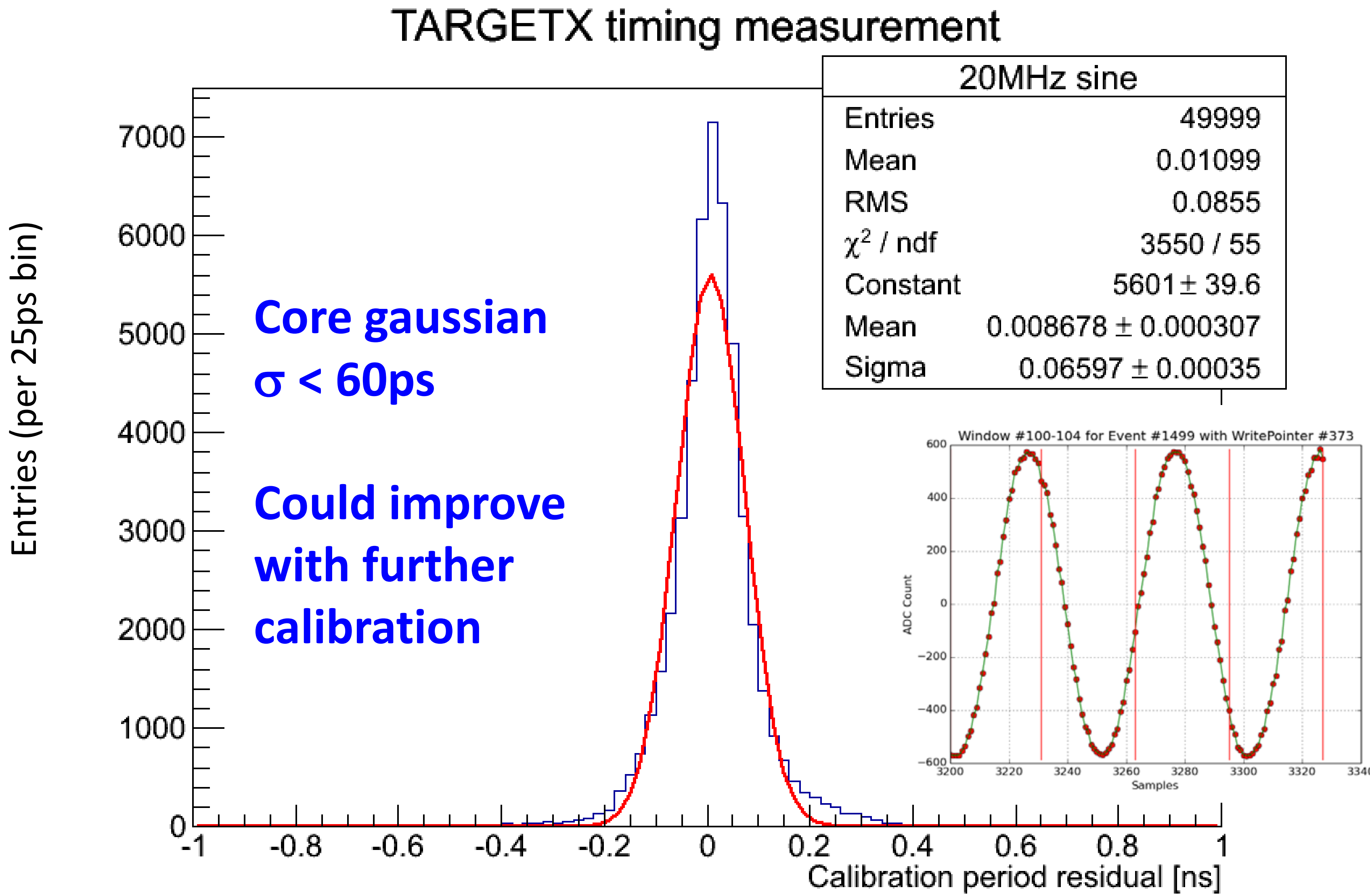
- TargetX verification
  - Noise test, pedestal test
  - All samples, windows operational
  - Timing calibration for best performance
    - 40MHz sine input @ 600mVpp
    - Per chip scan of Delay Lock Loop feedback
- Analog Front-end
  - MPPC bias test
  - Preamplifier carrier temperature readout
  - Trigger threshold scan
  - Waveform sampling triggered by MPPCs



# Timing Improvement




**Core gaussian**
**σ < 60ps**

**Could improve with further calibration**

| PCLK # | | | | |
|---|---|---|---|---|
| 1 | Trigger Threshold | Ch. 1 | | |
| 2 | Wbias | Ch. 1 | | |
| 3 | Trigger Threshold | Ch. 2 | | |
| 4 | Wbias | Ch. 2 | | |
| 5 | Trigger Threshold | Ch. 3 | | |
| 6 | Wbias | Ch. 3 | | |
| 7 | Trigger Threshold | Ch. 4 | | |
| 8 | Wbias | Ch. 4 | | |
| 9 | Trigger Threshold | Ch. 5 | | |
| 10 | Wbias | Ch. 5 | | |
| 11 | Trigger Threshold | Ch. 6 | | |
| 12 | Wbias | Ch. 6 | | |
| 13 | Trigger Threshold | Ch. 7 | | |
| 14 | Wbias | Ch. 7 | | |
| 15 | Trigger Threshold | Ch. 8 | | |
| 16 | Wbias | Ch. 8 | | |
| 17 | Trigger Threshold | Ch. 9 | | |
| 18 | Wbias | Ch. 9 | | |
| 19 | Trigger Threshold | Ch. 10 | | |
| 20 | Wbias | Ch. 10 | | |
| 21 | Trigger Threshold | Ch. 11 | | |
| 22 | Wbias | Ch. 11 | | |
| 23 | Trigger Threshold | Ch. 12 | | |
| 24 | Wbias | Ch. 12 | | |
| 25 | Trigger Threshold | Ch. 13 | | |
| 26 | Wbias | Ch. 13 | | |
| 27 | Trigger Threshold | Ch. 14 | | |
| 28 | Wbias | Ch. 14 | | |
| 29 | Trigger Threshold | Ch. 15 | | |
| 30 | Wbias | Ch. 15 | | |
| 31 | Trigger Threshold | Ch. 16 | | |
| 32 | Wbias | Ch. 16 | | |
| 33 | unused (T7 legacy) | Ch.1-4 | | |
| 34 | unused (T7 legacy) | Ch.1-4 | | |
| 35 | unused (T7 legacy) | Ch.1-4 | | |
| 36 | unused (T7 legacy) | Ch.1-4 | | |
| 37 | unused (T7 legacy) | Ch.5-8 | | |
| 38 | unused (T7 legacy) | Ch.5-8 | | |
| 39 | unused (T7 legacy) | Ch.5-8 | | |
| 40 | unused (T7 legacy) | Ch.5-8 | | |
| 41 | unused (T7 legacy) | Ch.9-12 | | |
| 42 | unused (T7 legacy) | Ch.9-12 | | |
| 43 | unused (T7 legacy) | Ch.9-12 | | |
| 44 | unused (T7 legacy) | Ch.9-12 | | |
| 45 | unused (T7 legacy) | Ch.13-16 | | |
| 46 | unused (T7 legacy) | Ch.13-16 | | |
| 47 | unused (T7 legacy) | Ch.13-16 | | |
| 48 | unused (T7 legacy) | Ch.13-16 | | |
| 49 | Sbbias | Vramp | Dbbias | |
| 50 | Vdisch | Vramp | Dbbias | |
| 51 | Isel | Vramp | Dbbias | |
| 52 | Dbbias | Vramp | | |
| 53 | Qbias | PLL | Vqbuff | |
| 54 | Vqbuff | PLL | | |
| 55 | VtrimT | PLL | Vqbuff | |
| 56 | Misc Digital Reg | | 12 bit | |
| 57 | VadjP | Timebase | VAPbuff | |
| 58 | VAPbuff | Timebase | | |
| 59 | VadjN | Timebase | VANbuff | |
| 60 | VANbuff | Timebase | | |
| 61 | unused (T7 legacy) | Trigger | Itbias | |
| 62 | Vbias | Trigger | Itbias | |
| 63 | TRGGbias | Trigger | Itbias | |
| 64 | Itbias | Trigger | | |
| 65 | SSPin LE | Timebase | | 8 bit time |
| 66 | SSPin TE | Timebase | | 8 bit time |
| 67 | WR_ADDR_Incr1 LE | Timebase | | 8 bit time |
| 68 | WR_ADDR_Incr1 TE | Timebase | | 8 bit time |
| 69 | WR_STRB1 LE | Timebase | | 8 bit time |
| 70 | WR_STRB1 TE | Timebase | | 8 bit time |
| 71 | WR_ADDR_Incr2 LE | Timebase | | 8 bit time |
| 72 | WR_ADDR_Incr2 TE | Timebase | | 8 bit time |
| 73 | WR_STRB2 LE | Timebase | | 8 bit time |
| 74 | WR_STRB2 TE | Timebase | | 8 bit time |
| 75 | MonTiming SEL | Timebase | | 8 bit time |
| 76 | SSToutFB | Timebase | | 8 bit time |
| 77 | CMPbias2 | Wilk | Sbbias | |
| 78 | Pubias | Wilk | Sbbias | |
| 79 | CMPbias | Wilk | Sbbias | |
| 80 | TPGreg | | | 12 bit pattern |

**Hopefully, these will start to make sense in terms of how these settings map onto operational parameters of the TARGETX**

# Timebase Control

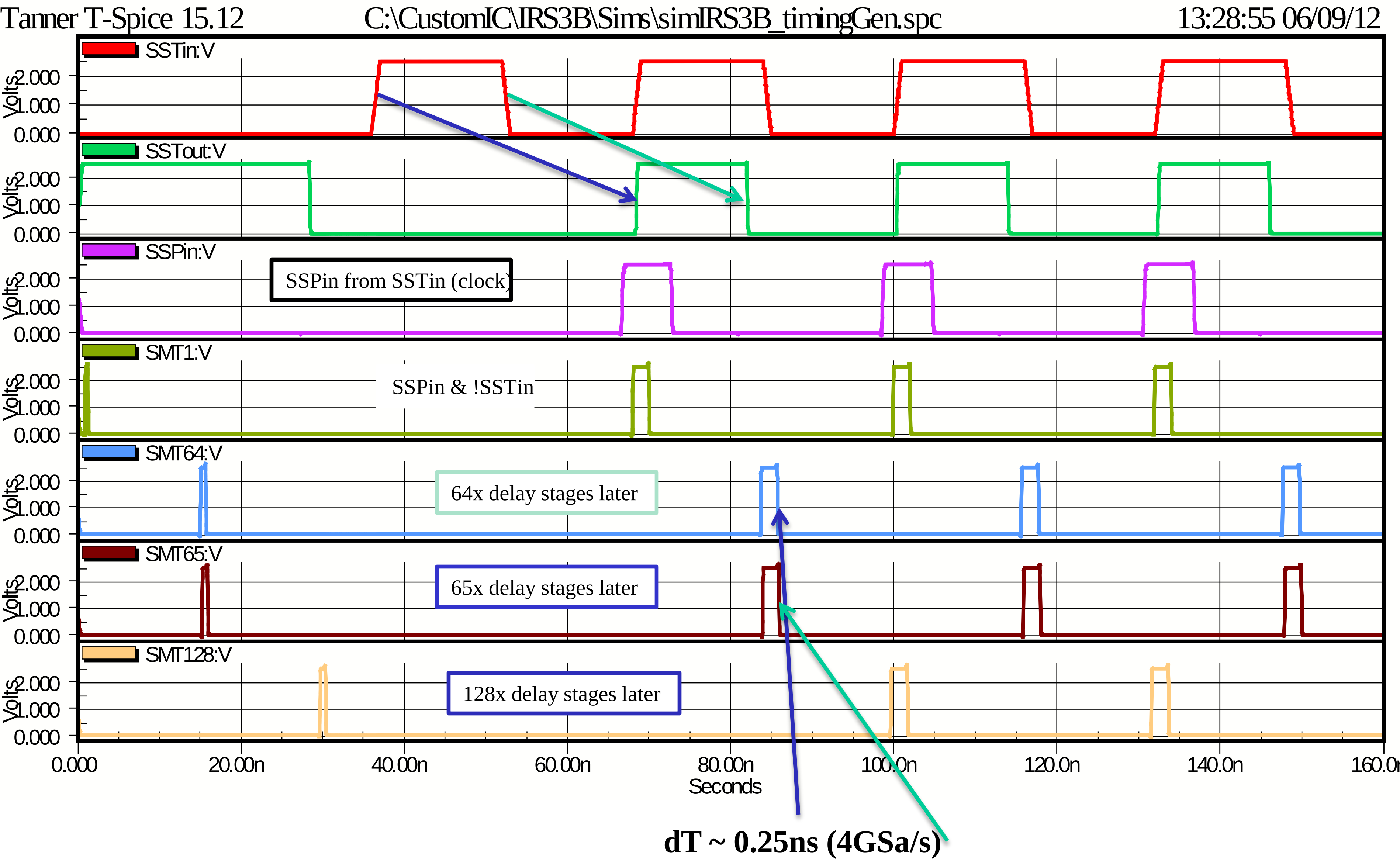
➔ Use copies of the Sample Strobe signals (from voltage-controlled delay line) to synthesize all critical internal timing signals **[difficult to fine-tune in firmware]**

➔ All driven from 1 precision time clock (SSTin – which is a copy of the system clock) **[why this clock MUST be clean/stable]**

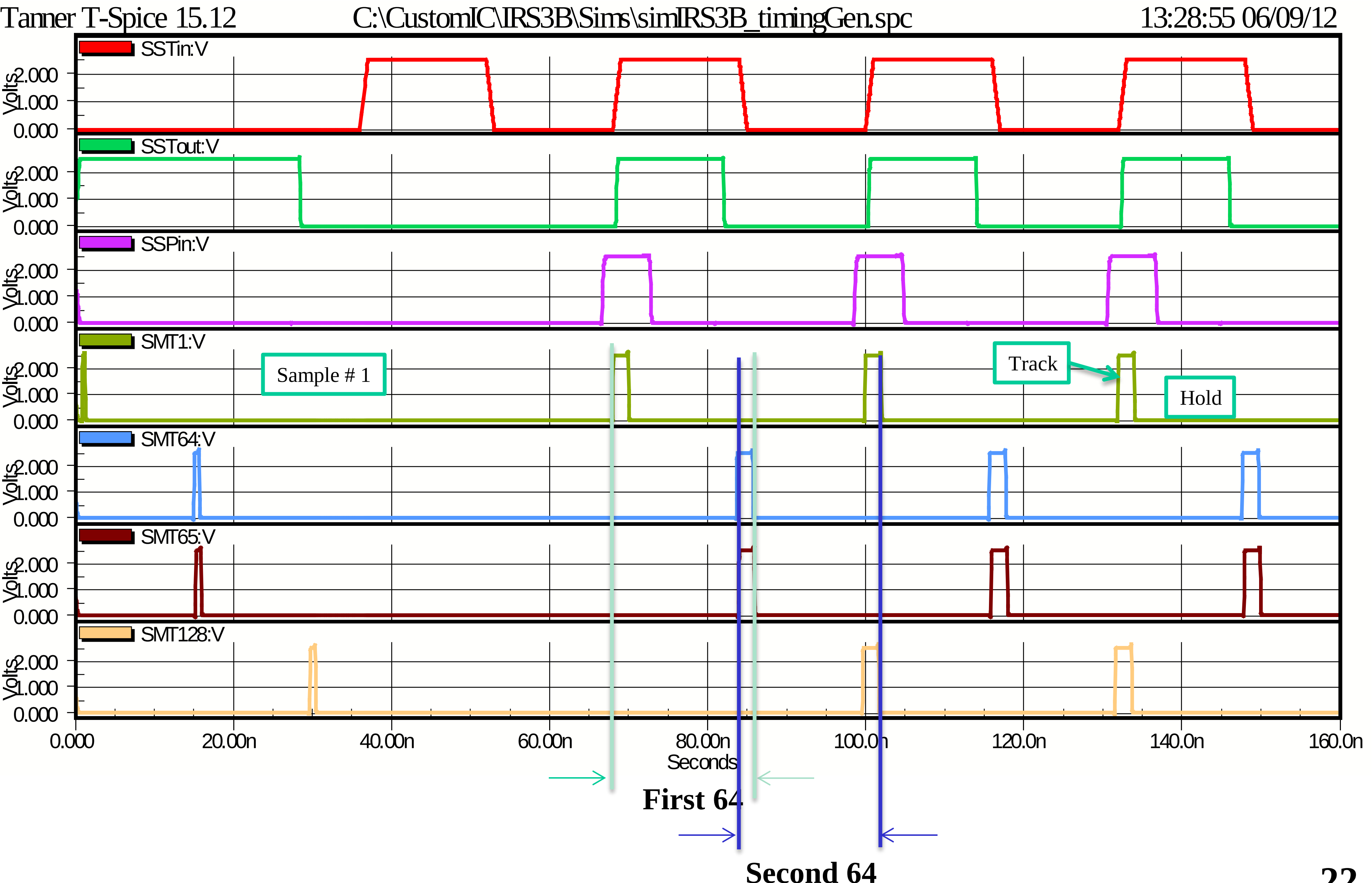
Specifically, can adjust with ns resolution:

- SSPin (Sample strobe width)
- WR_STRB – phase and width of analog transfer to storage array
- All timing signals MUXed out for monitoring

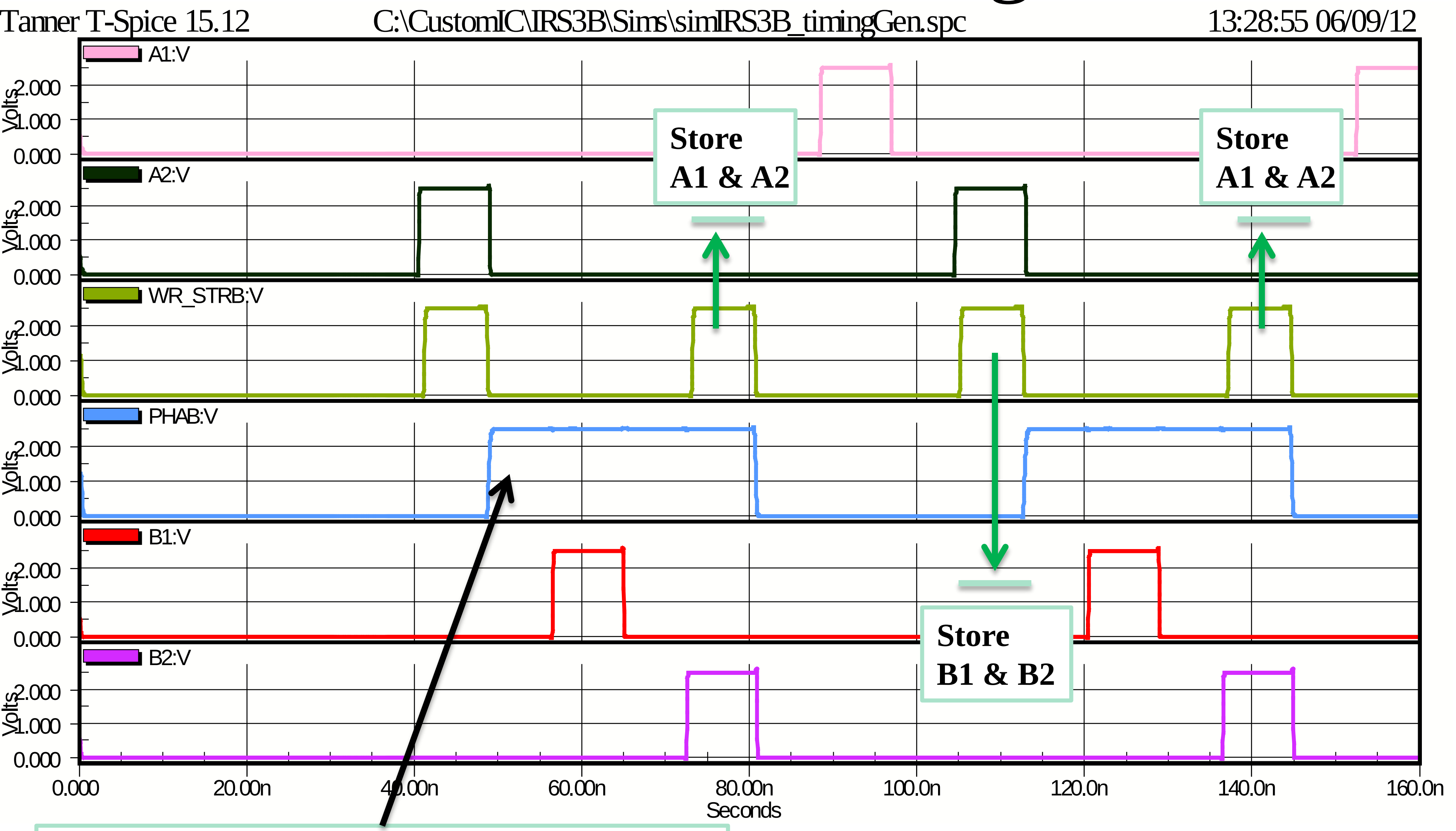
# Sample Timebase Generation



# Sampling Active



# Transfer to Storage



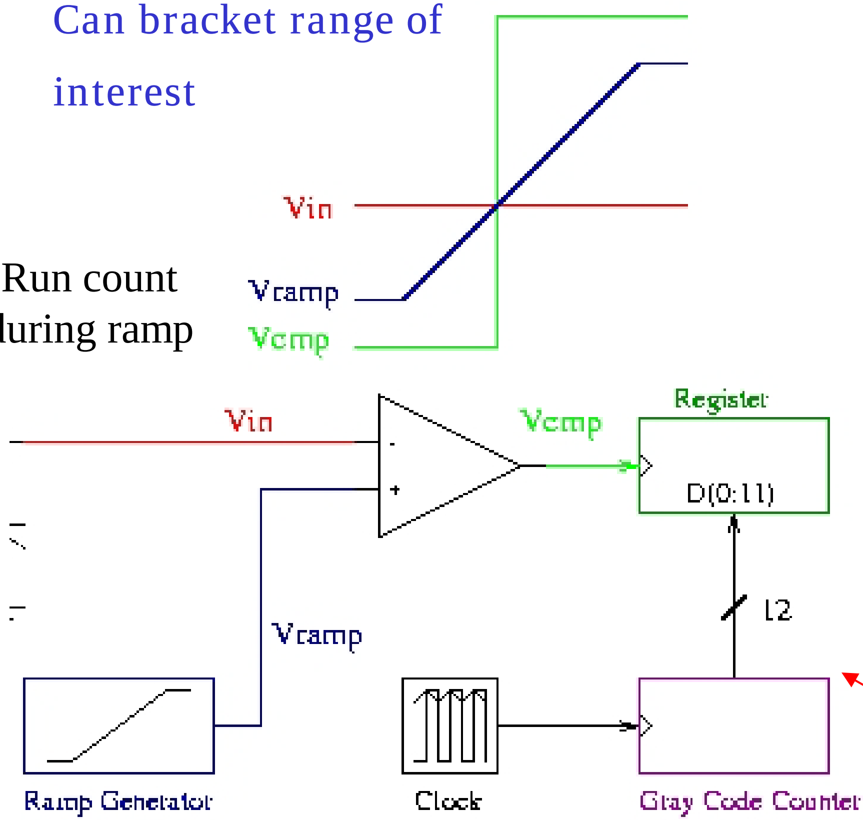

**Monitor PHAB to choose WR ADDR to Assert**
**(just need once after reset/reprogram)**

# Analog to Digital Conv

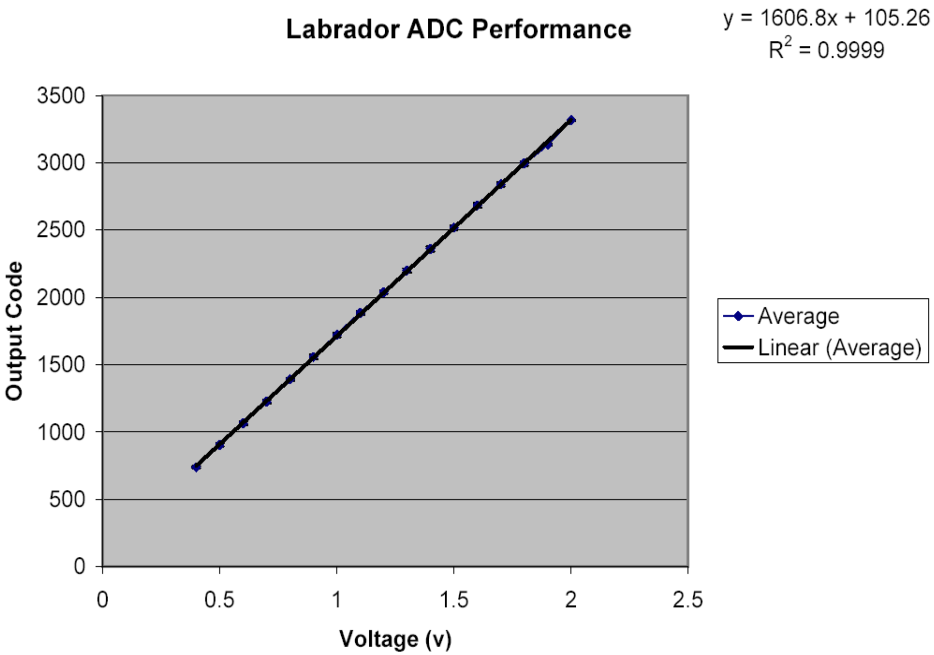
## Wilkinson ADC

- No missing codes
- Linearity as good as can make ramp
- Can bracket range of interest

Run count during ramp



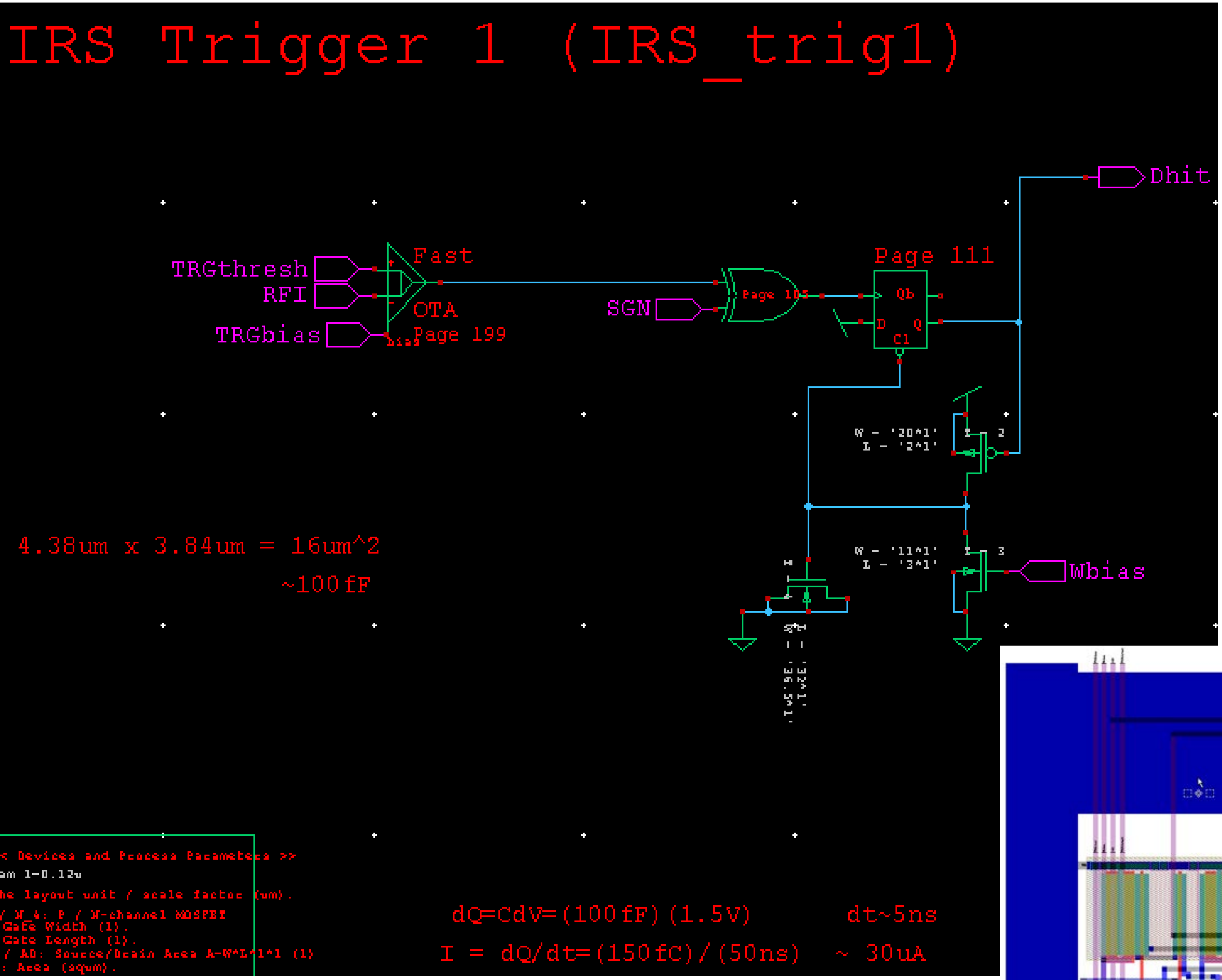

12-bit ADC

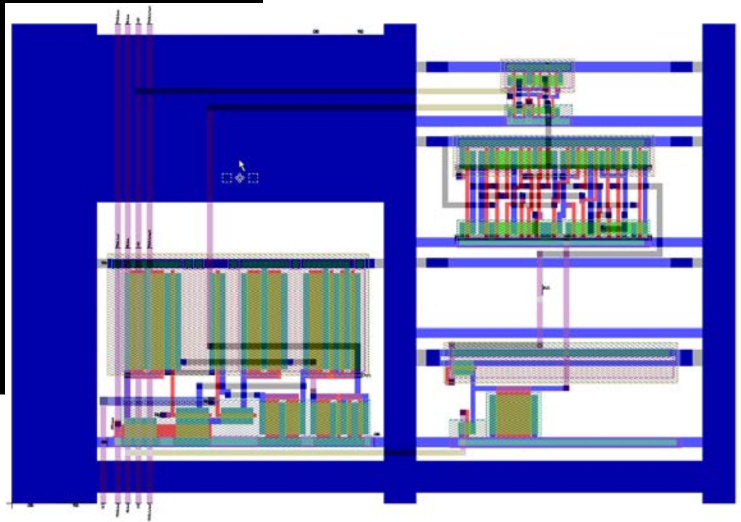



Modified! (self-counter) [~0.7 GHz]

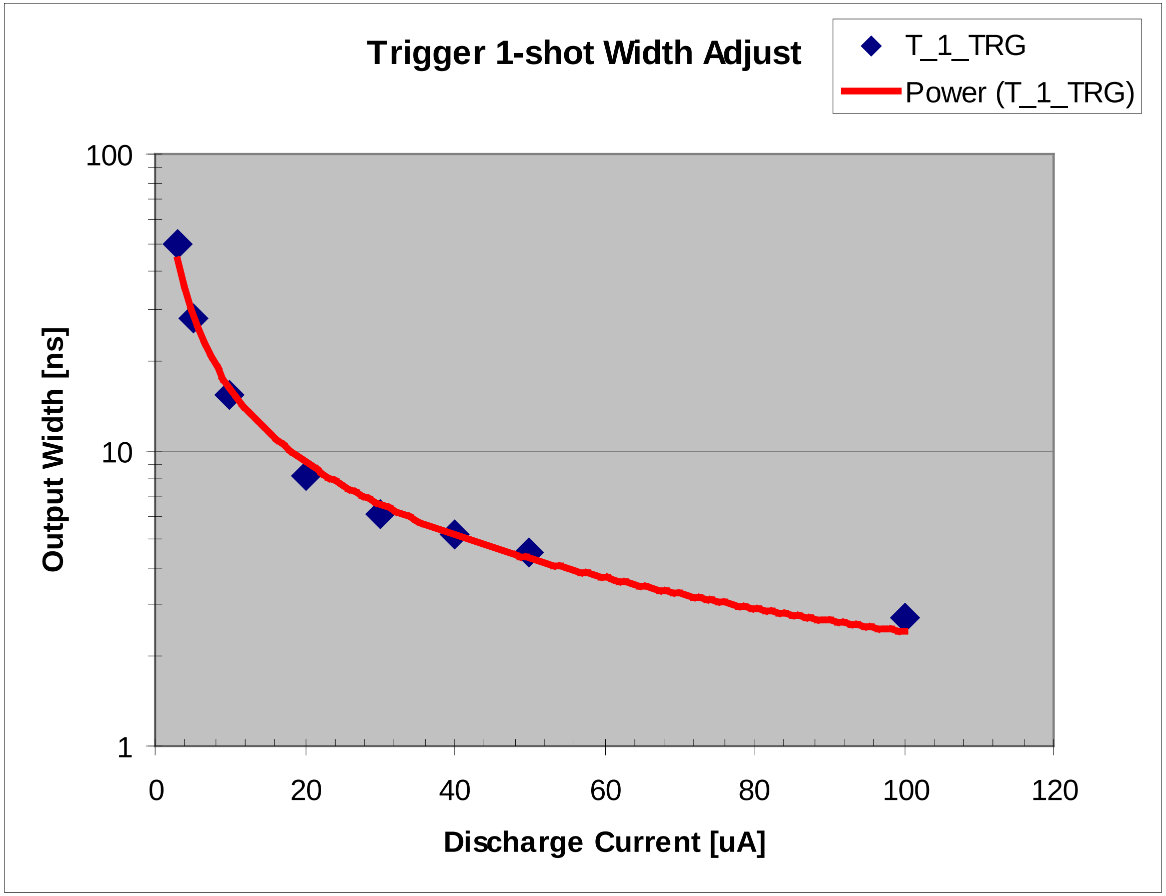
- Excellent linearity
- Basically as good as can make current source/comparator
- Comparator ~0.4 – 2.1V; ~700MHz GCC max

# Triggering


IRS Trigger 1 (IRS_trig1)
Dhit
Fast
OTA
Page 199
TRGthresh
RFI
TRGbias
SGN
Page 111
Qb
D
Q
C1
W = '20*1'
L = '2*1'
W = '11*1'
L = '3*1'
Wbias
4.38um x 3.84um = 16um^2
~100fF
dQ=CdV=(100fF)(1.5V)
dt~5ns
I = dQ/dt=(150fC)/(50ns)
~ 30uA



# Triggering – Tunable over a wide range




- IRS3B 1-size (Wbias) fits all (temp dependence only important for wide pulses)

# For next Monday

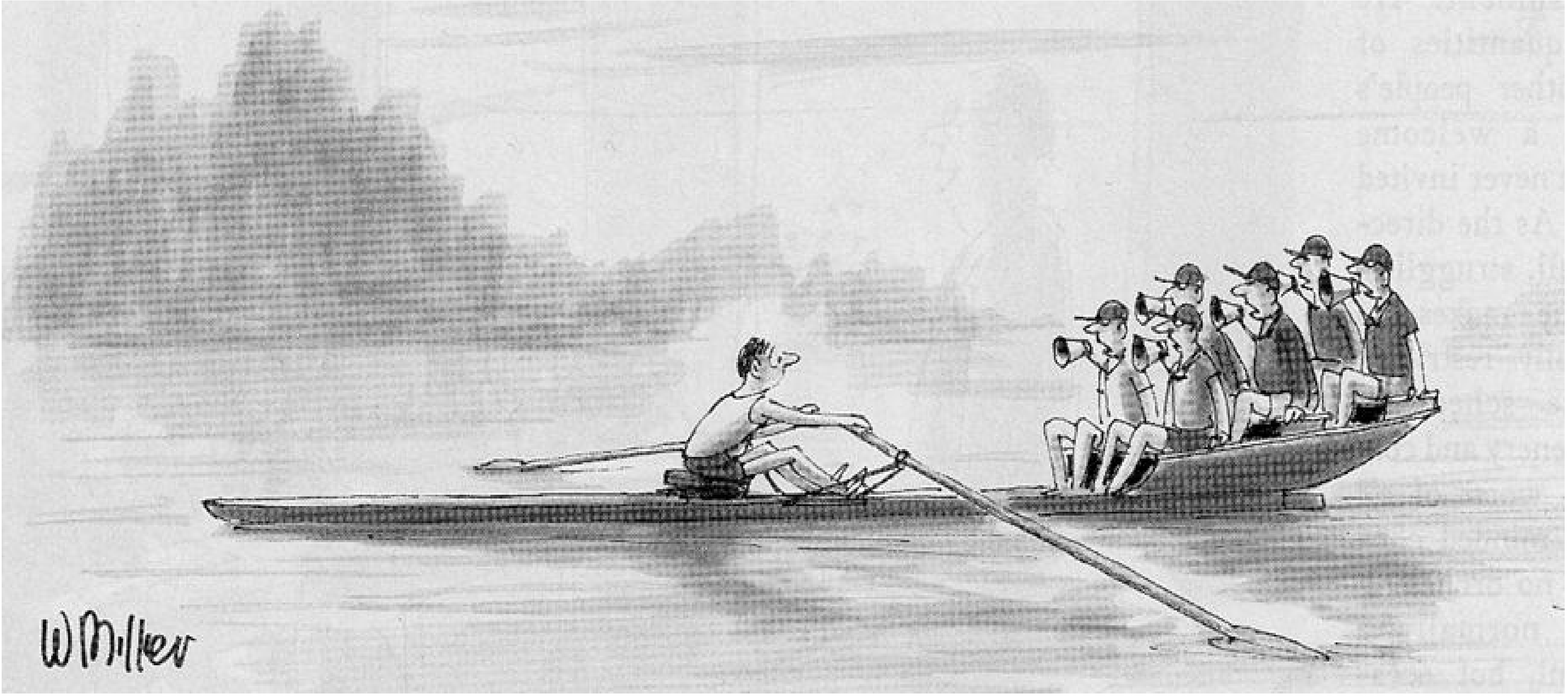
➔ Please come up with a set of your questions, to go over in more detail

➔ Much more pedagogical information pulled together for IRS familty, but want to do similar for TARGETX (responses to questions raised)

Important items to be characterized:

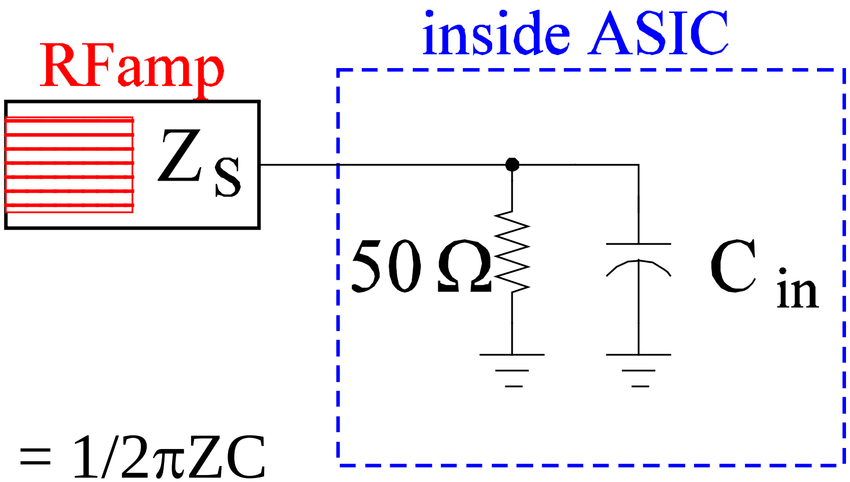
- Analog bandwidth
- Noise/ADC performance
- Cross-talk and further timing stability

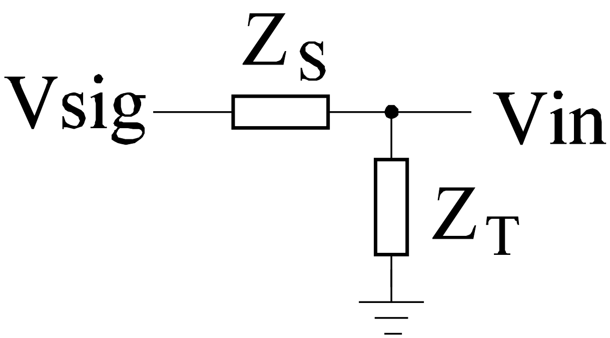
# Back-up slides



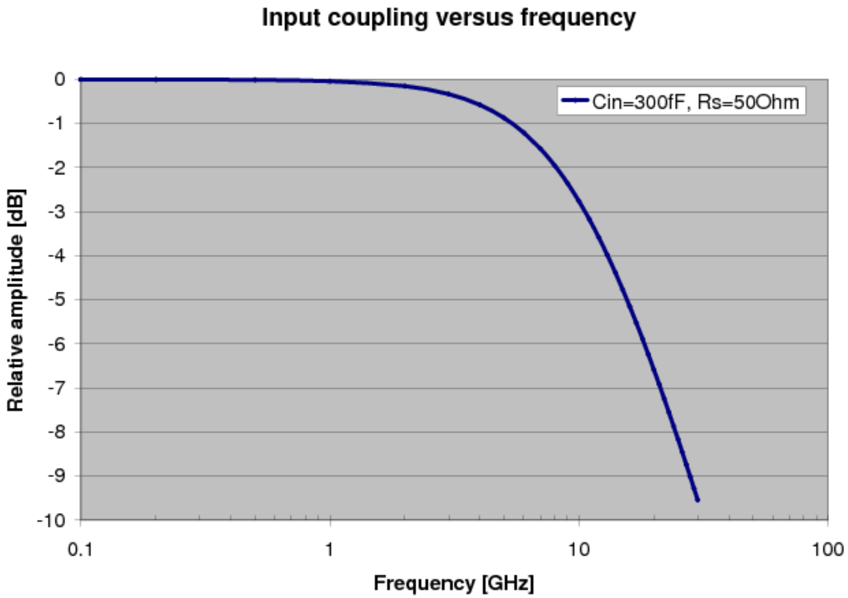
# Constraint 1: Analog Bandwidth

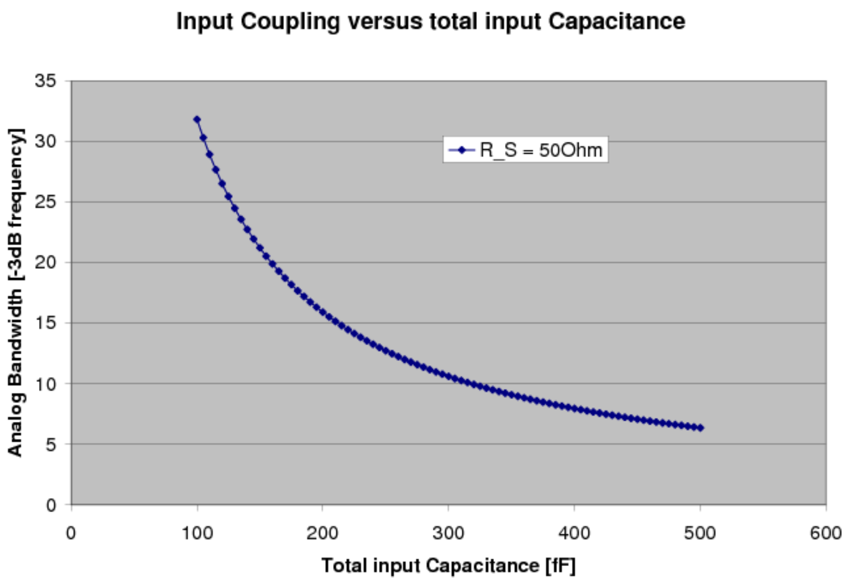
**Difficult to couple in Large BW (C is deadly)**



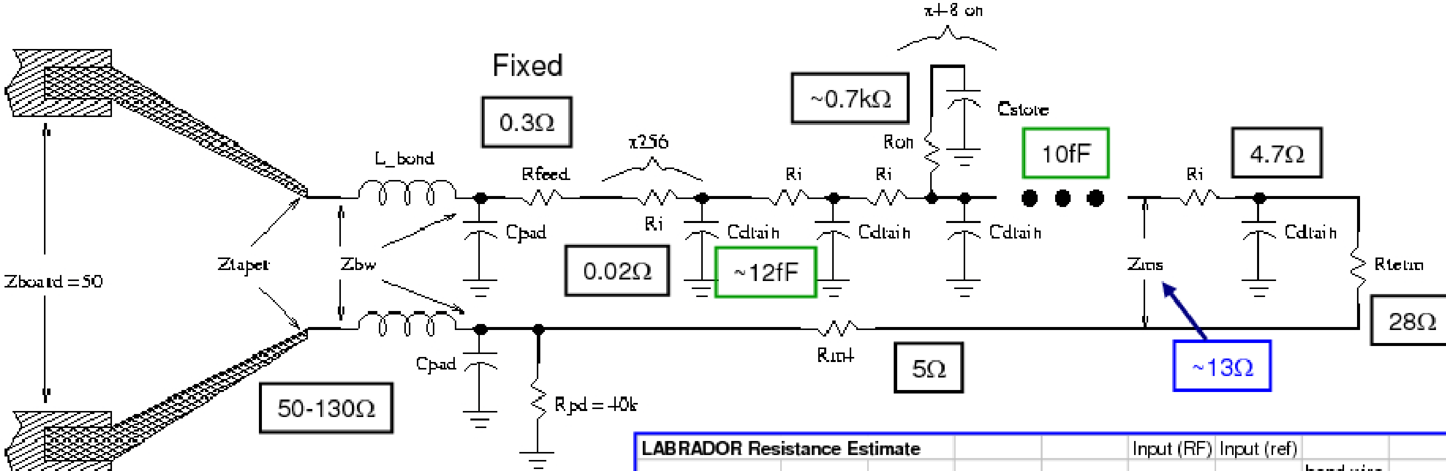



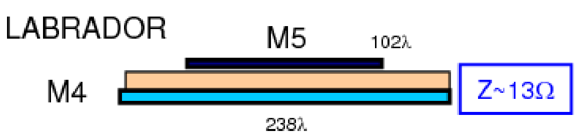

$f_{3dB} = 1/2\pi ZC$



# Constraint 2:  Storage Depth




| LABRADOR Resistance Estimate | | | | | Input (RF) | Input (ref) | | |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | bond wire | |
| **Length** | 17000 | λ | | | 0.0 | 0.1 | pad | |
| | | | 70 | | | 0.2 | M5-M4 | |
| Metal 4(sheet) = | 0.07 | Ohm/sq | | 71.42857 | | 5.0 | typ length (sq.) | |
| Metal 5(sheet) = | 0.03 | Ohm/sq | 166.6667 | | 5.0 | | typ length (sq.) | |
| Poly contact = | 5.1 | Ohm | 6 | 6 | 0.9 | 0.9 | | |
| via 1= | 2.7 | Ohm | 6 | 3 | 0.5 | 0.9 | | |
| via 2= | 5.35 | Ohm | 6 | 3 | 0.9 | 1.8 | | |
| via 3= | 8.26 | Ohm | 6 | 3 | 1.4 | 2.8 | | |
| via 4= | 11.34 | Ohm | 6 | | 1.9 | | | |
| | | | | | 10.5 | 11.5 | Total per feed | |
| | | | | | | | | |
| | | | | | | 28 | Rterminator | |
| | | | | | | | | |
| | | Measured: | | Ohm | | **50.0** | Grand Total | |

## (LAB1 example)

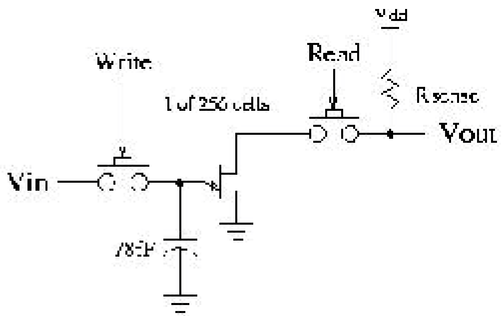
$$f_{3dB} = 1/2\pi ZC$$

Would like smallest possible Cstore

- For 1.2GHz, C <~ 2pF (NB input protection diode ~10pF)
- Minimize C, ($C_{drain}$ not negligible x260)

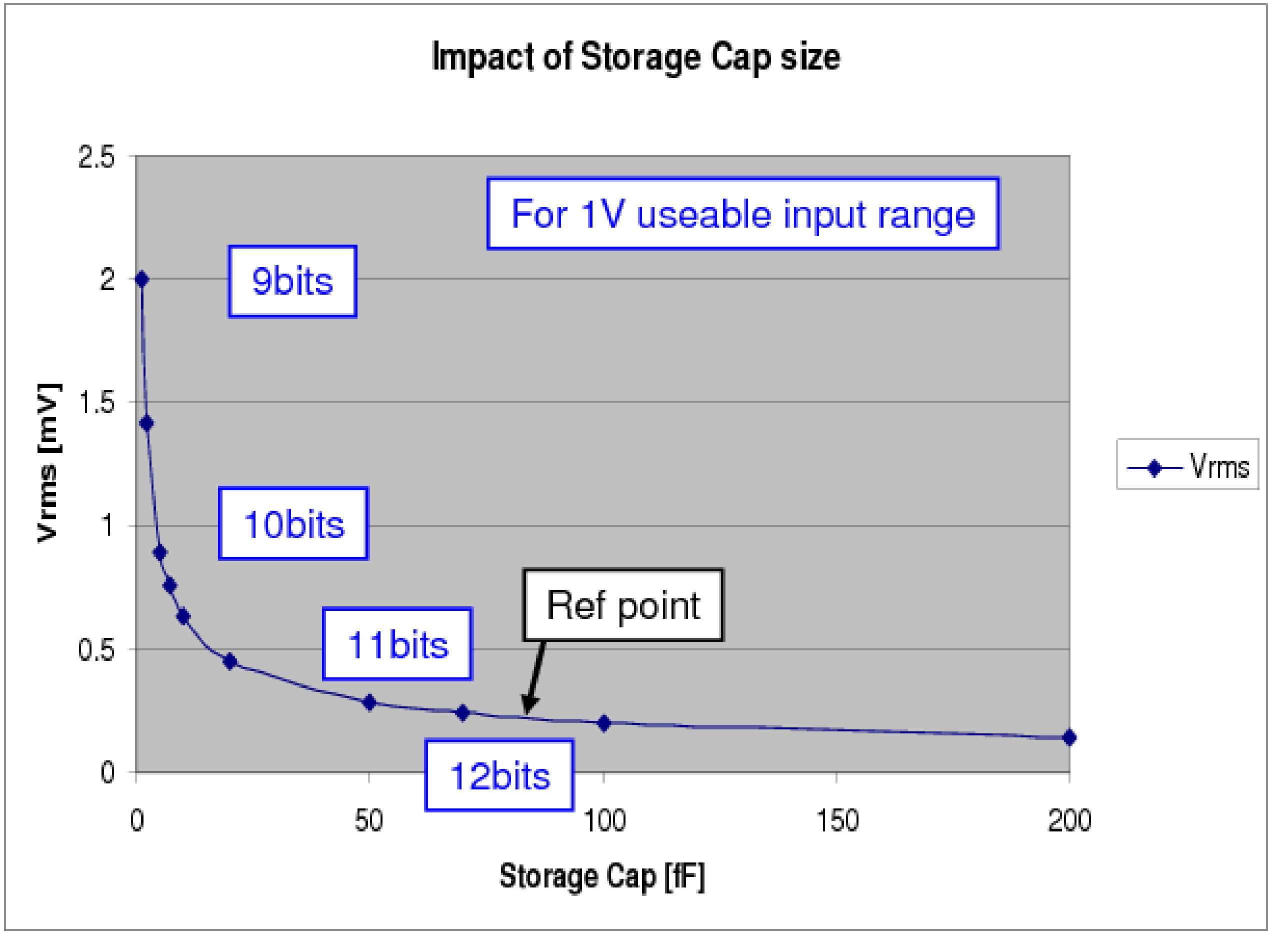
# Constraint 3:  kTC Noise

Want small storage C, but…



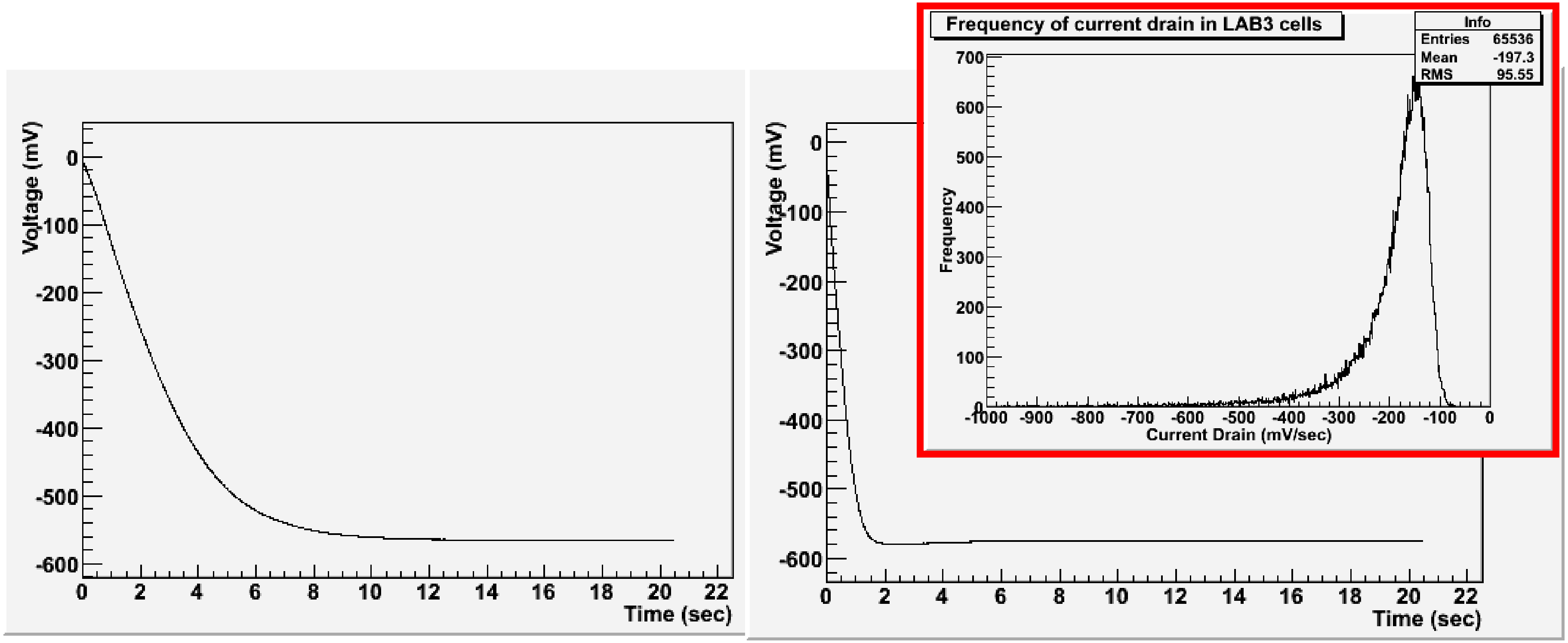

$$v_{rms} = \sqrt{\frac{kT}{C_{store}}} = 0.23mV$$

$C_{store}$ = 78fF



# Similar Constraint 3b:  Leakage Current

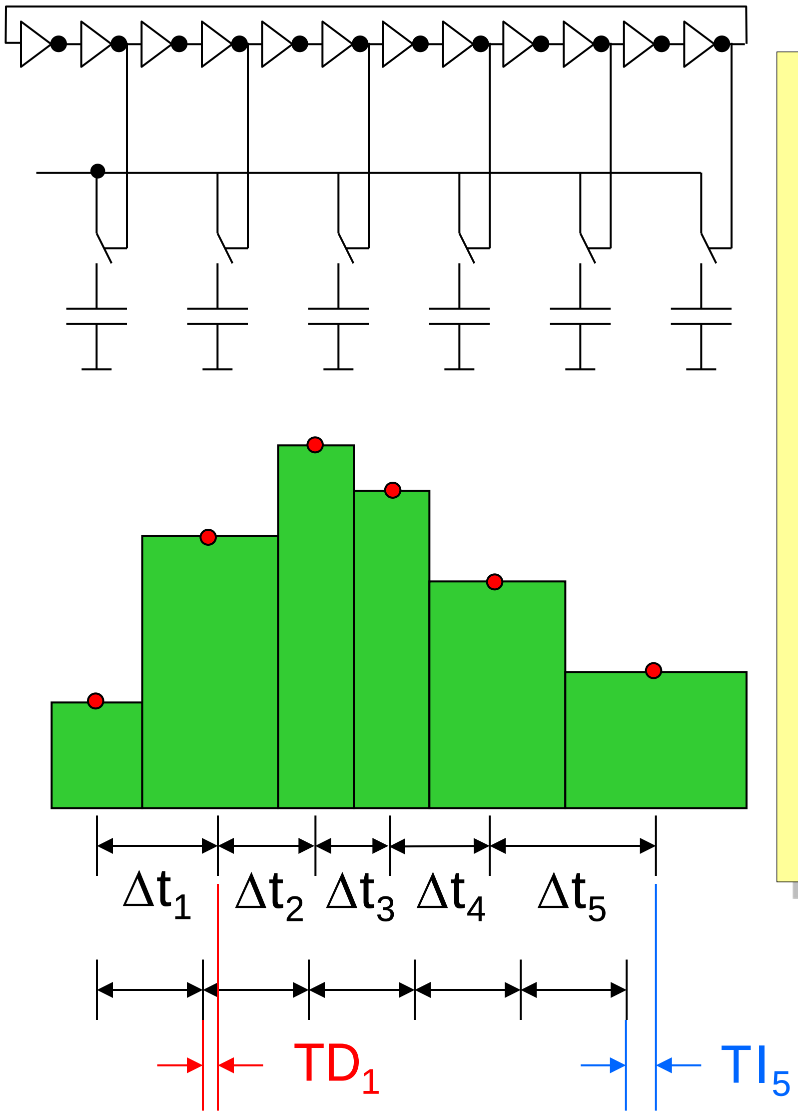
Increase C or reduce conversion time << 1mV




Sample channel-channel variation **~ fA**
leakage typically (0.25um process)

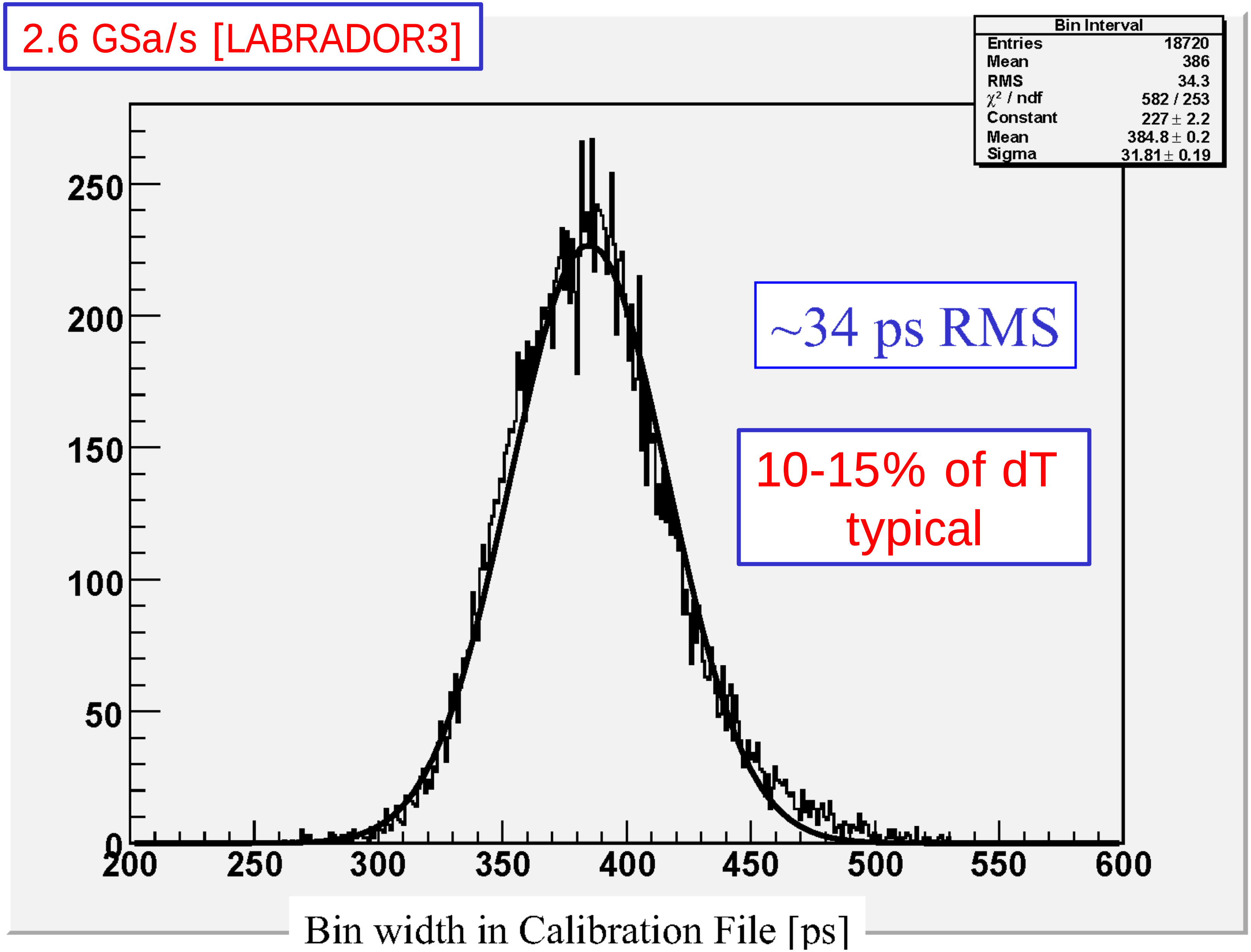
**Becomes much worse in faster (digital) processes**

# Constraint 4: Sample Aperture Variance



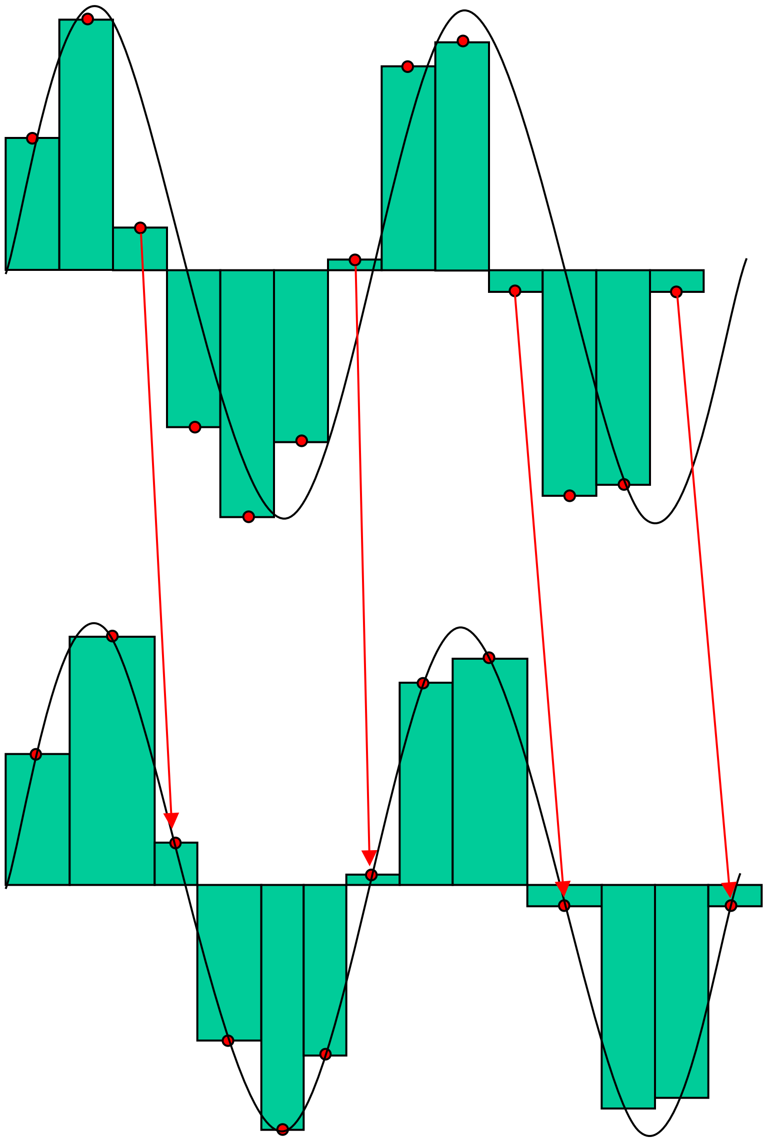

- Inverter chain has transistor variations
  $\rightarrow$ $\Delta t_i$ between samples differ
  $\rightarrow$ "Fixed pattern aperture jitter"
- "Differential temporal nonlinearity"
  $TD_i = \Delta t_i - \Delta t_{nominal}$
- "Integral temporal nonlinearity"
  $TI_i = \Sigma \Delta t_i - i \cdot \Delta t_{nominal}$
- "Random aperture jitter" = variation of $\Delta t_i$ between measurements

# dT Spread



2.6 GSa/s [LABRADOR3]
Bin Interval
Entries 18720
Mean 386
RMS 34.3
χ² / ndf 582 / 253
Constant 227 ± 2.2
Mean 384.8 ± 0.2
Sigma 31.81 ± 0.19
~34 ps RMS
10-15% of dT typical
0
50
100
150
200
250
200
250
300
350
400
450
500
550
600
Bin width in Calibration File [ps]

# Average aperture calibration



- Fixed aperature offsets are constant over time, can be measured and corrected
- Several methods are commonly used (sine fit [left], zero-crossing)
- Most use sine wave with random phase and correct for $TD_i$ on a statistical basis

**Great progress in improved algorithms:**

http://arxiv.org/abs/1405.4975

**However still computationally expensive (e.g. resampling for FFTs)**