STURM2 Evaluation Board

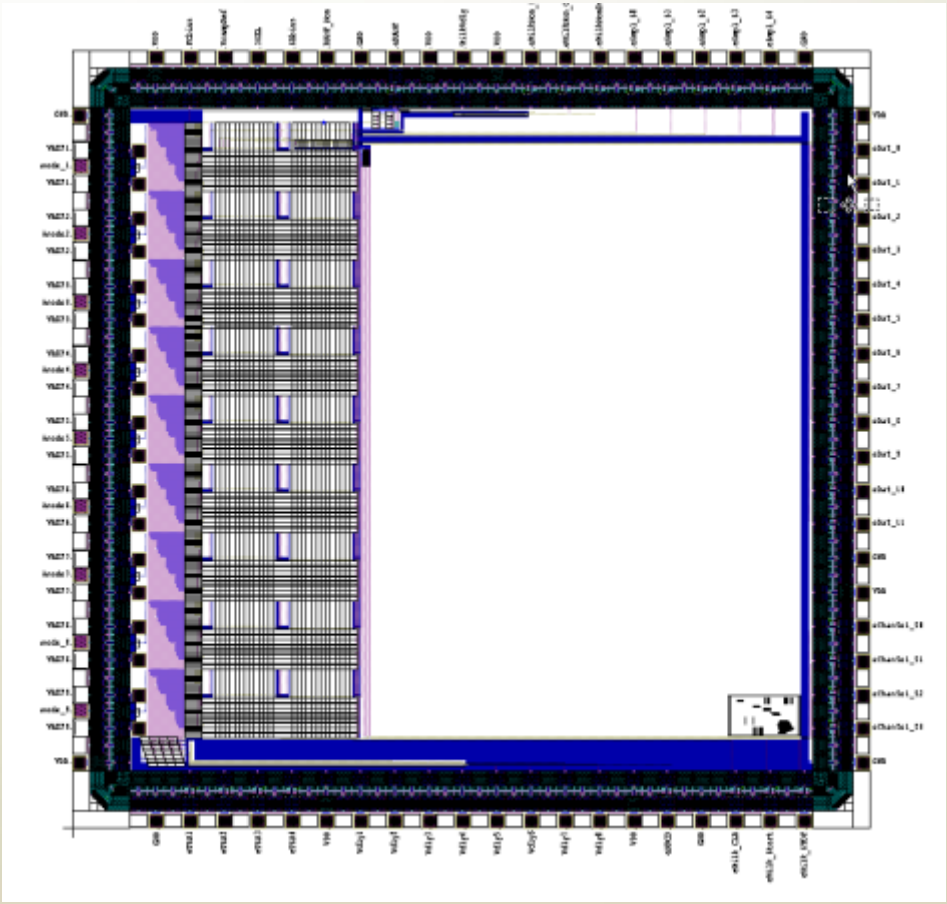
EE396 Project by Christian-Paul Borromeo

Overview

- What is the STURM2?
- My role
- What has been done
- What is left to complete

What is the STURM2

- Sampler of Transient Uniform Redundant Mask version 2
- Sample rate of over 10 GSa/s
- Custom chip with the capability to sample at very high rates



My Role

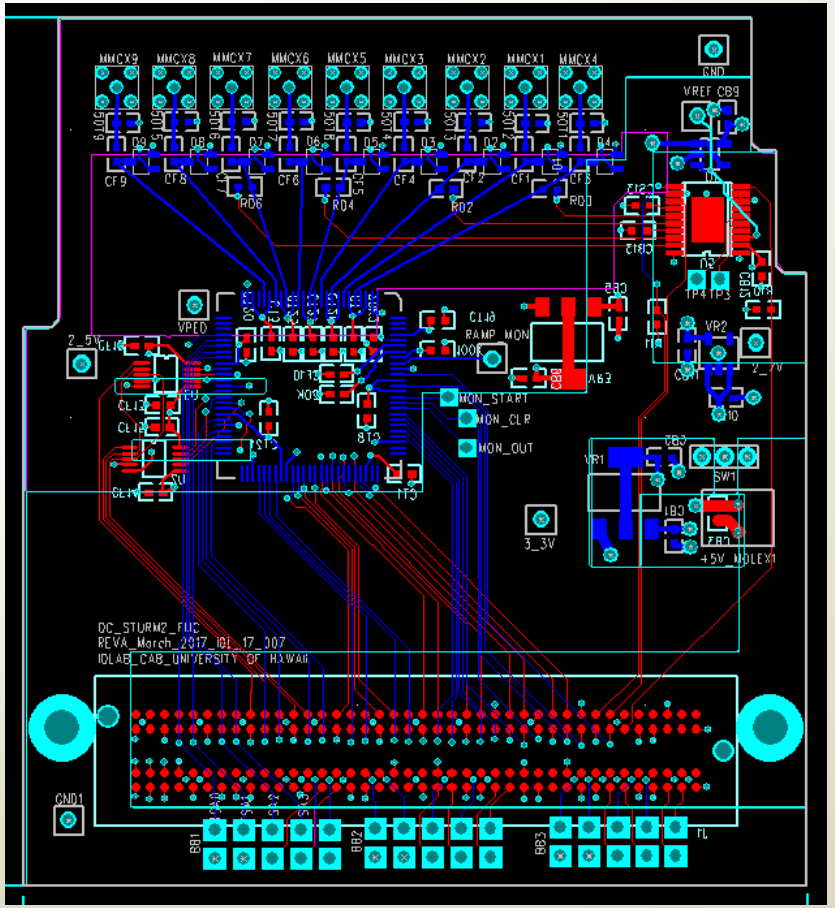
Test out the ASIC and to see if it functions as intended

This includes but not limited to:

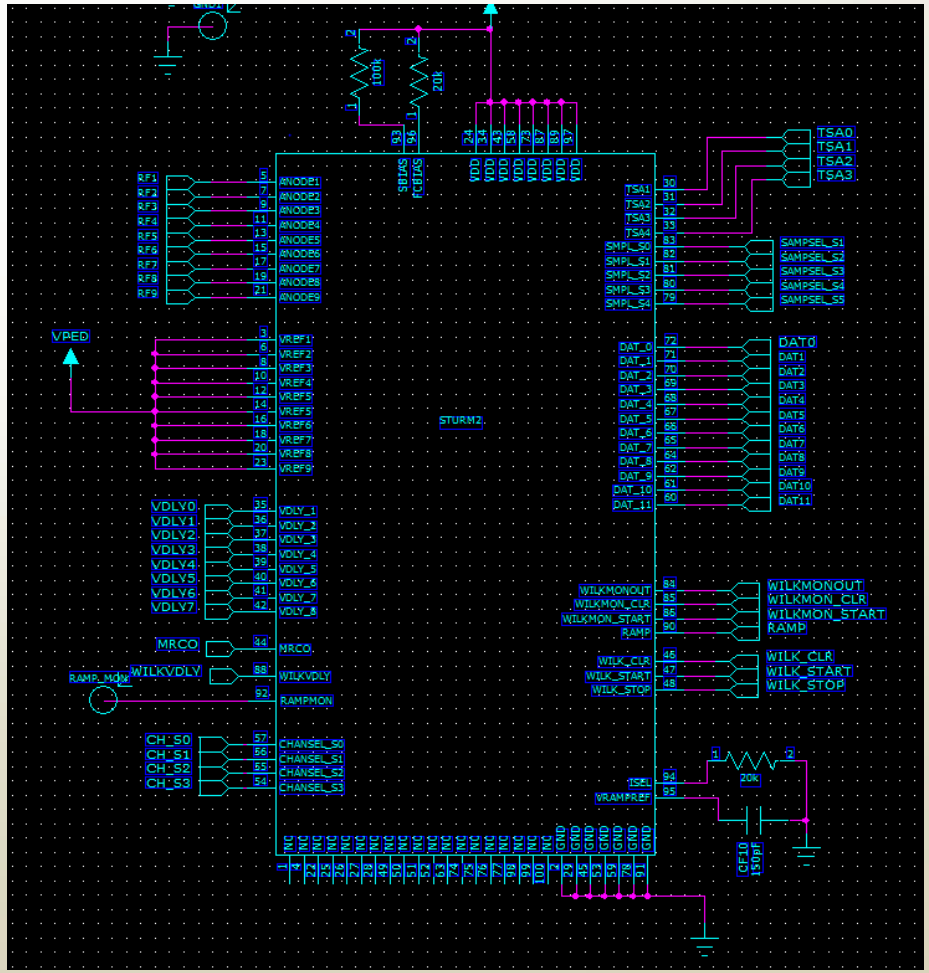
- Design and fabricate evaluation board for testing
- Write firmware for said board
- Hopefully have data readout

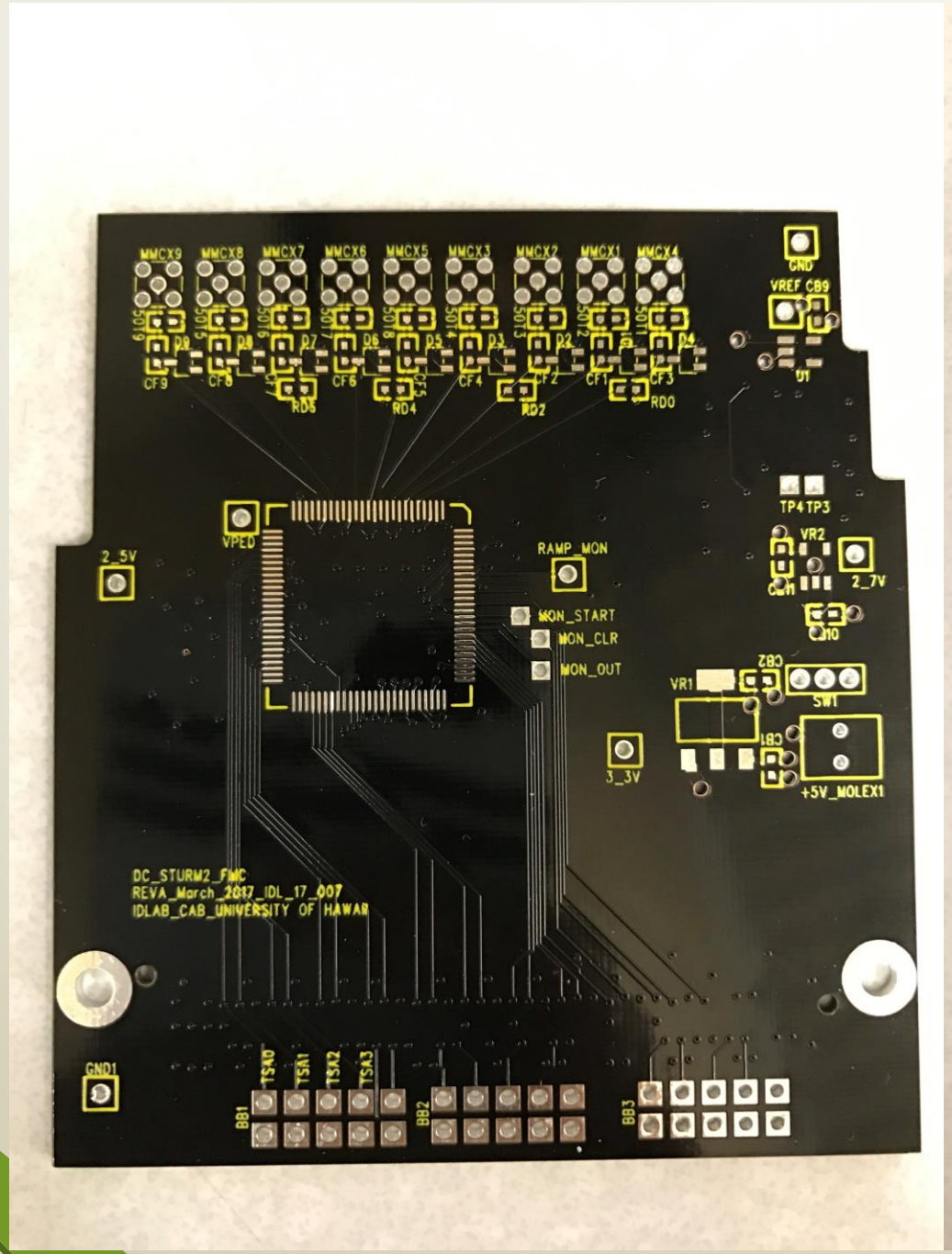
What has been done?

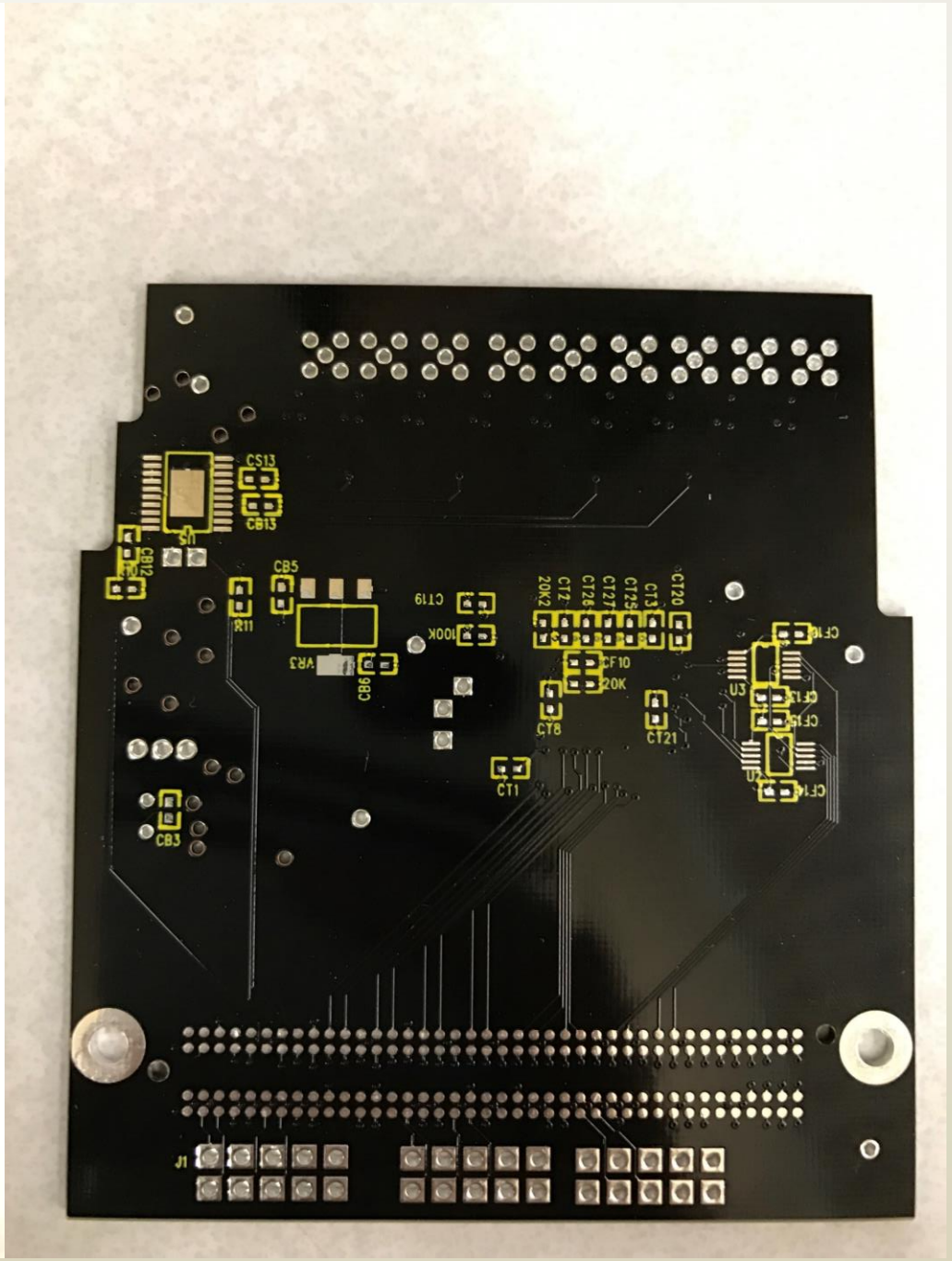
- Board schematic and layout has been created using PADS Mentor
- Went though extensive review from others before being sent out (thanks for all the help everybody)
- Received boards from PCBuniverse



- Looked towards the TargetX board for inspiration
- Four Layer board
  1. Top Signal
  2. Ground
  3. Power
  4. Bottom Signal
- Designed to keep 50-ohm impedance along analog lines




MMCX9
MMCX8
MMCX7
MMCX6
MMCX5
MMCX3
MMCX2
MMCX1
MMCX4
GND
VREF_CB9
TP4 TP3
VR2
2_7V
2_5V
VPED
RAMP_MON
MON_START
MON_CLR
MON_OUT
VR1
SW1
3_3V
+5V_MOLEX1
DC_STURM2_FMC
REVA_March_2017_IDL_17_007
IDLAB_CAB_UNIVERSITY OF HAWAI
GND1
TSA0
TSA1
TSA2
TSA3
BB1
BB2
BB3


CS13
CB13
CB12
CB5
CB6
CB3
CT1
CT8
CT21
CF10
20K
100K
J1
U3
U2

What is left to complete

EVERYTHING!!!!

What is left to complete

- Assemble board
- Write Firmware for board (Hopefully finished a few modules by end of summer)
- Next semester, will hope to be to see ASIC fully implemented

Recap

- STURM2 is a sampler with sample rate of over 3GSa/s
- My role is to characterize the STURM2 ASIC
- The design and fabrication of Evaluation board has been completed
- Assembly, Firmware needs to be finished. Then the real fun begins

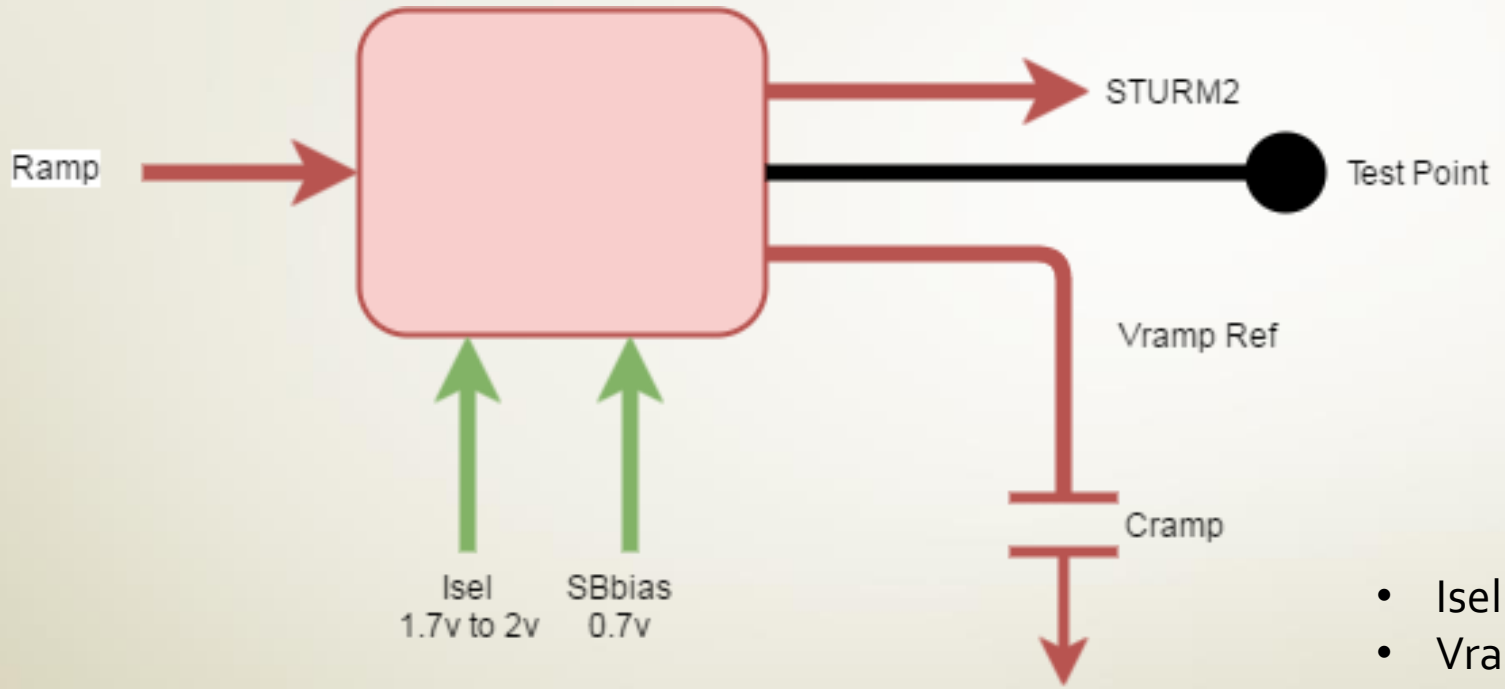
Things I've Learned/ will Learn

- Implemented material learned in previous courses when dealing with impedance control
- Learned PCB design
- Has gained greater urgency for time management
- Will learn micro soldering/ surface mount soldering
- Will build upon knowledge of VHDL

Questions?

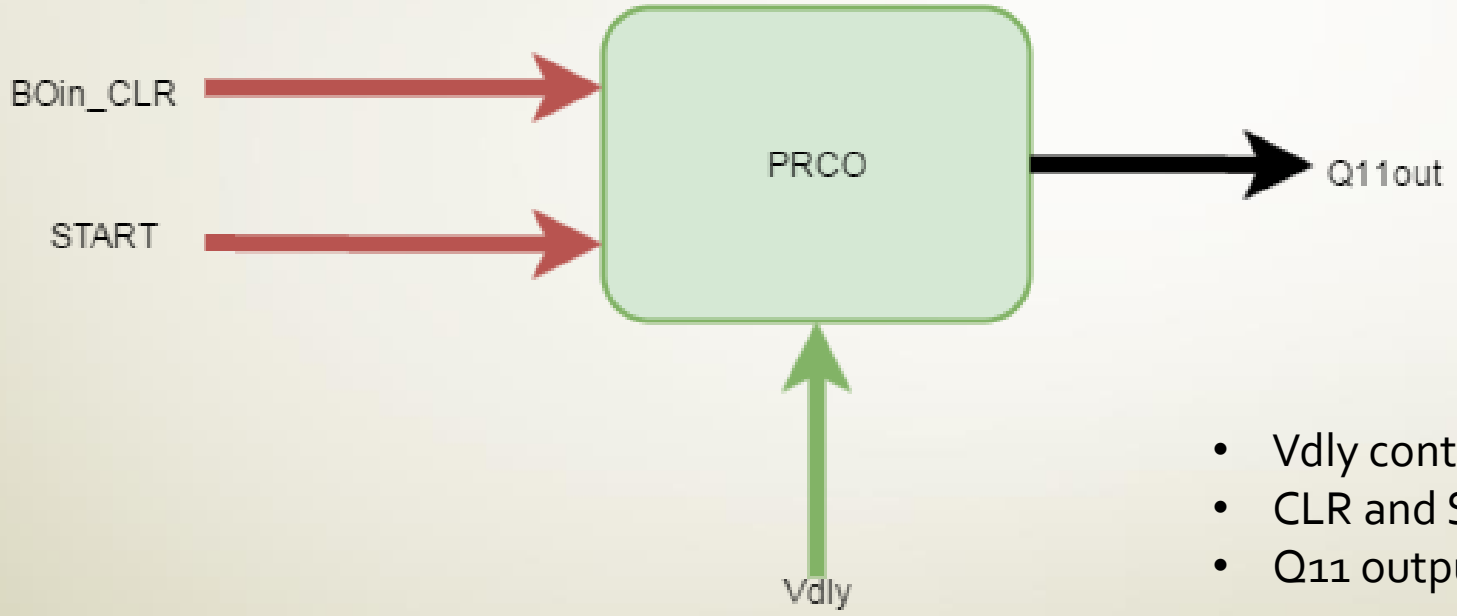

Thank You
DC_STURM2_FMC
REVA_March_2017_IDL_17_007
IDLAB_CAB_UNIVERSITY OF HAWAII
GND1
TSA0
TSA1
TSA2
TSA3

Vramp Block



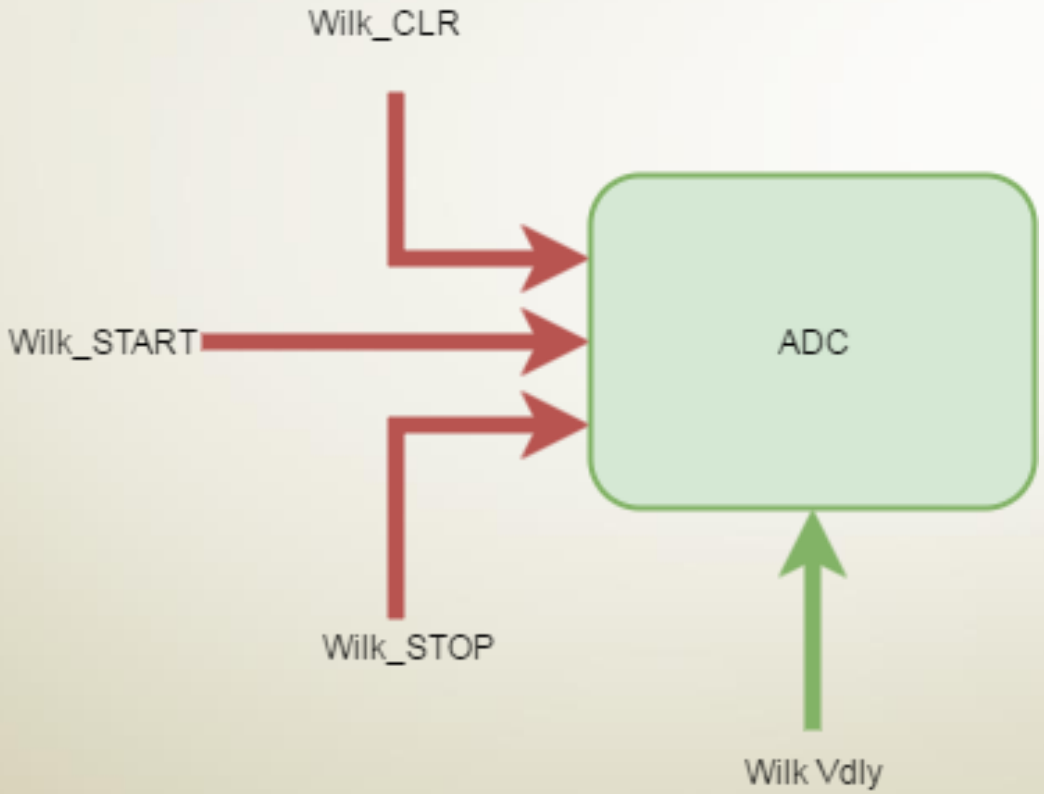
- Isel controls slope of Vramp
- Vramp Ref for Wilkinson
- SBbias for buffer

Wilkinson ADC Monitor



- Vdly controls the sampling speed
- CLR and START to start sampling
- Q11 output

Wilkinson Conversion ADC



- Wilk CLR, START, STOP controls sampling
- Vdly controls sampling speed

Data Readout